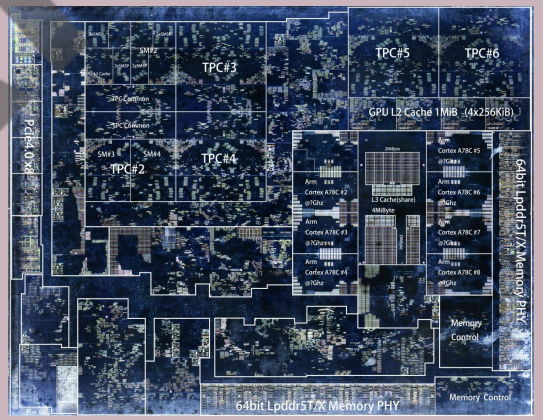
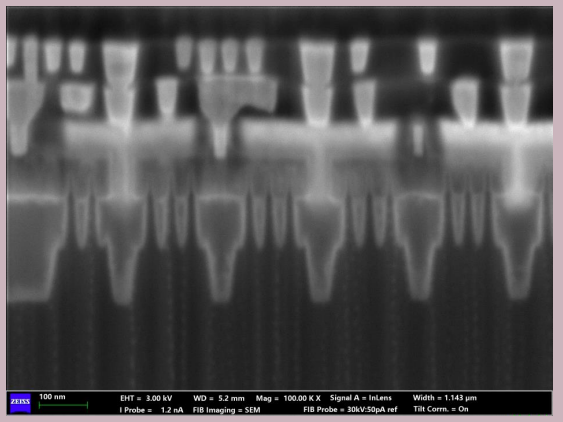
Nintendo Switch 2

Chip and Process analyze

V1.1

@Kurnal





Verison of this Report

Version	Date	Updates	Anthor
V0	2025/04/23	Working	Kurnal
V1	2025/05/07 22:51	Finish ?	Kurnal
V1.1	2025/05/08 20:53	修改了语法（感谢雪球老师！）	Kurnal/雪球
B站工坊			

This report is not for commercial use

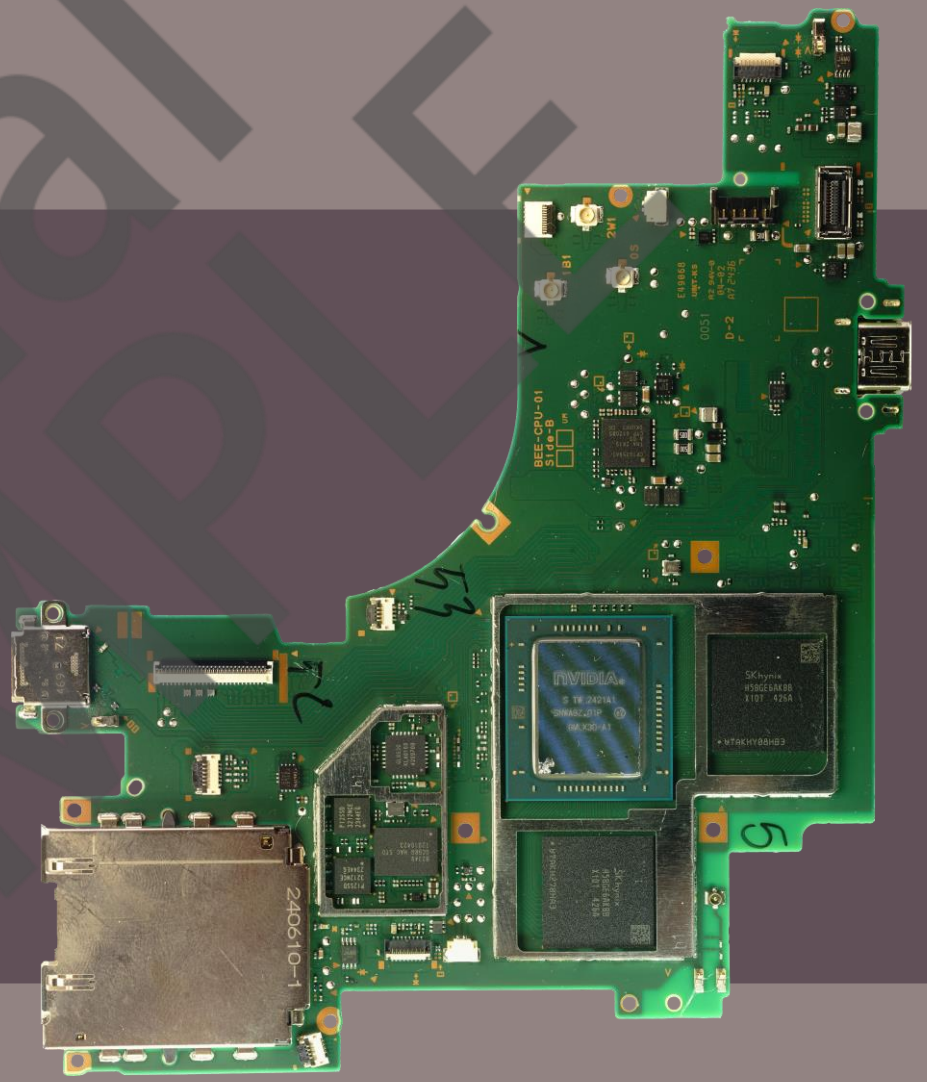
This Report is made From @Kurnal

BiliBili: @Kurnal
X: @Kurnalsalts
WeChat: KurnalWeChat

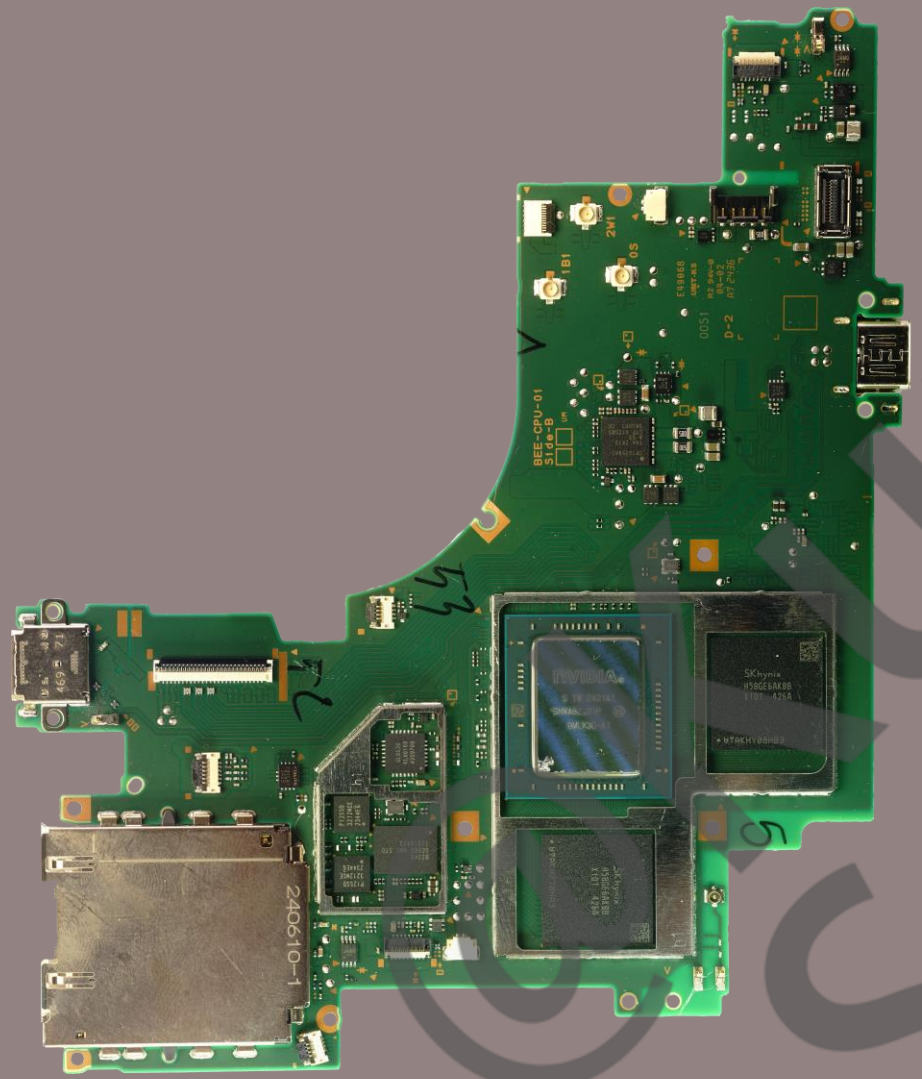
This report is not for commercial use

Mother board

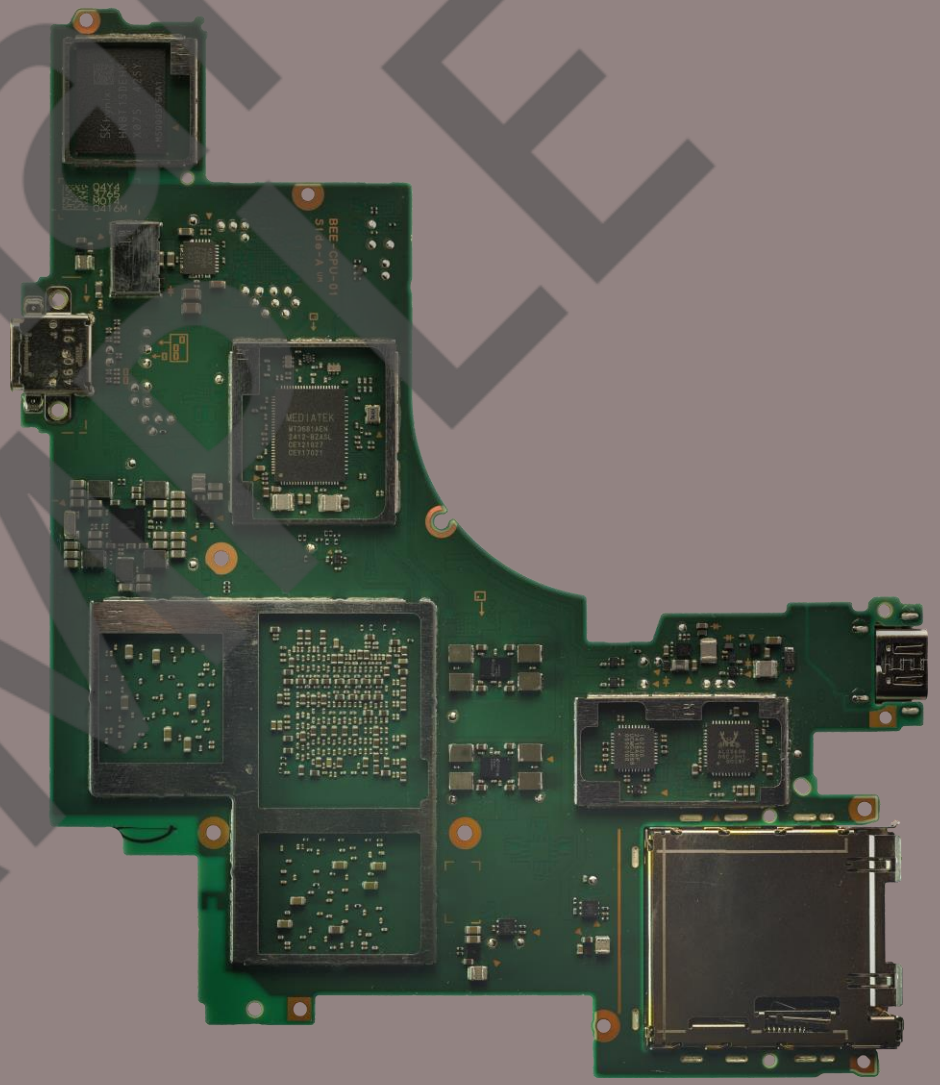
Component analyze



Mother board analyze

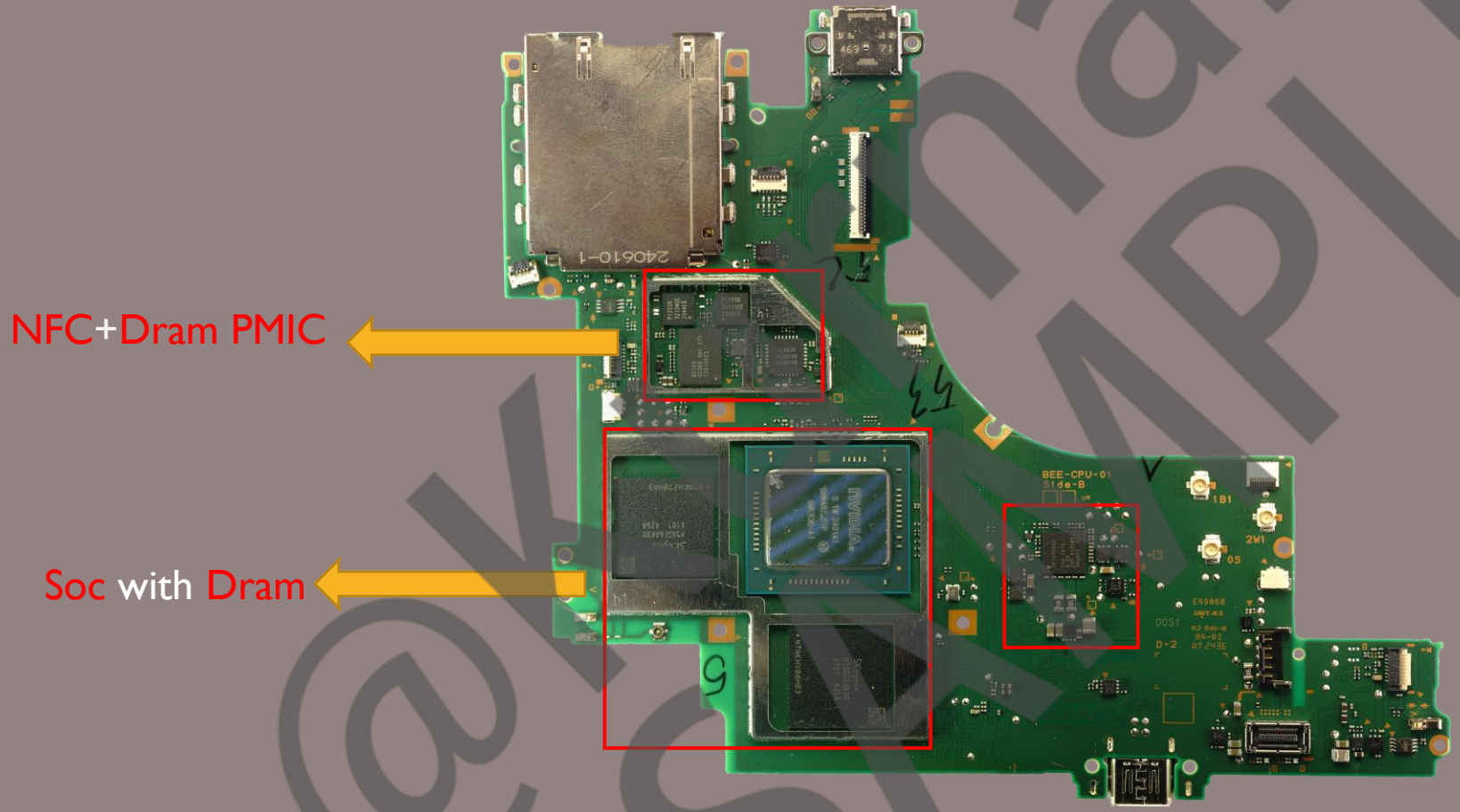


PCB frontside photo



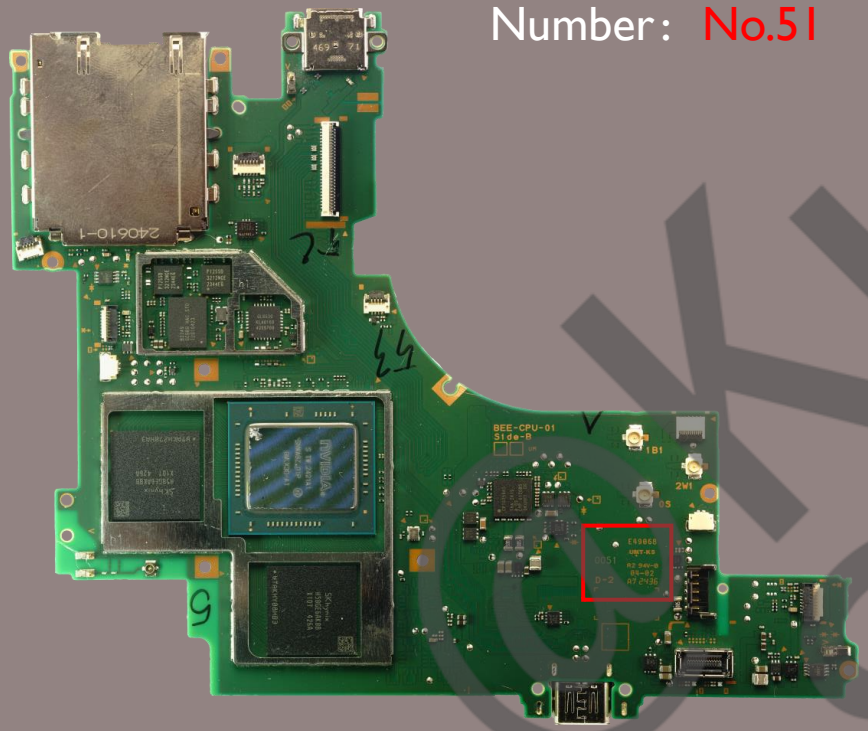
PCB backside photo

PCB-Frontside

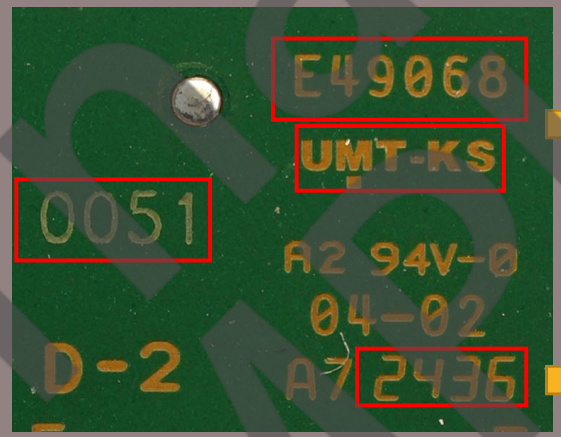


PCB frontside photo

PCB-Frontside-mark



PCB frontside photo



Number： No.51

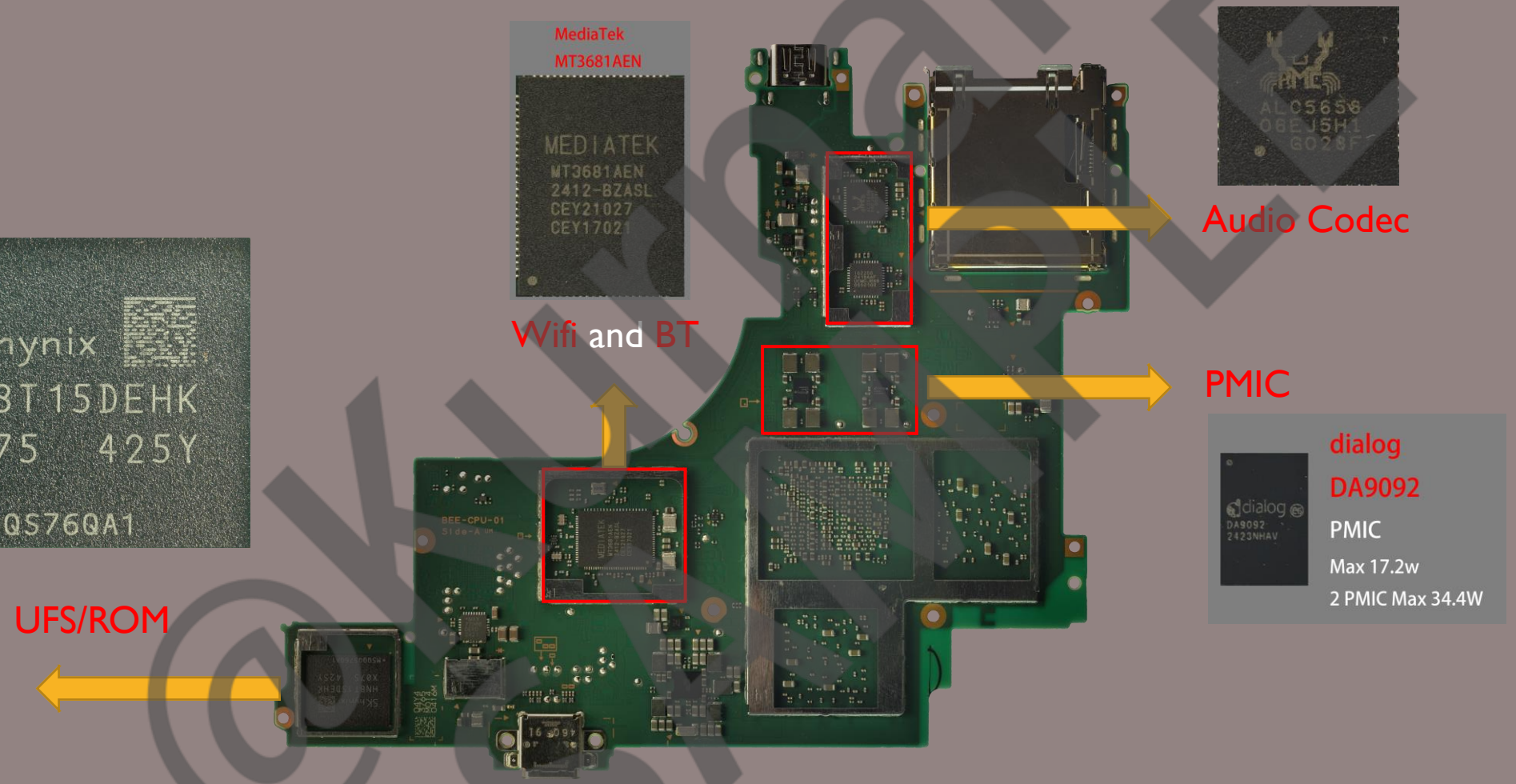
Unimicron 欣興電子

PCB made From Unimicron

欣兴电子

PCB made on 2024-Week36

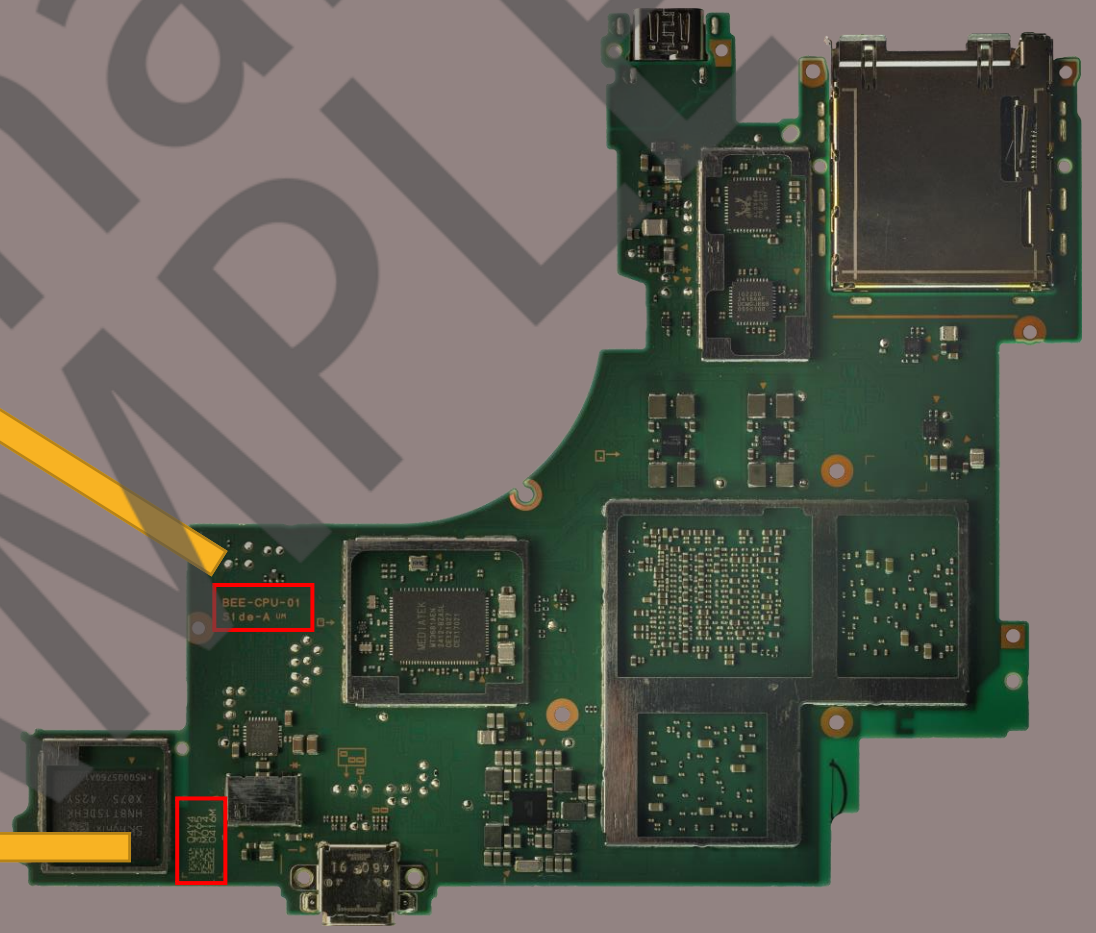
PCB-Backside



PCB backside photo

PCB-Backside-mark

Running code



PCB backside photo

PCB total chip

Dram From Sk hynix

ROM From Sk hynix

PCB total chip

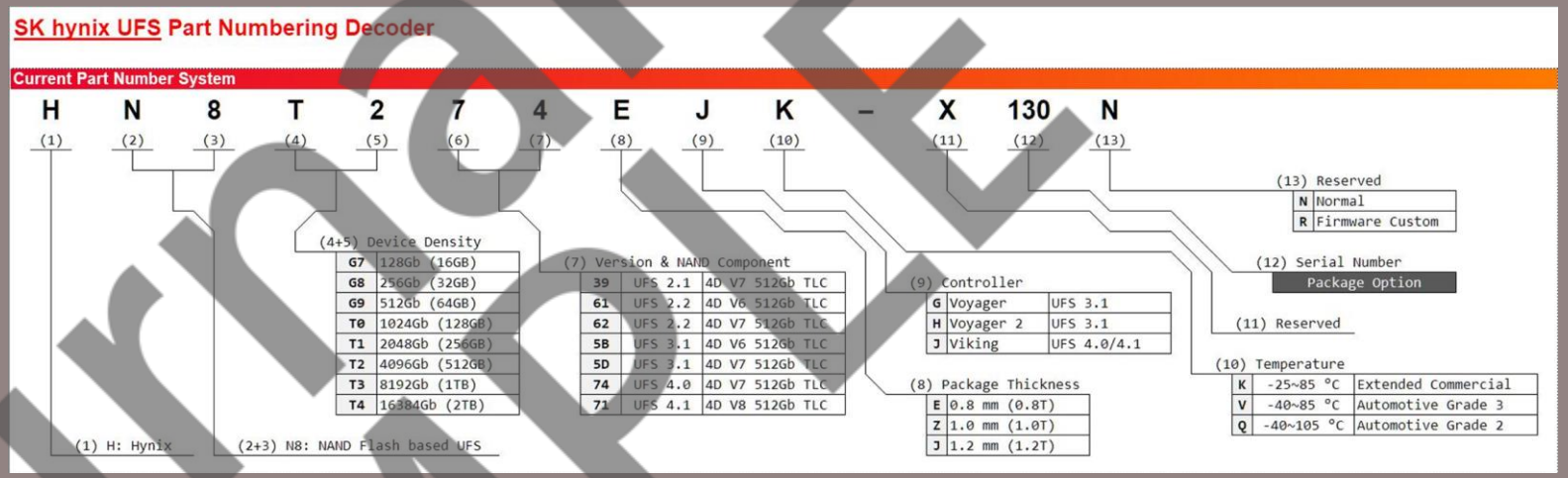
Dram From Sk hynix

H58GE6AK8PX107N	6GB	1.8V / 1.05V / 0.5V	8533Mbps	441Ball	MP
H58GE6AK8QX107N	6GB	1.8V / 1.05V / 0.5V	8533Mbps	441Ball	MP
H58GE6AK8VX107N	6GB	1.8V / 1.05V / 0.5V	8533Mbps	441Ball	MP

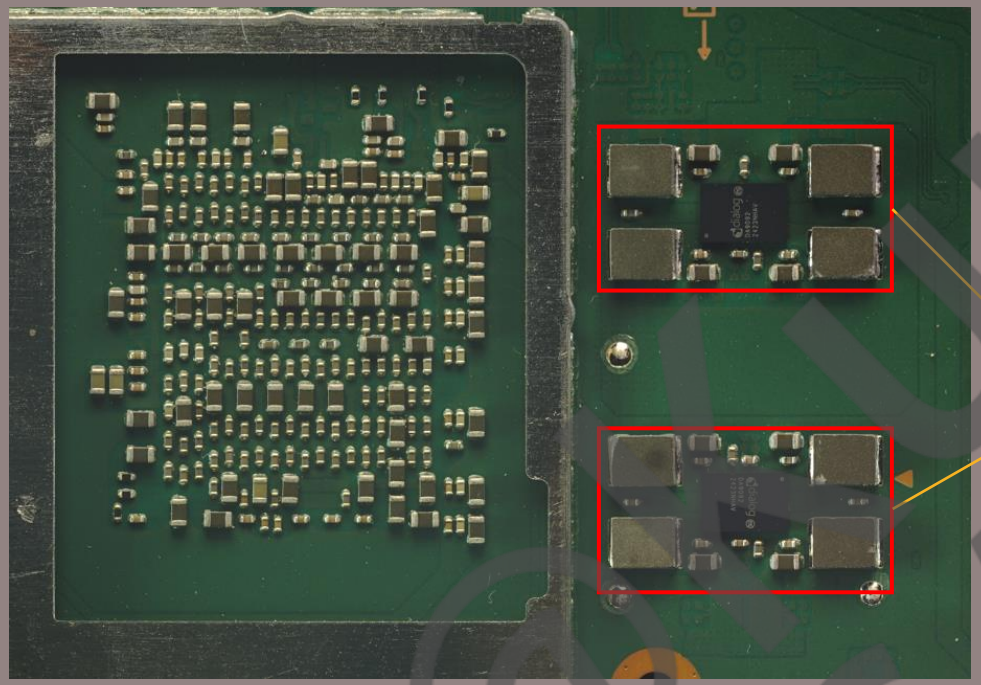
H58GE6AK8B X107
LPDDR5T/5X
8533MT/s 4266MHz/s
Pkg Density: 6GB
DIE: 12Gb A-die
PKG: BGA-441

PCB total chip

ROM From Sk Hynix



Hynix UFS 3.1
2048Gb/256GB
4D v7 512Gb TLC
Package Thickness : 0.8mm
Controller: Voyager2
Extended commercial



Soc PMIC

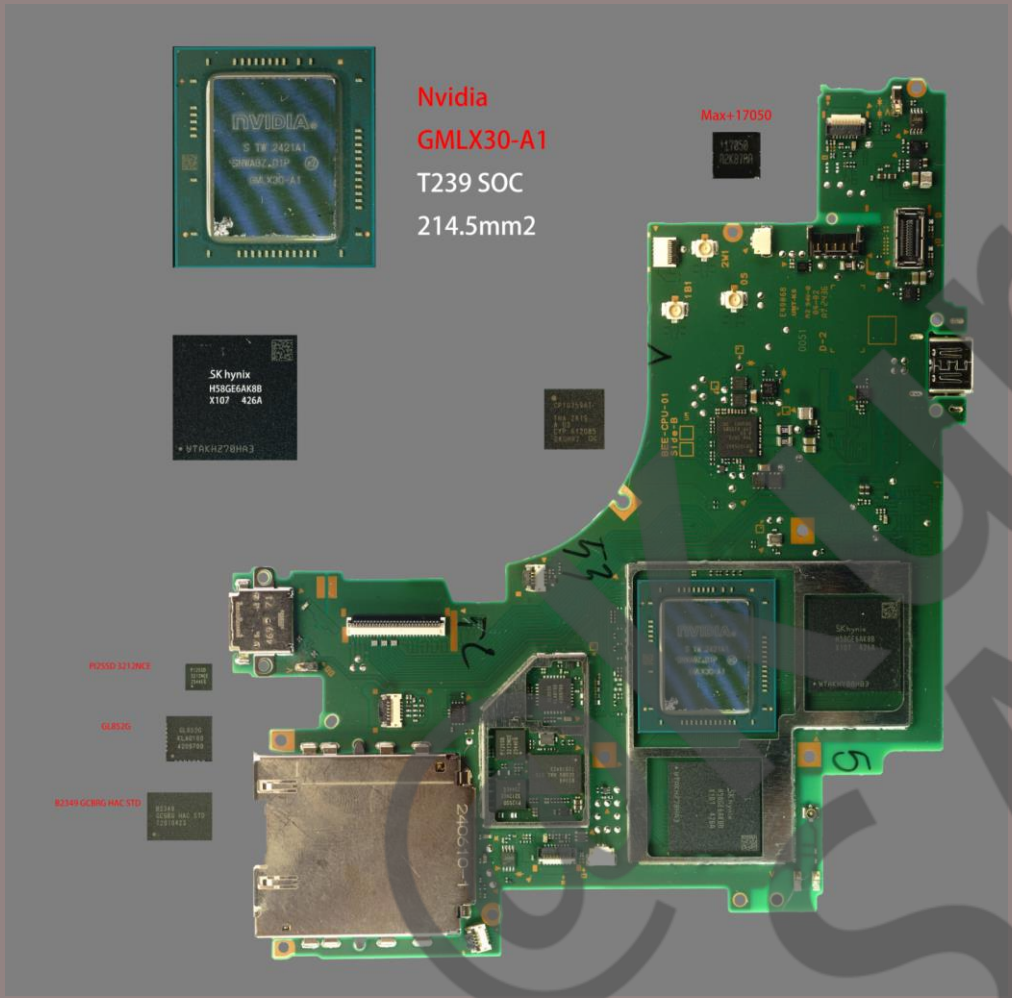
Dialog
DA9092

Key Features

- Input voltage 2.8 V to 5.5 V
- Four buck converters with dynamic voltage control:
  - Buck1: 0.3 V to 1.57 V, 2.5 A
  - Buck2: 0.3 V to 1.57 V, 2.5 A (can be used in dual-phase configuration with Buck1)
  - Buck3: 0.8 V to 3.34 V, 2 A
  - Buck4: 0.53 V to 1.8 V, 1.5 A (can be used as DDR VTT supply)
- 3 MHz switching frequency (enables low profile inductors)
- Four LDO regulators:
  - LDO1: 0.9 V to 3.6 V, 100 mA
  - LDO2, LDO3, LDO4: 0.9 V to 3.6 V, 300 mA
- Programmable power mode sequencer
- System supply and junction temperature monitoring
- Watchdog timer
- Five GPIOs
- Coin cell/super-capacitor charger
- Ultra-low power RTC with alarm
- 32 kHz oscillator with external crystal
- -40 °C to +125 °C junction temperature range
- 40-pin QFN 6 mm × 6 mm package, 0.5 mm pitch (exposed paddle)
- Automotive AEC-Q100 Grade 2 version available

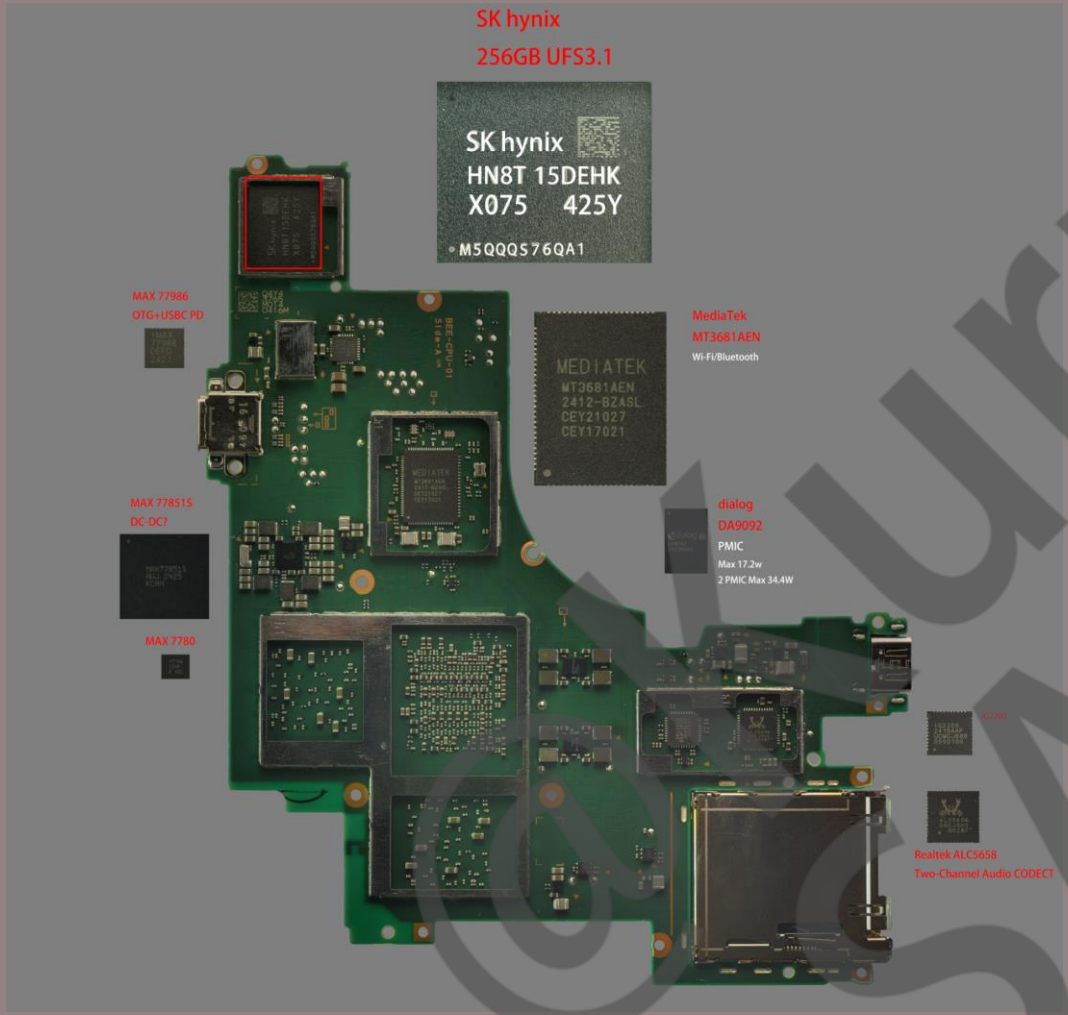
One PMIC Maximum 17.2w
Total Power Maximum 34.4w

PCB total chip



Top side chip	
T239 SOC	Nvidia GMLX30-A1
LPDDR	SK Hynix H58GE6AK8B X107 426A
?	PI2SSD 3212NCE
?	GL852G
?	B2349 GECBRG HAC STD
?	CP10359AT
Battery?	Max+17050

PCB total chip



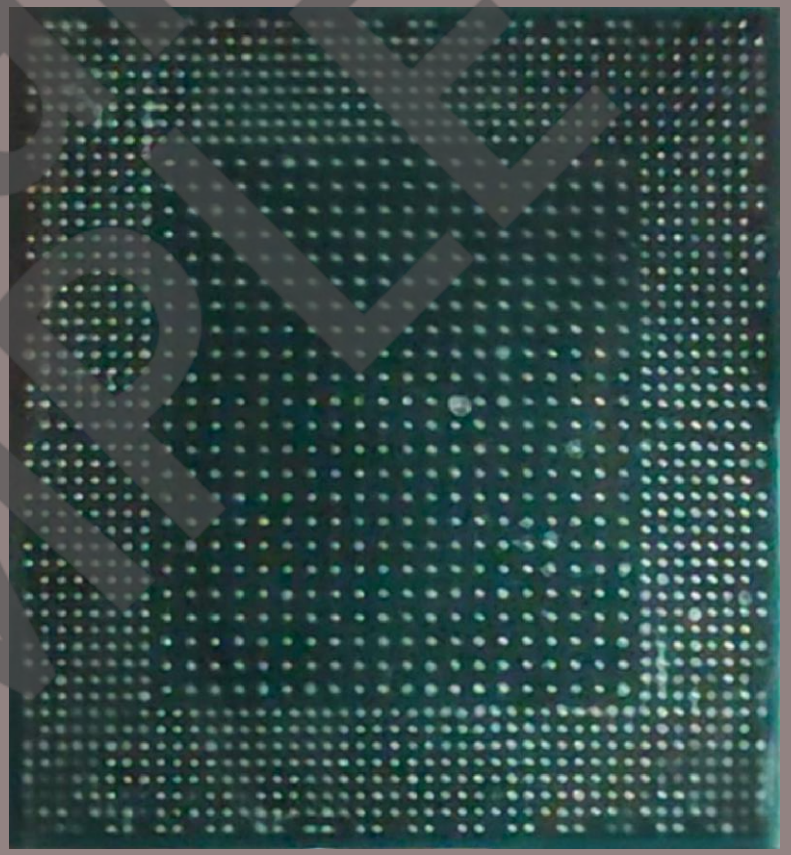
Back side chip	
UFS3.1 256GB	SK Hynix HN8T 15DEHK X075 425Y
WIFI/BT	MediaTek MT3681AEN
PMIC	Dialog DA9092
Audio	Realtek ALC5658
?	IG2200
USB DC-DC?	MAX 77851S
	MAX7780
OTG/USB PD	MAX 77986

Switch2 soc analyze

Package Analysis

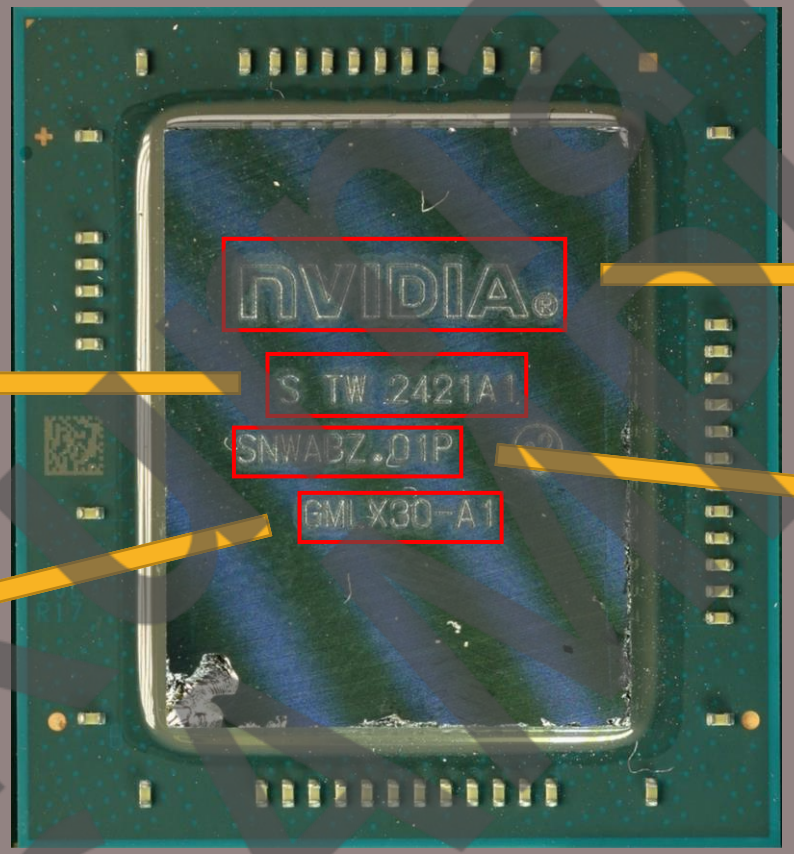
Package

GMLX30 topside photo



GMLX30 bottom side photo

Package – top mark



GMLX30 topside photo

The chip is from Nvidia

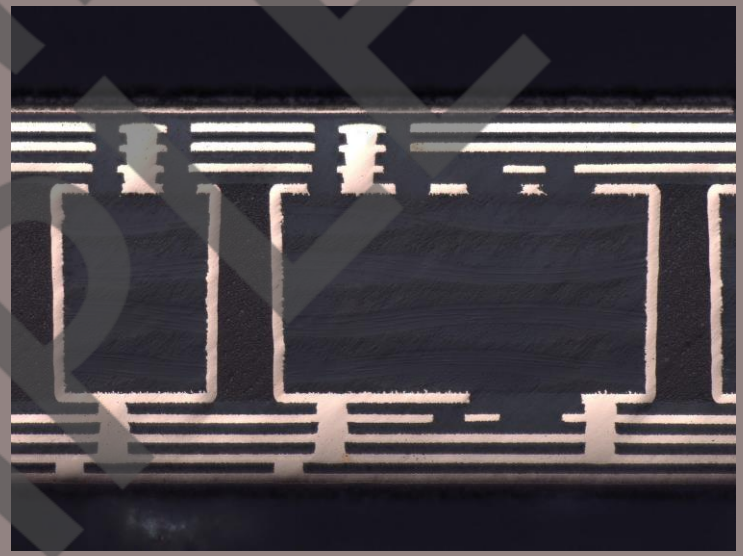
S: Packaged From ASE Group
TW: Packaged in Taiwan
2421:Made on 2024-Week 21

Traceability Code

Code named GMLX30-A1

Package – top mark

GMLX30 topside photo

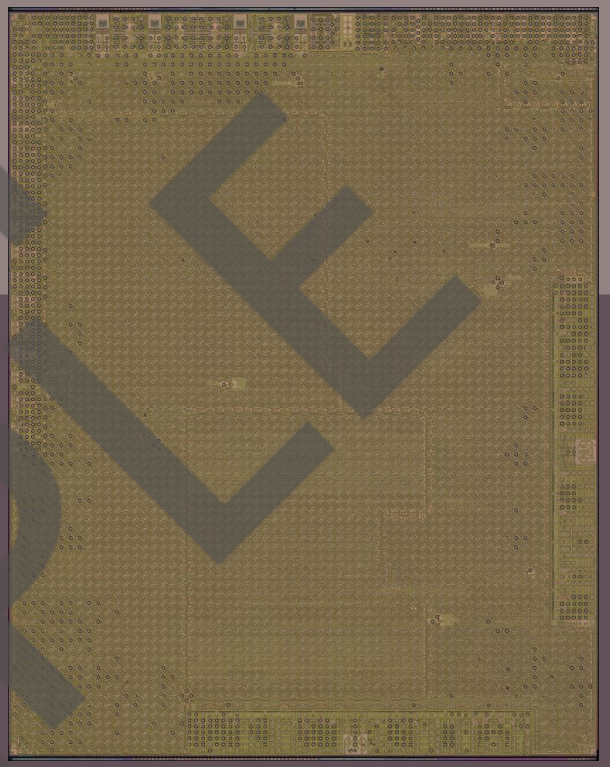


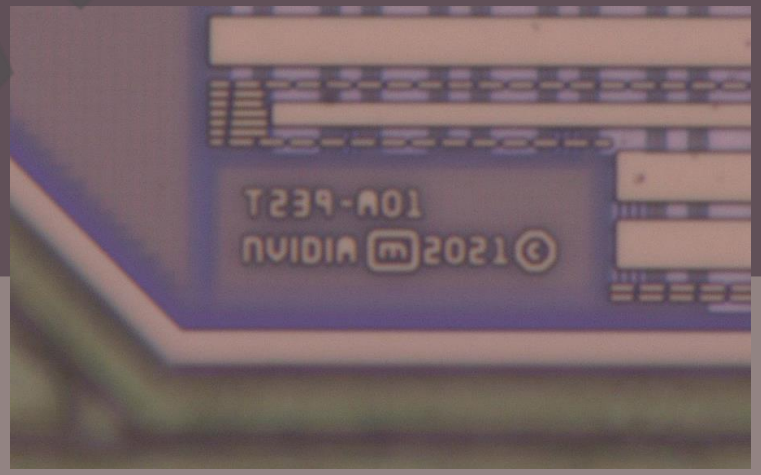
Interposer PCB layers: 10 Layers

The GMLX30 SOC used package named Filp-Chip Fan Out Package(FCFOP/FCBGA)

Switch2 soc analyze

Die-AnalySIS

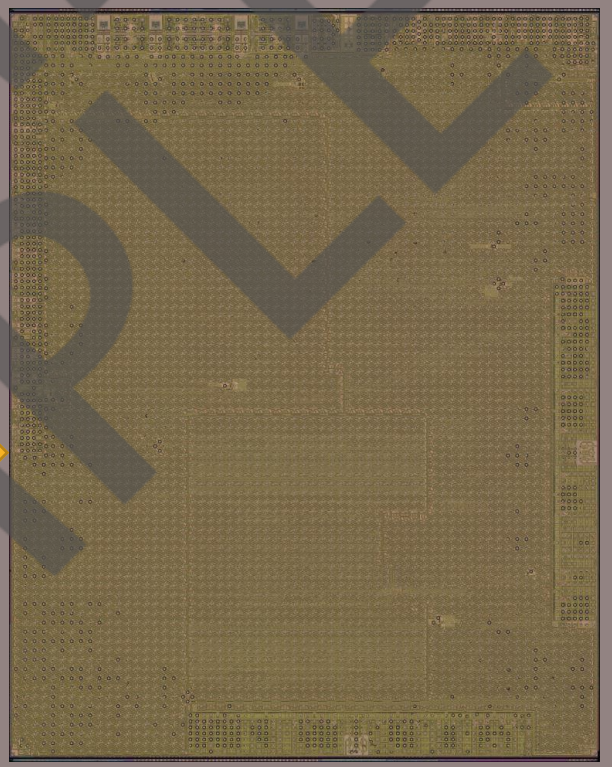




Die analyze

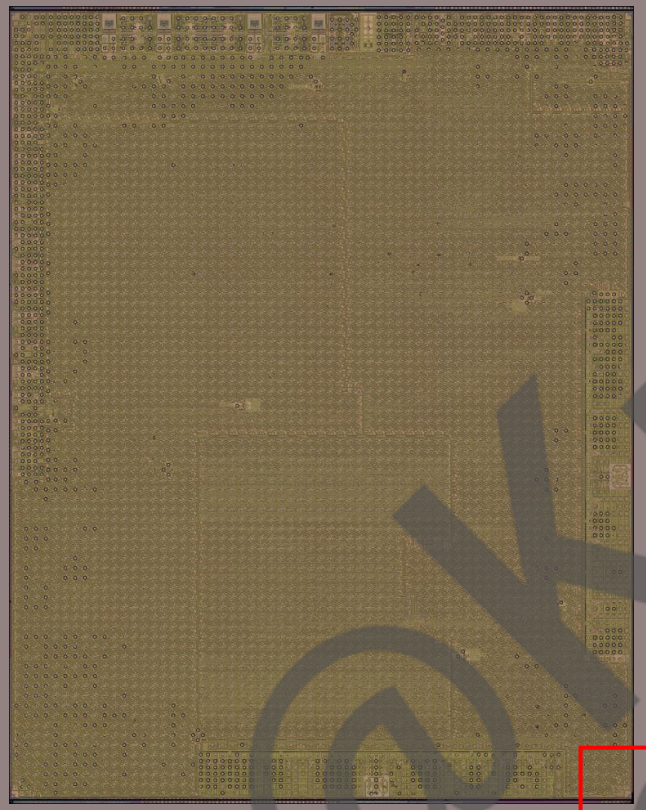
GMLX30 topside photo

Decapped

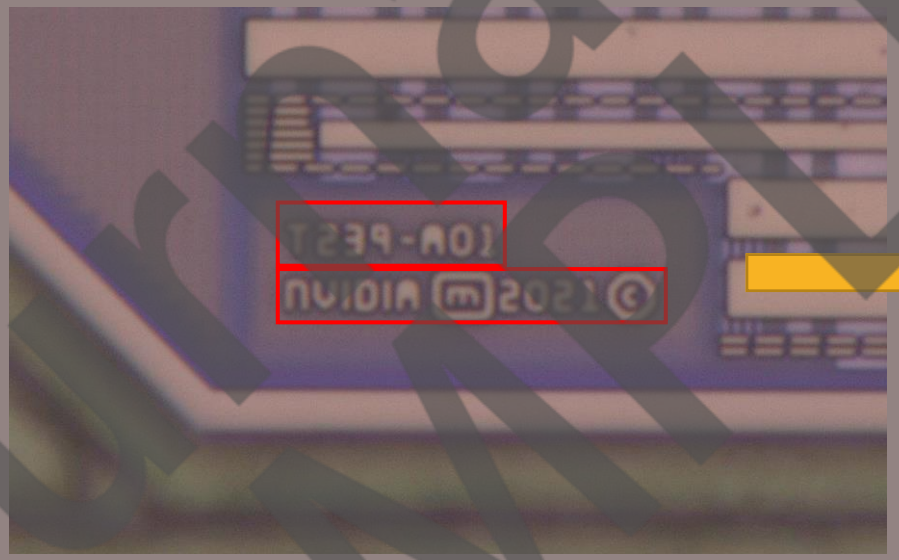


GMLX30 metal layer Views

Die analyze



GMLX30 metal Views



Diemark

Chip name: T239-A01
Tap out : Nvidia M 2021 C

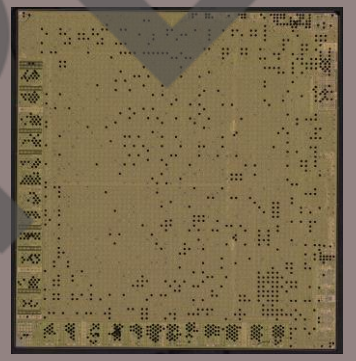
GDS Freeze in 2021?

Die analyze

GA107 topside photo

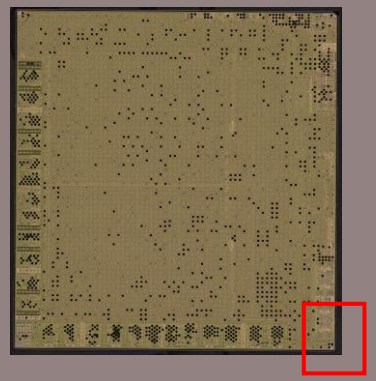
This is a similar chip to Nvidia GA107
(RTX 3050)

Decapped

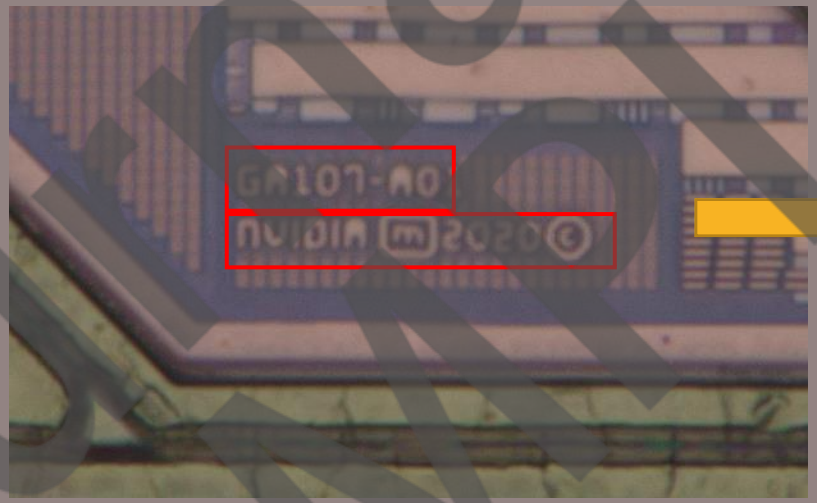


GA107 metal layer Views

Die analyze



GA107 metal Views

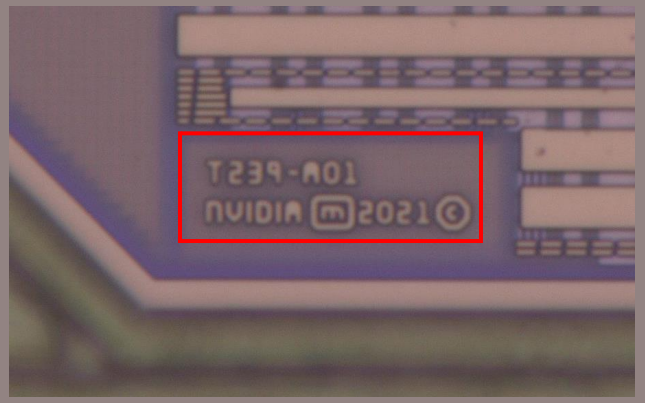


Diemark

Chip name: GA107-A0
Tap out : Nvidia M 2020 C

GDS Freeze in 2020?

Die analyze

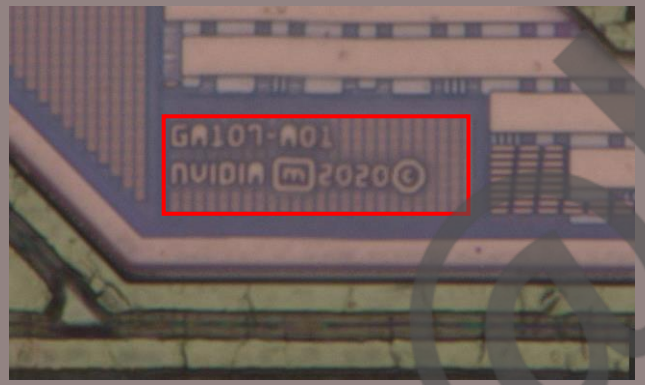


Switch2 soc Diemark

Chip code: T239-A01
Freeze date : Nvidia M 2021 C

In Nintendo Switch2
Release date: 2025/6/05

4years later



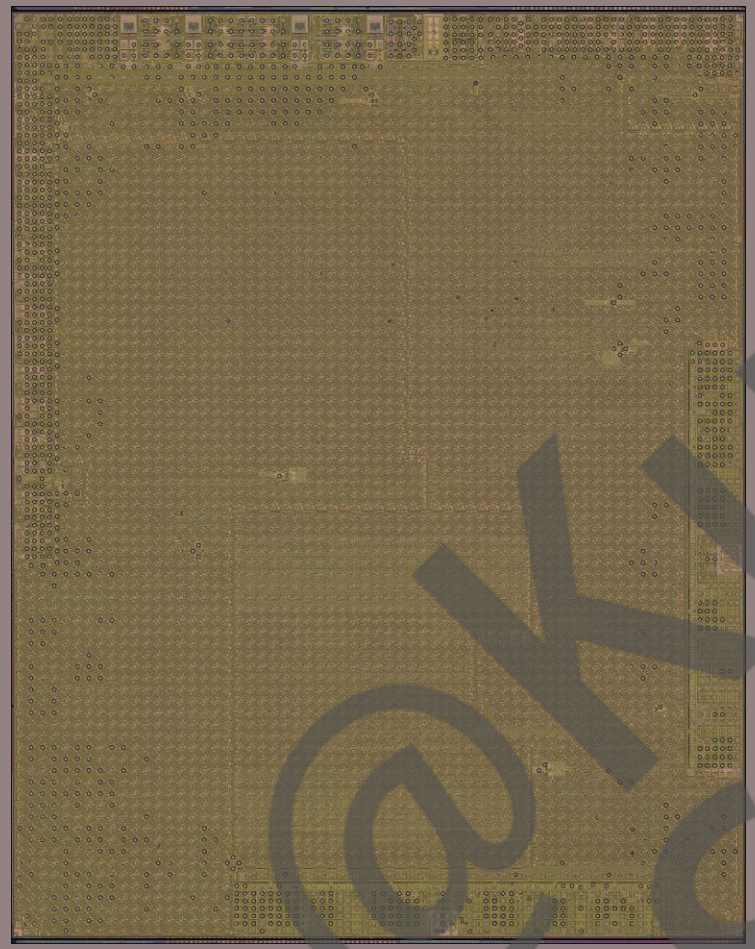
GA107 GPU Diemark

Chip code: GA107-A01
Freeze date : Nvidia M 2020 C

In Nvidia A2 GPU
Release date: 2021/11/10

1years later

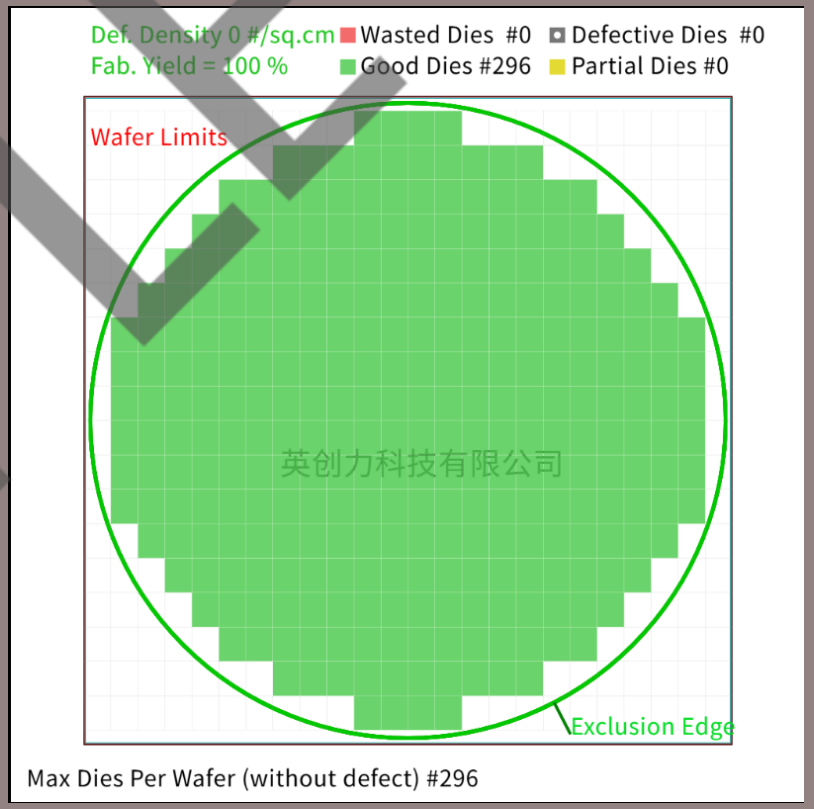
Die analyze



Diesize: 207.35mm2

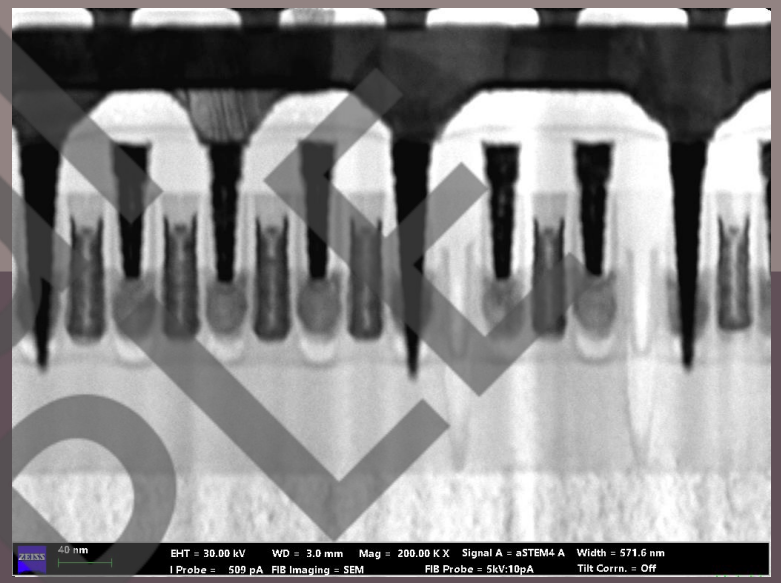
(12.76mm x 16.25mm)

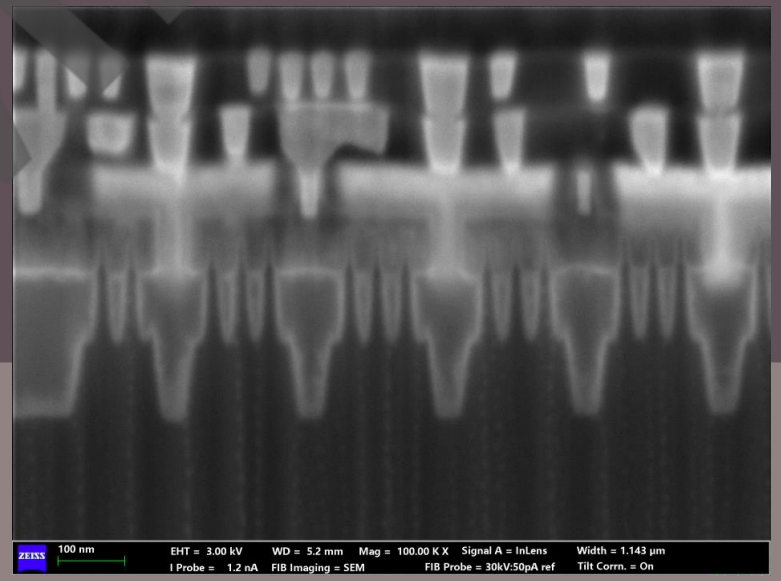
DPW Nb: 296



Switch2 soc analyze

Process analysis





How to know the Process for Switch2 T239?

We need to do Process analyze

Samsung ?nm: NDS Nvidia T239

Samsung 8nm: Nvidia GA107

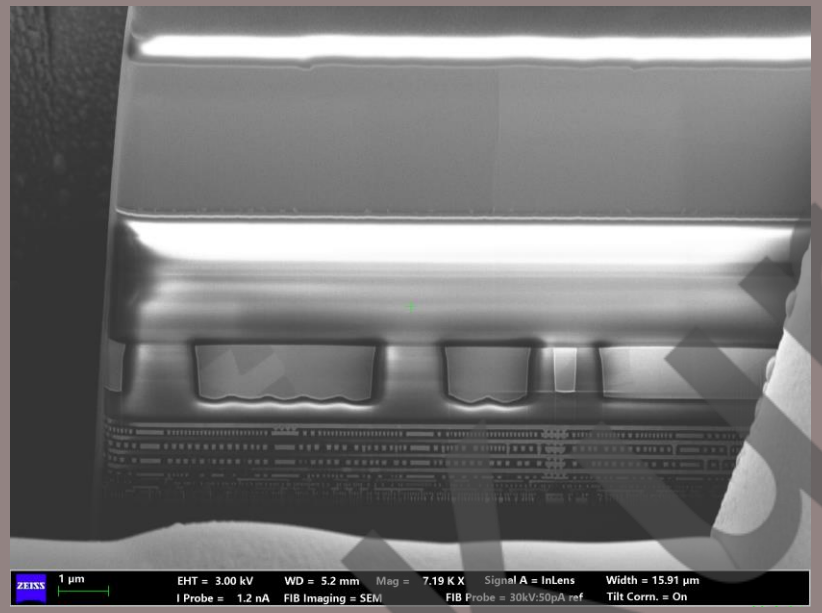
Samsung 5nm: Qualcomm SM8350(Snapdragon 888) (making)

Switch2 soc analyze

Process analyze-Nvidia T239

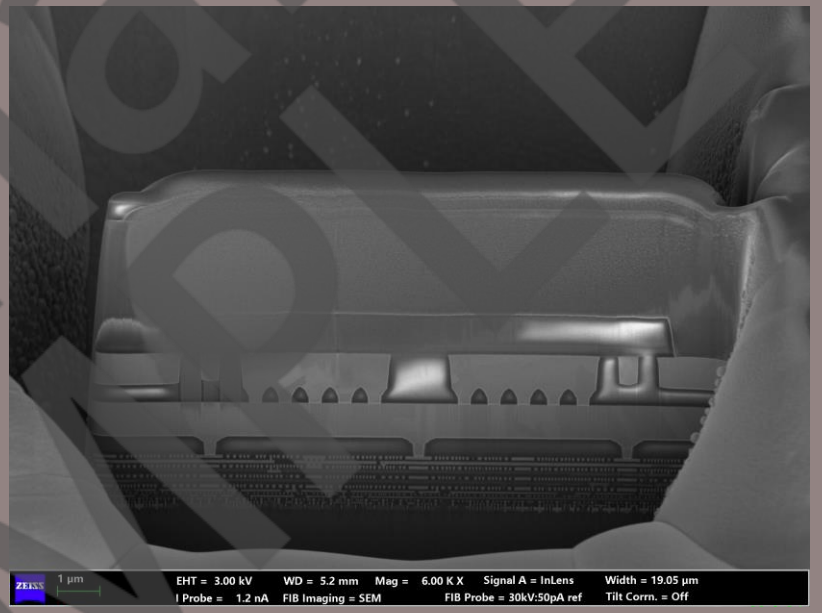
Process analyze-Nvidia T239

Process analyze-Nvidia T239



Data from (T239 1-04)

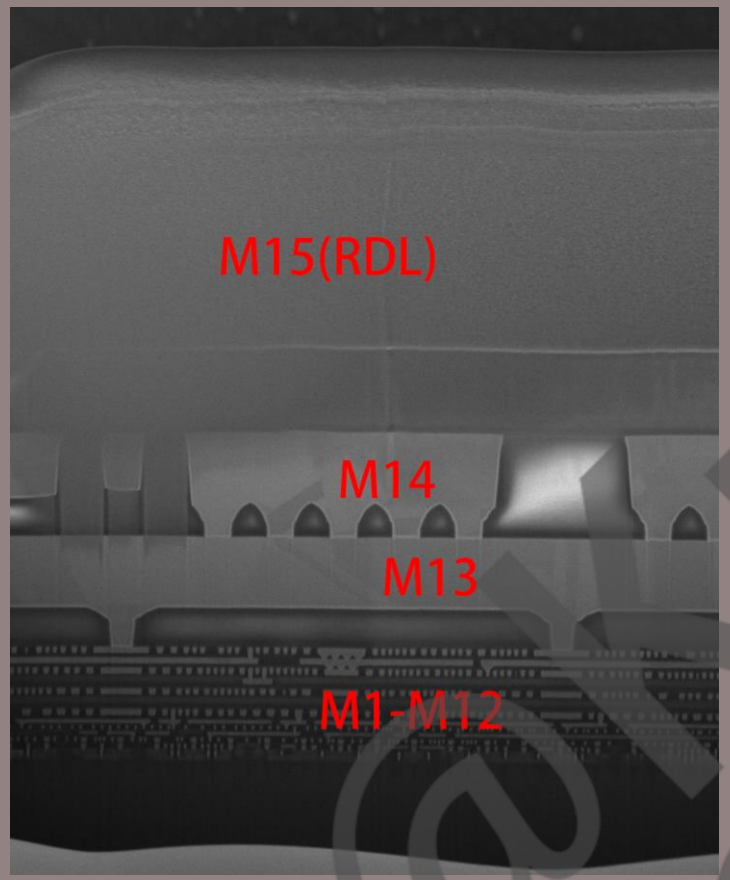
X-Cut(1)



Data from(T239 2-02)

Y-Cut(2)

Process analyze-Nvidia T239

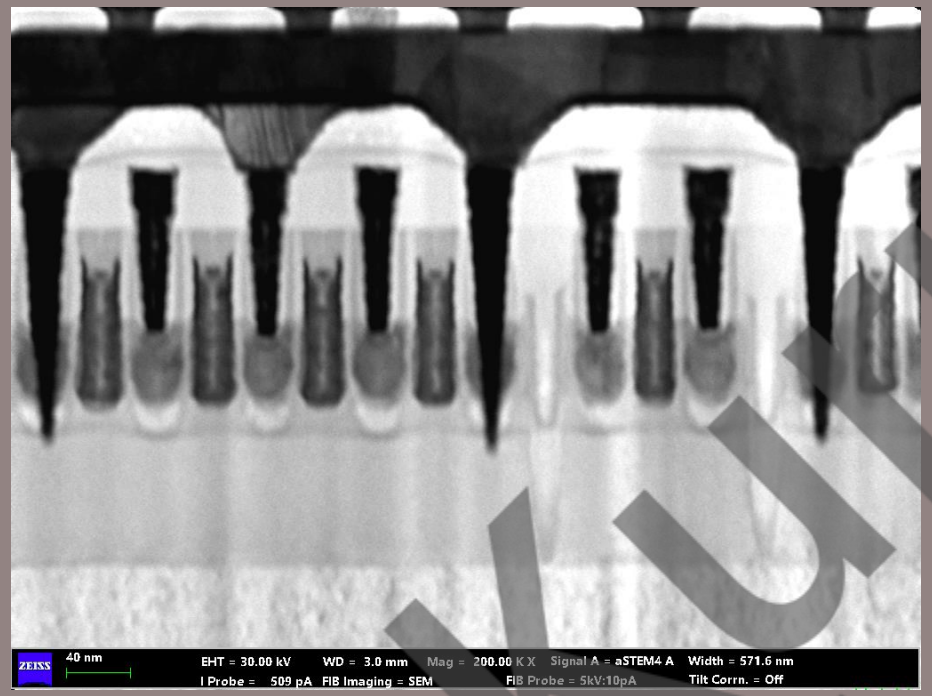


Data from(T239 2-02)

Data from(T239 2-03)

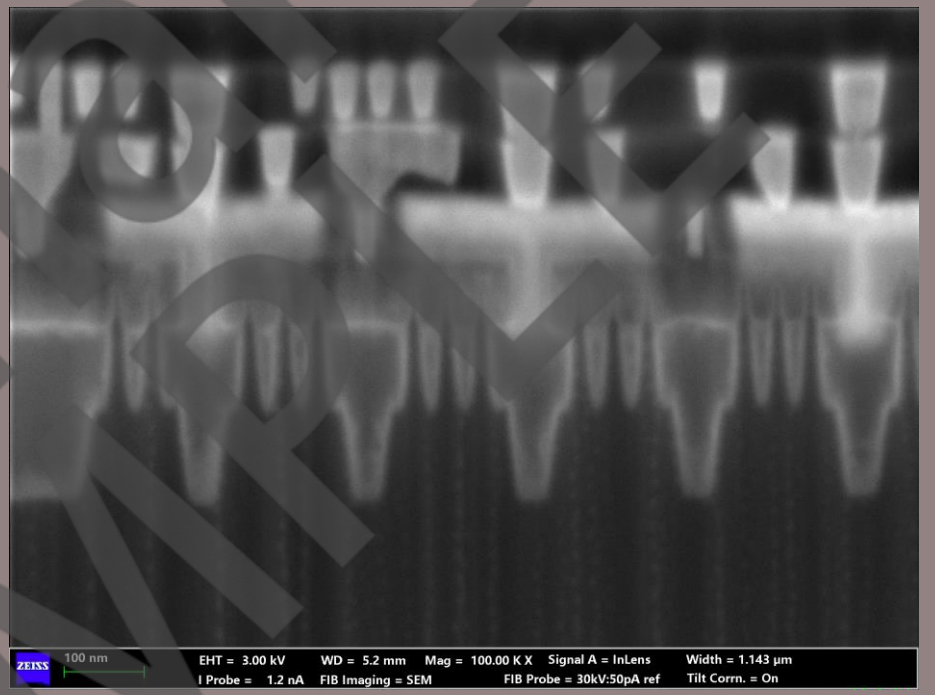
In the Nvidia T239
Total have 1P 15Metal (14Metal+1RDL)

Process analyze-Nvidia T239



Data from(T239 1-16)

X-Cut(1) Gate cut



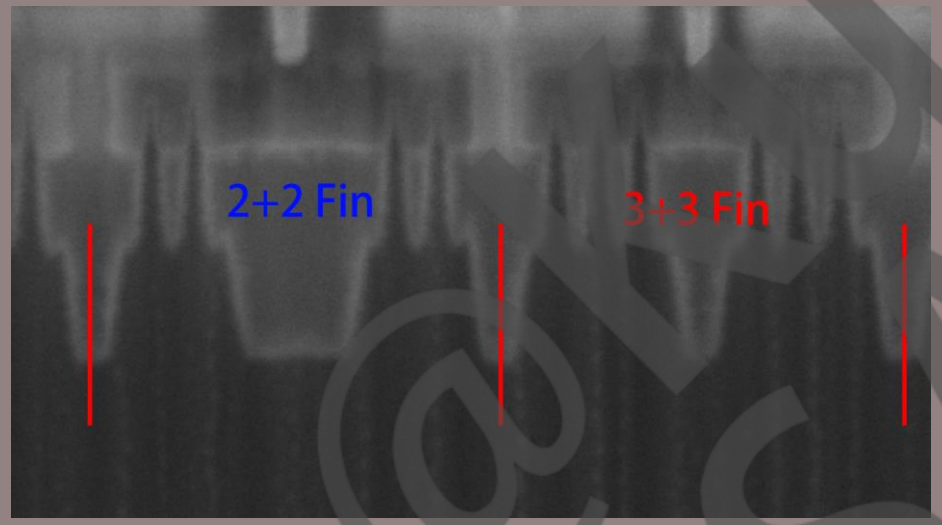
Data from(T239 2-07)

Y-Cut(2) Fin cut

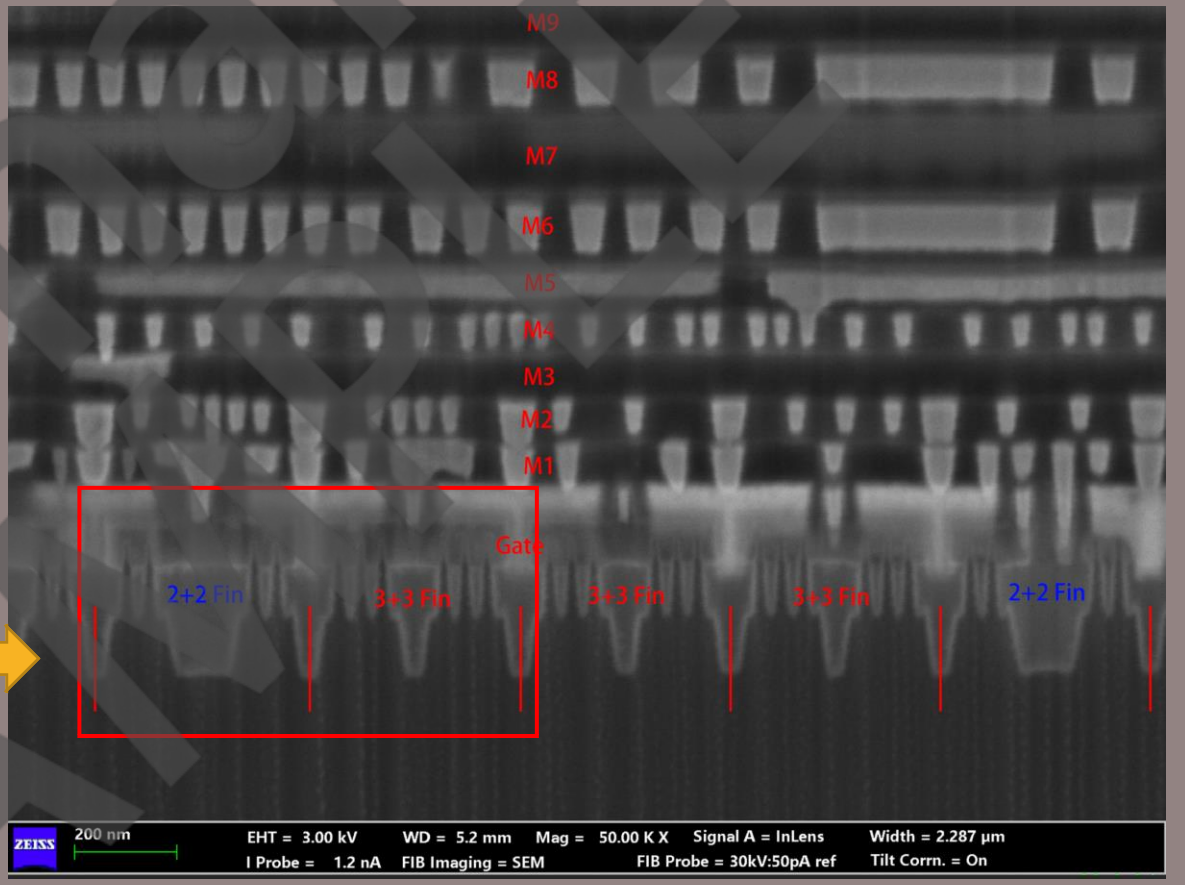
Analyze Fincut First

Process analyze-Nvidia T239-Fin cut

In the T239 GPU area
There are 2 type of Fin number
2+2 Fin and 3+3 Fin

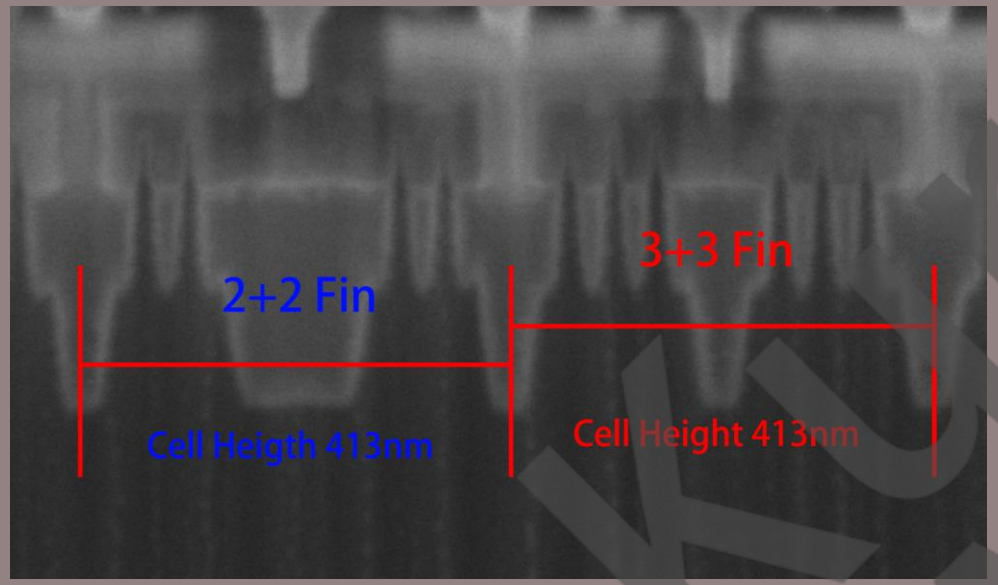


Data From (T239 2-06)



Data From (T239 2-06)

Process analyze-Nvidia T239-Fin cut



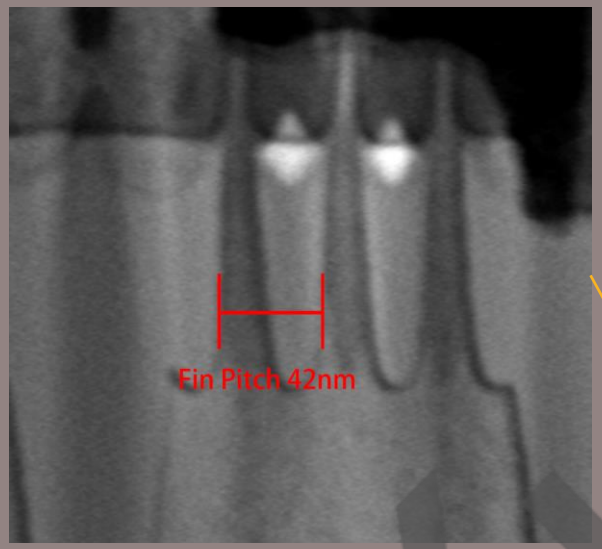
Data From (T239 2-06)

In the Nvidia Switch2 T239

Both 3+3 and 2+2 cells share the same cell height

Process analyze-Nvidia T239-Fin cut

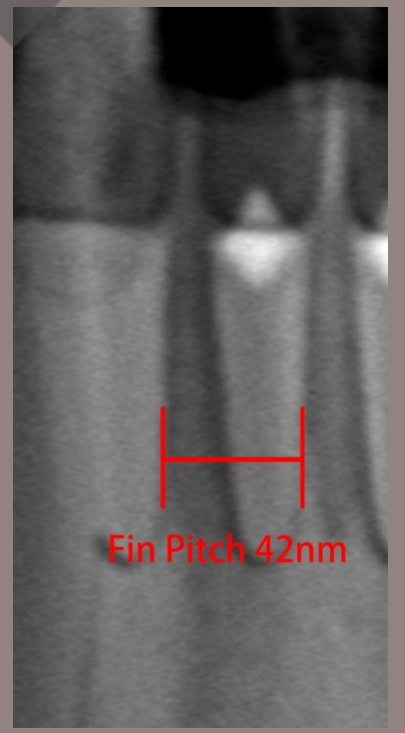
3+3 Fin



2+2 Fin

In the Nvidia T239

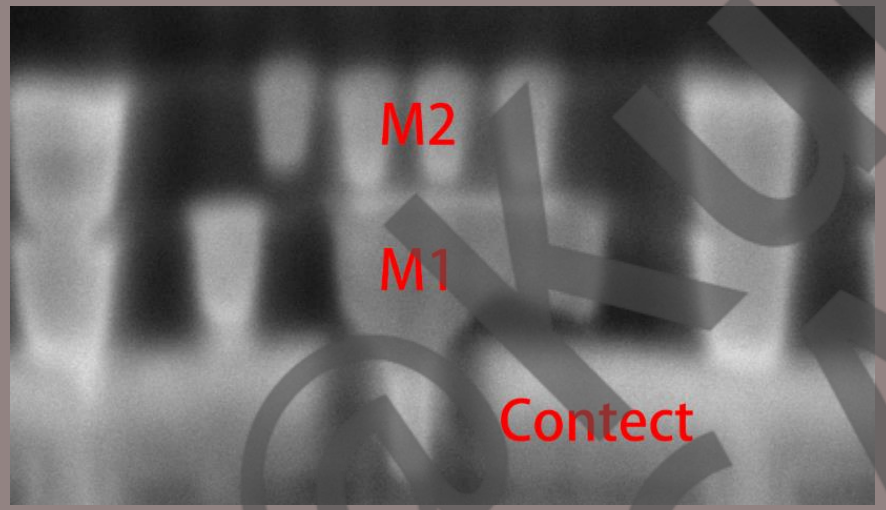
This 2 libs Fin Pitch both 42nm

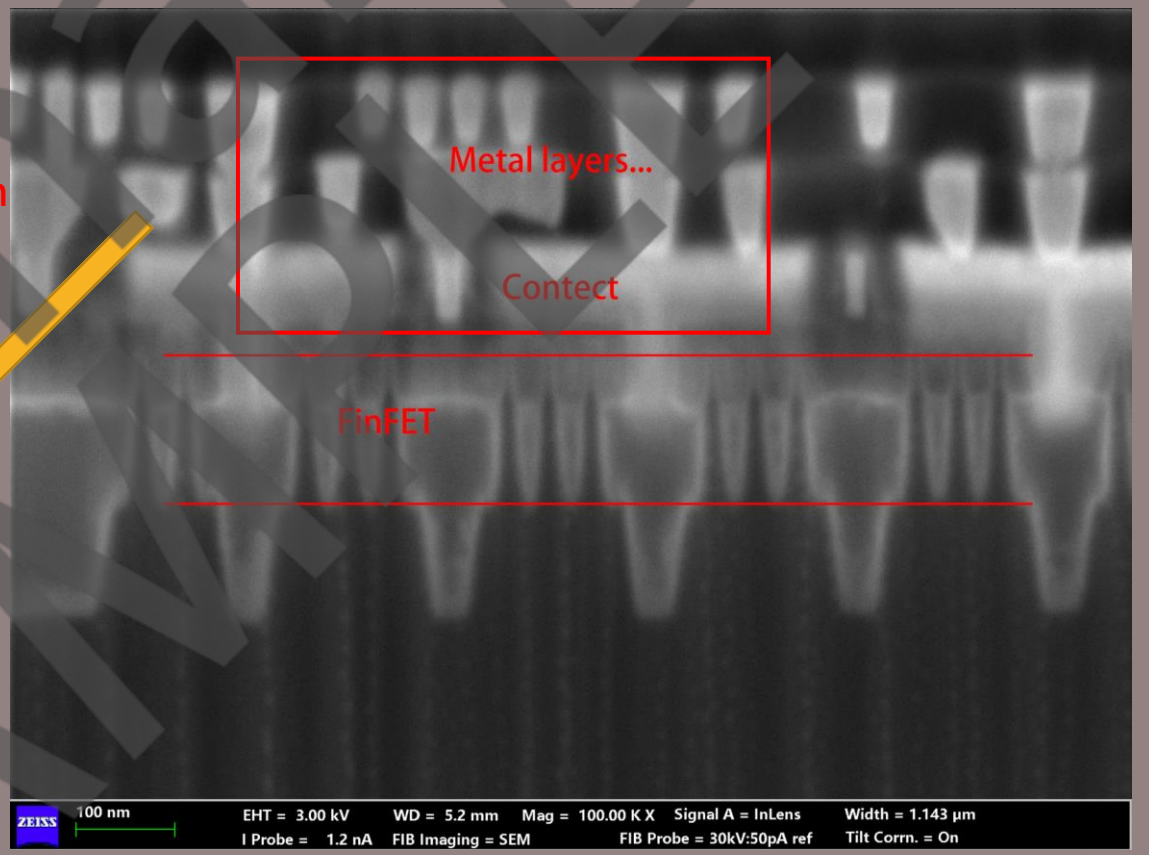


Data From (T239 2-10)

Process analyze-Nvidia T239-Metal

On the top of the Fin, there are Metal layers
We need to know the minimum metal pitch,and metal 2 pitch

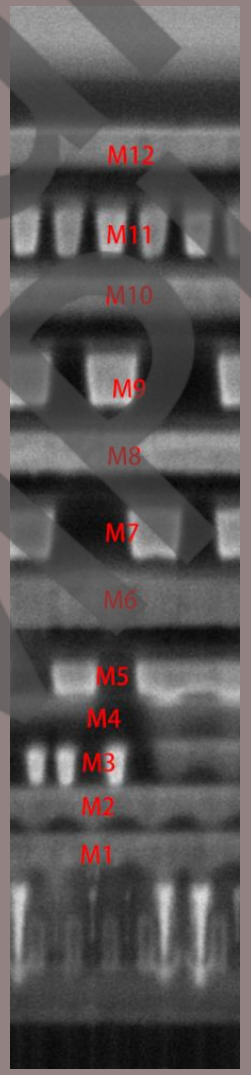




Data From (T239 2-07)

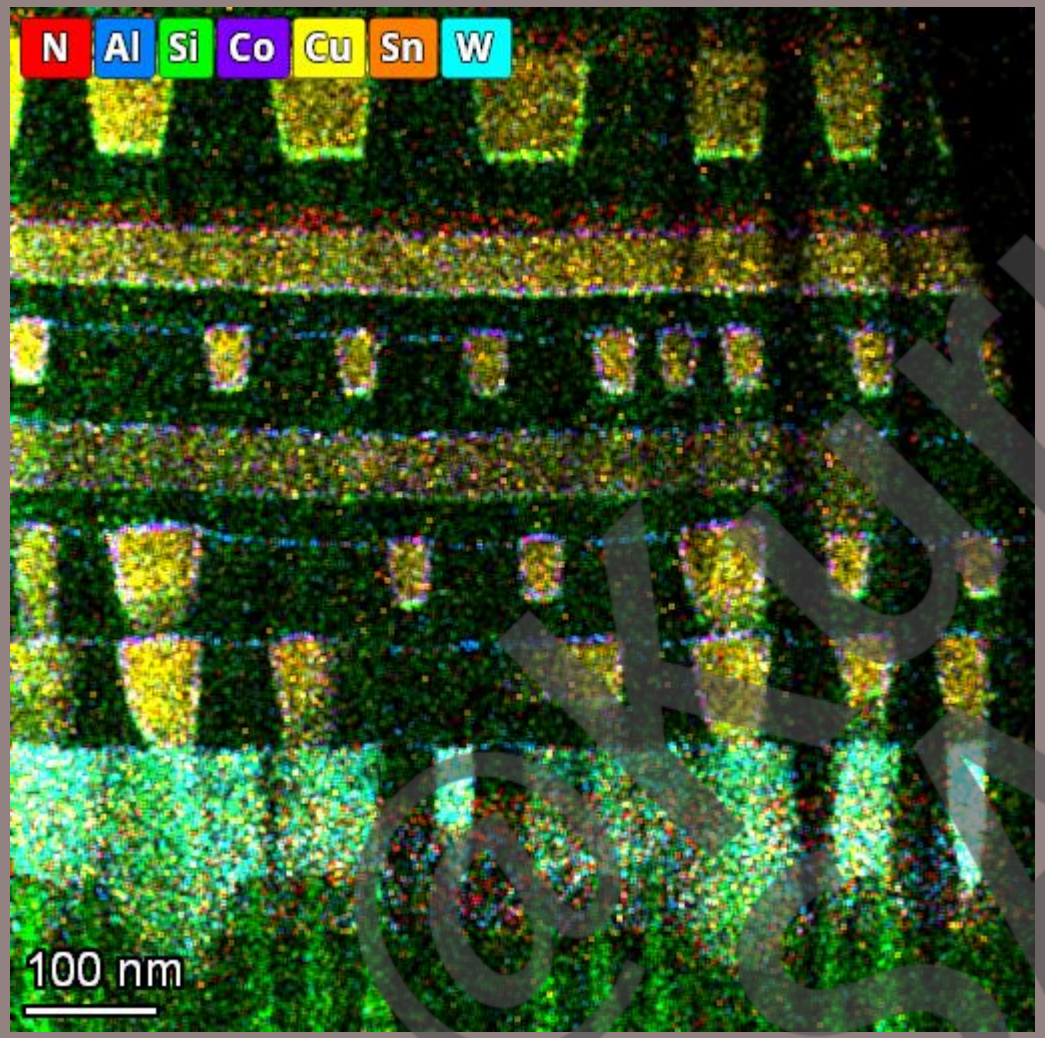
Process analyze-Nvidia T239-Metal

	Pitch	MMP	Element	Isolation(down)
M1	68nm	Gate Pitch	eCu	Aluminium?
M2	48nm	1x	eCu	Aluminium?
M3	48nm	1x	eCu	Aluminium?
M4	48nm	1x	eCu	Aluminium?
M5	80nm	1.66x	eCu	Aluminium?
M6	80nm	1.66x	Cu	Nitride
M7	80nm	1.66x	Cu	Nitride
M8	80nm	1.66x	Cu	Nitride
M9	80nm	1.66x	Cu	Nitride
M10	80nm	1.66x	Cu	Nitride
M11	80nm	1.66x	Cu	Nitride
M12	80nm	1.66x	Cu	Nitride

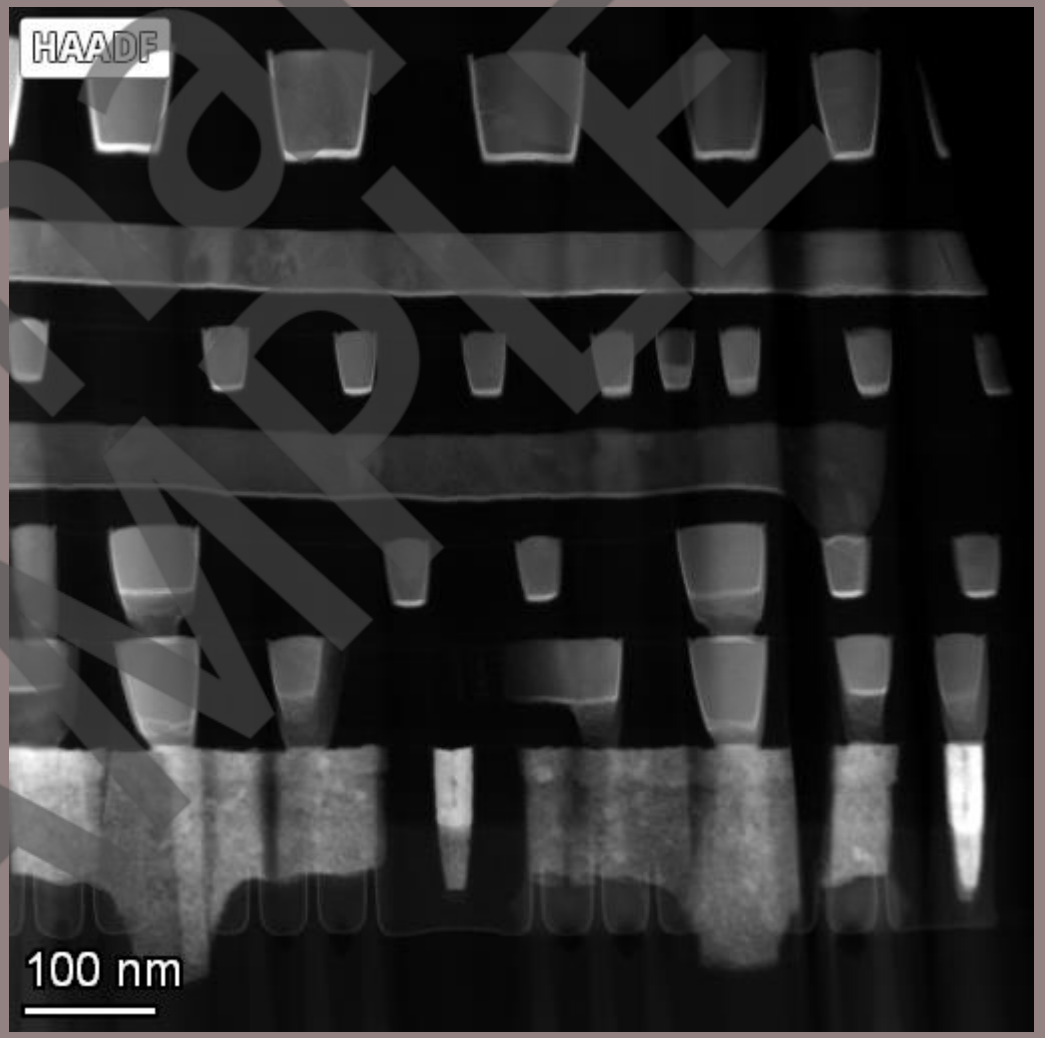


Data From (T239 1-07)

Process analyze-Nvidia T239-Fin cut-EDS

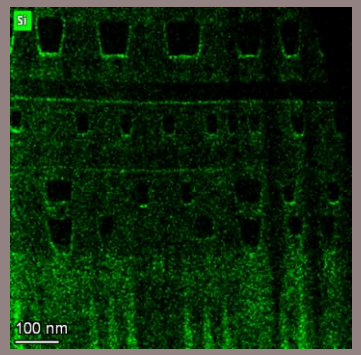


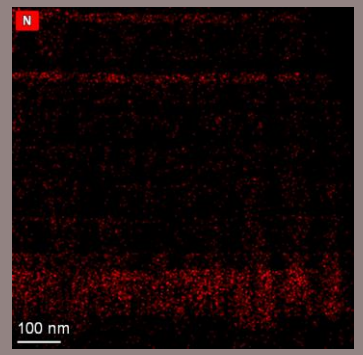
Data From (T239 EDS Y 1LA 1040 SI 130 kx ColorMix-net)

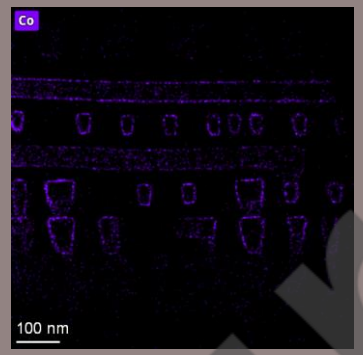


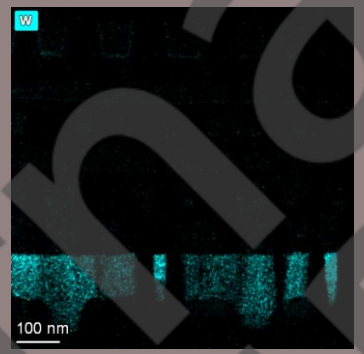
Data From (T239 EDS Y 1LA 1040 SI 130 kx HAADF)

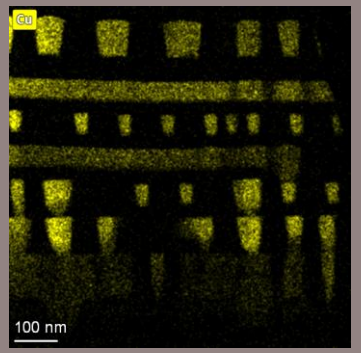
Process analyze-Nvidia T239-Fin cut-EDS

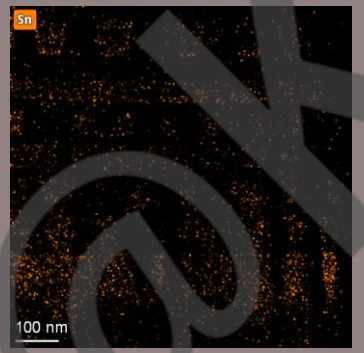


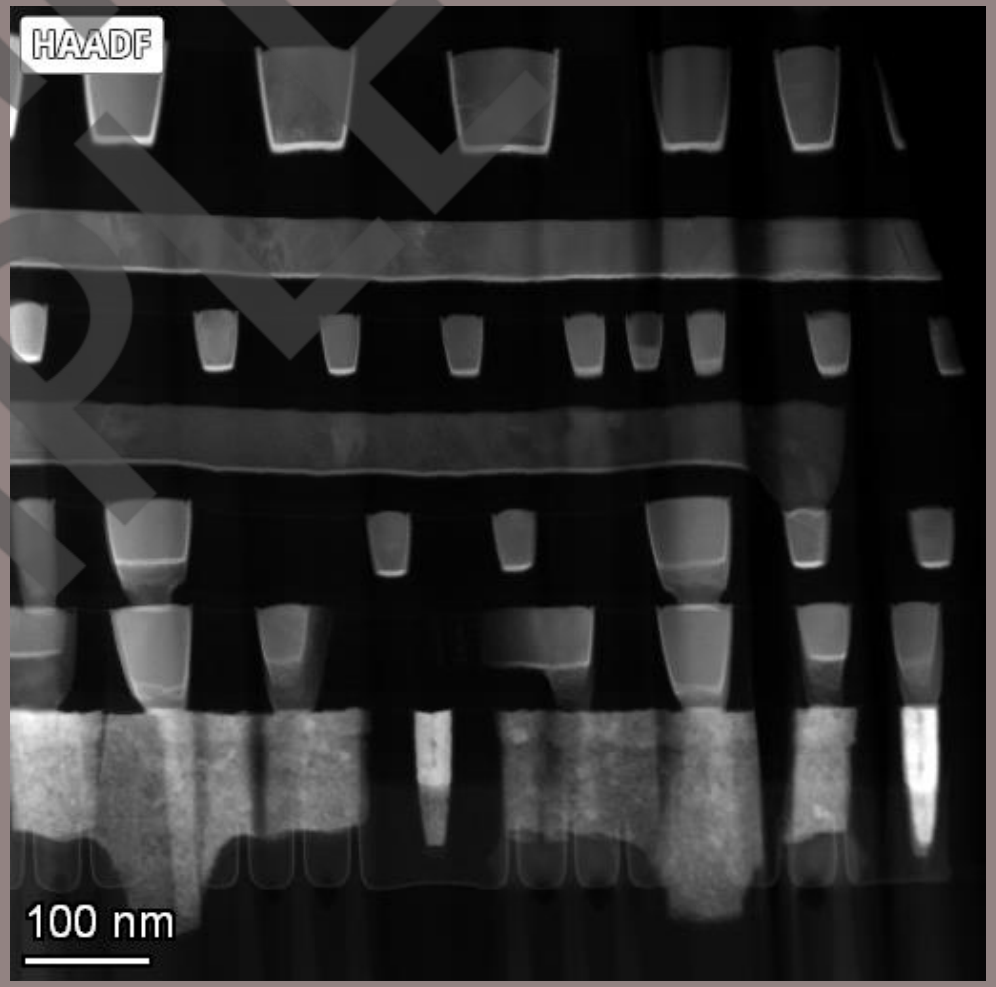






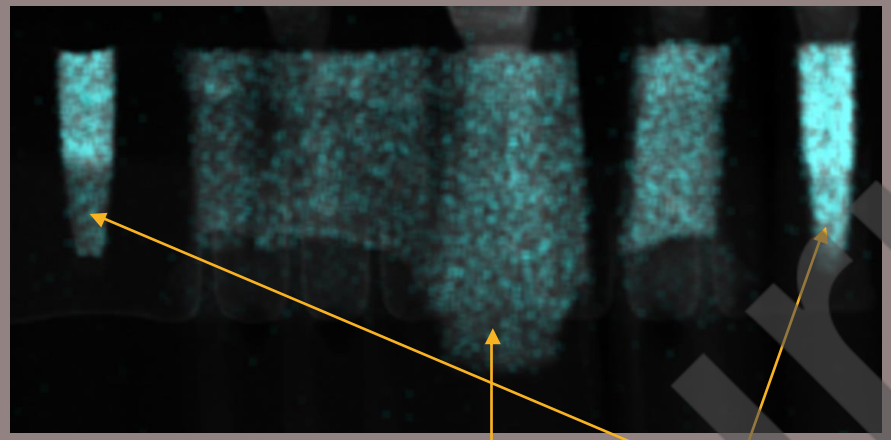




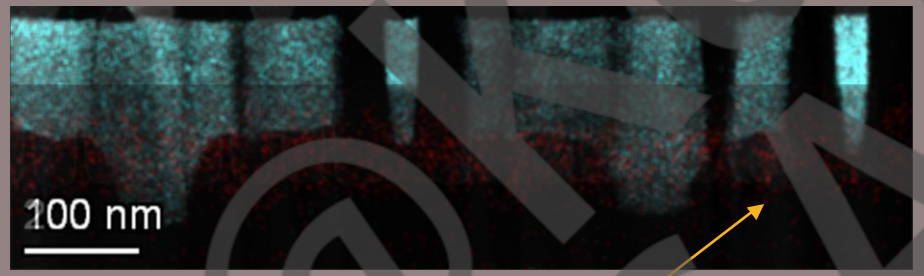


Data From (T239 EDS Y 1LA 1040 SI 130 kx HAADF)

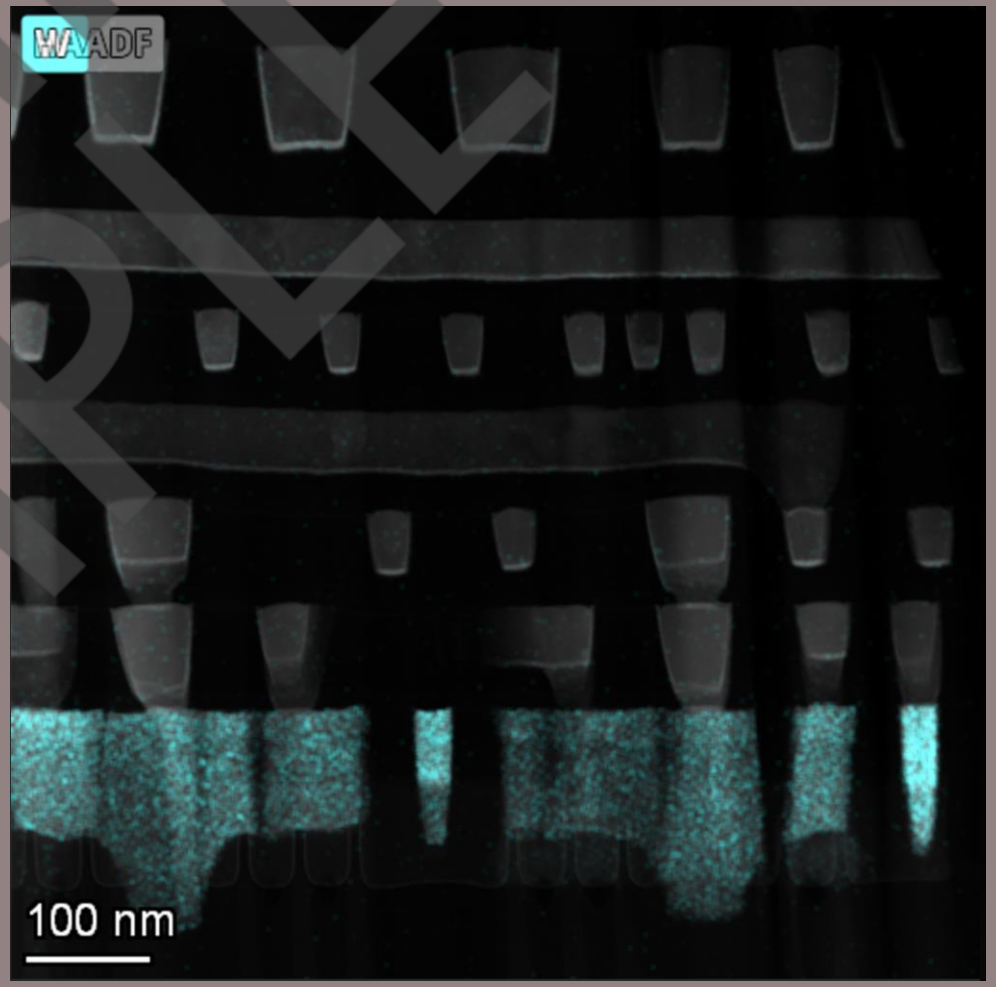
Process analyze-Nvidia T239-Fin cut-EDS



Used the W for Gate and contact plug

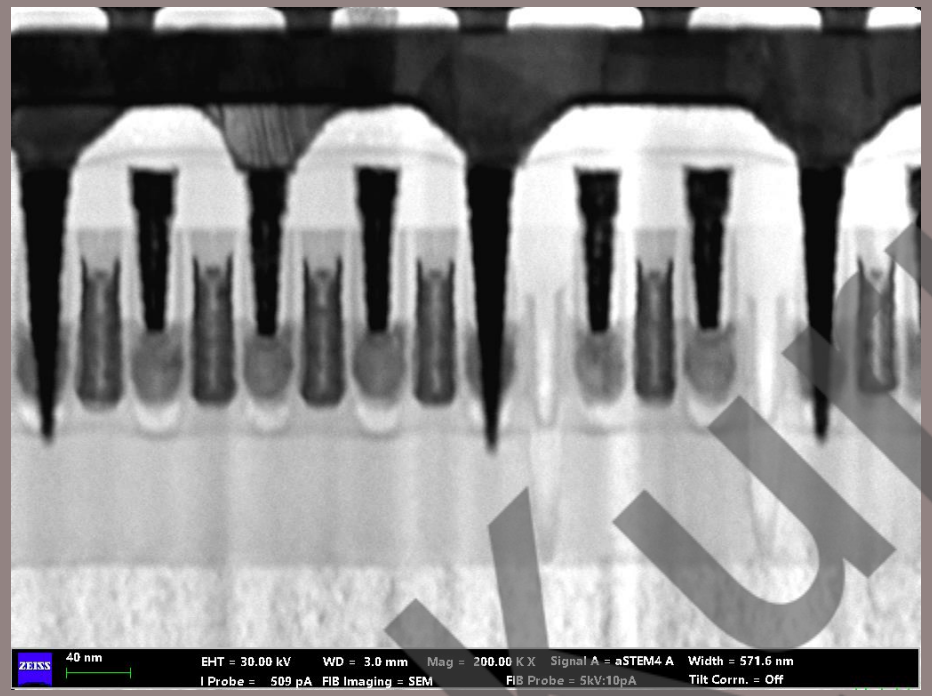


Used the N for Fin isolation

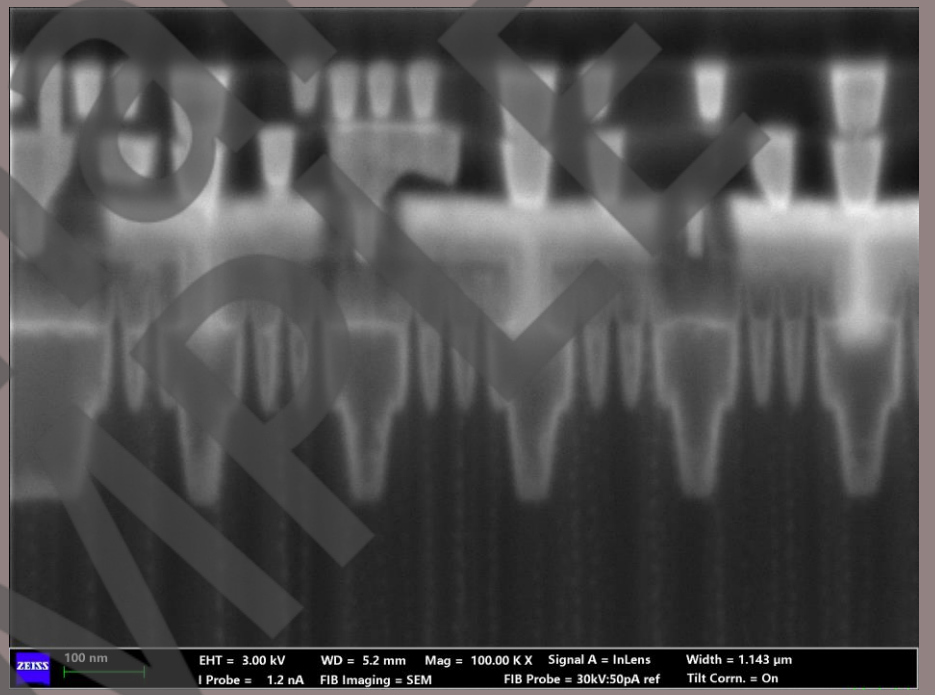


Data From (T239 EDS Y 1LA 1040 SI 130 kx HAADF)

Process analyze-Nvidia T239-Gate cut



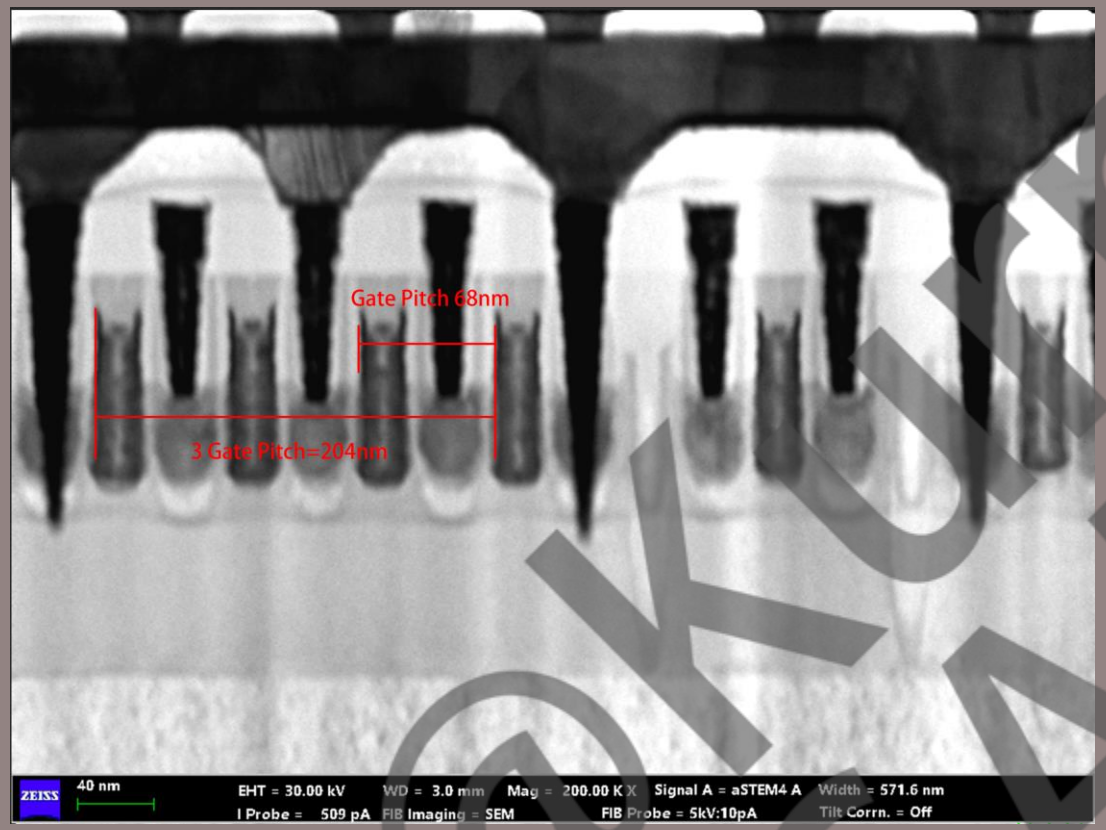
X-Cut(1) Gate cut



Y-Cut(2) Fin cut

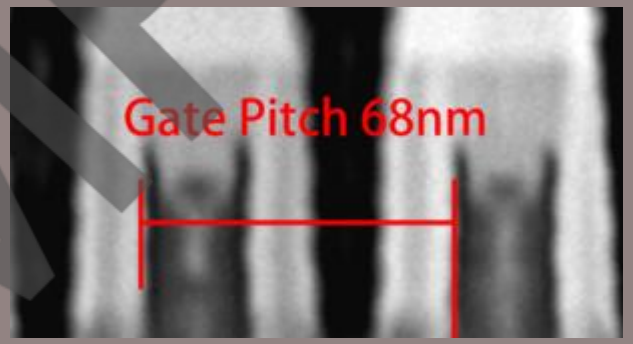
Analyze Gate cut

Process analyze-Nvidia T239-Gate cut

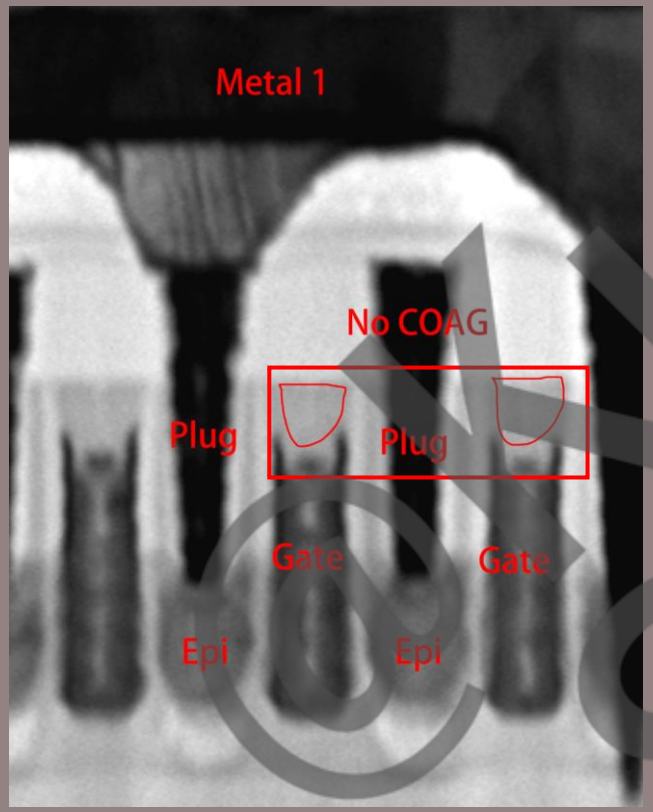


Data From (T239 1-16)

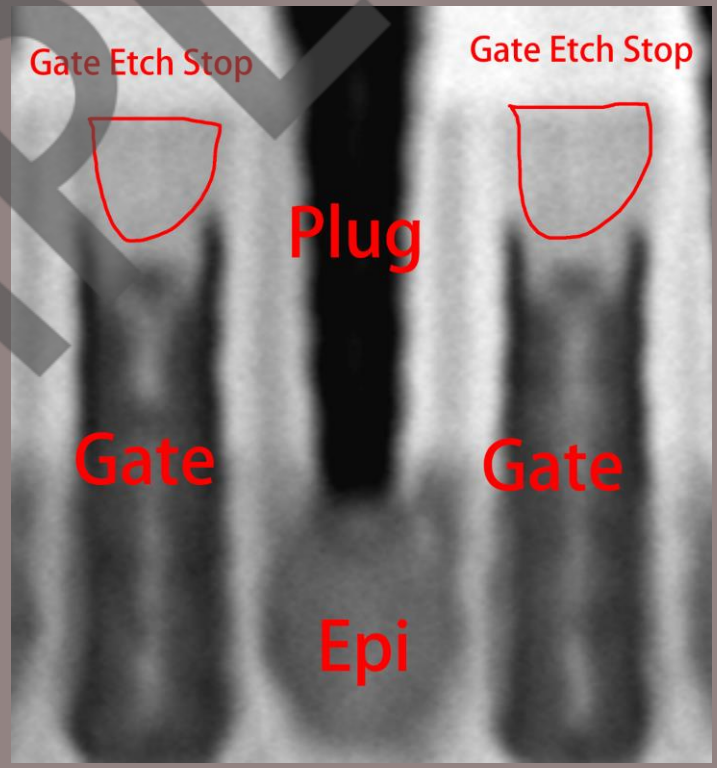
The Gate Pitch= 68nm



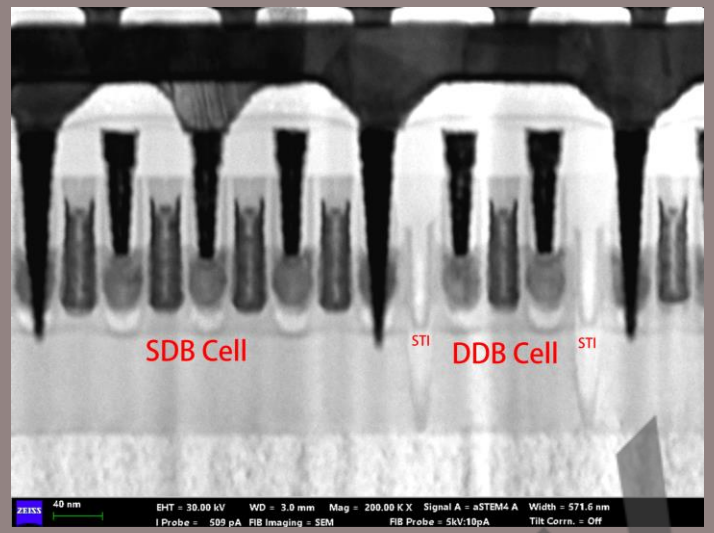
No COAG（contact Over Active Gate）



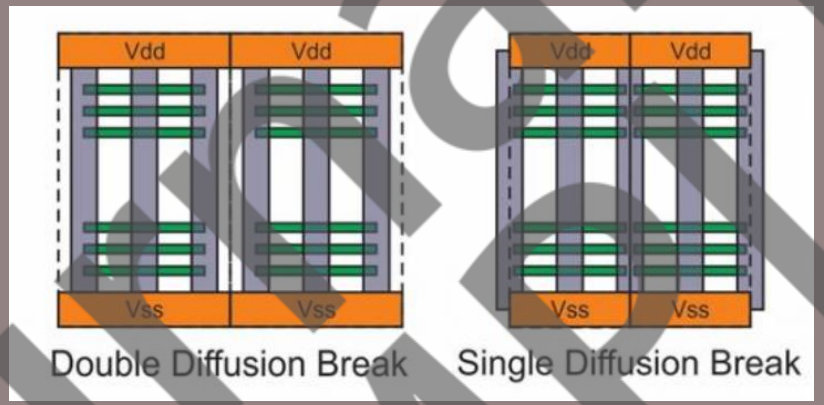
Use Self-Aligned-contact



Process analyze-Nvidia T239-Gate cut

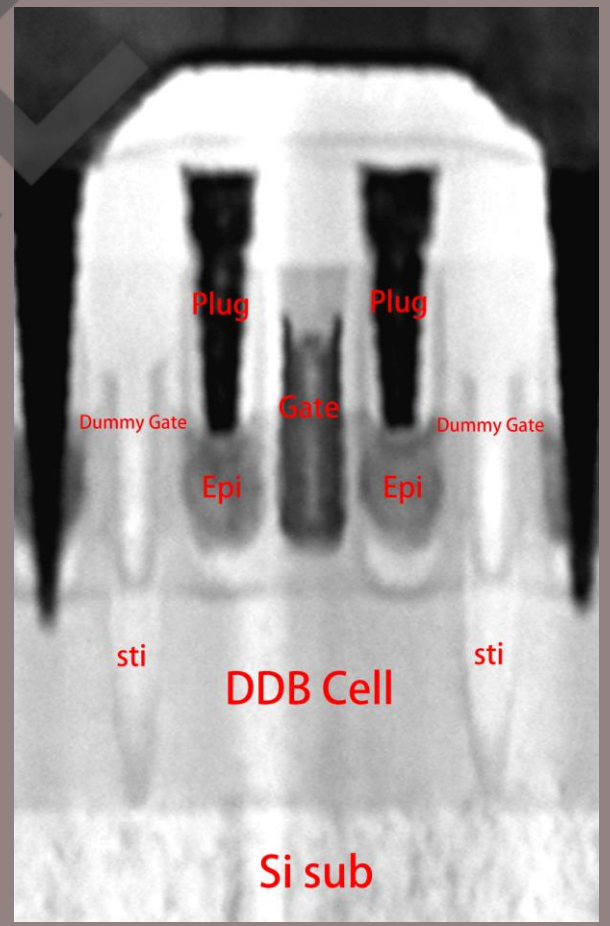


Data From (T239 1-16)

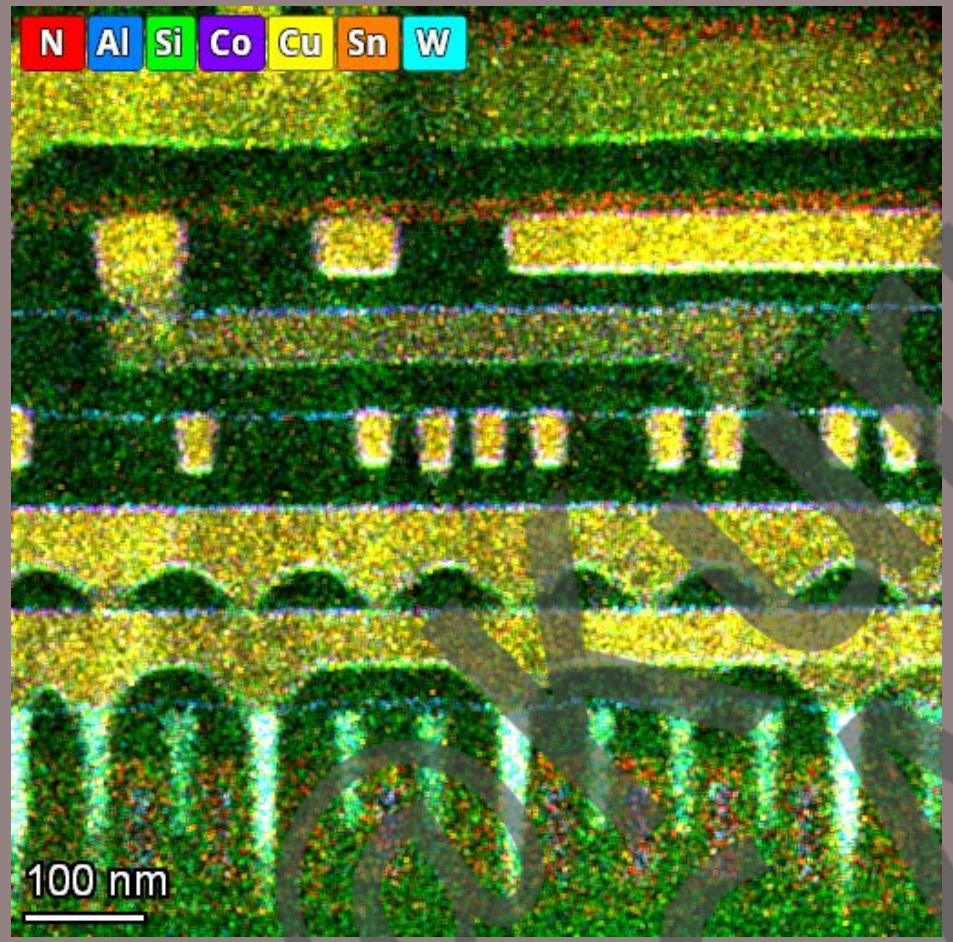


This Process uses MDB(Mixed Diffusion Break)

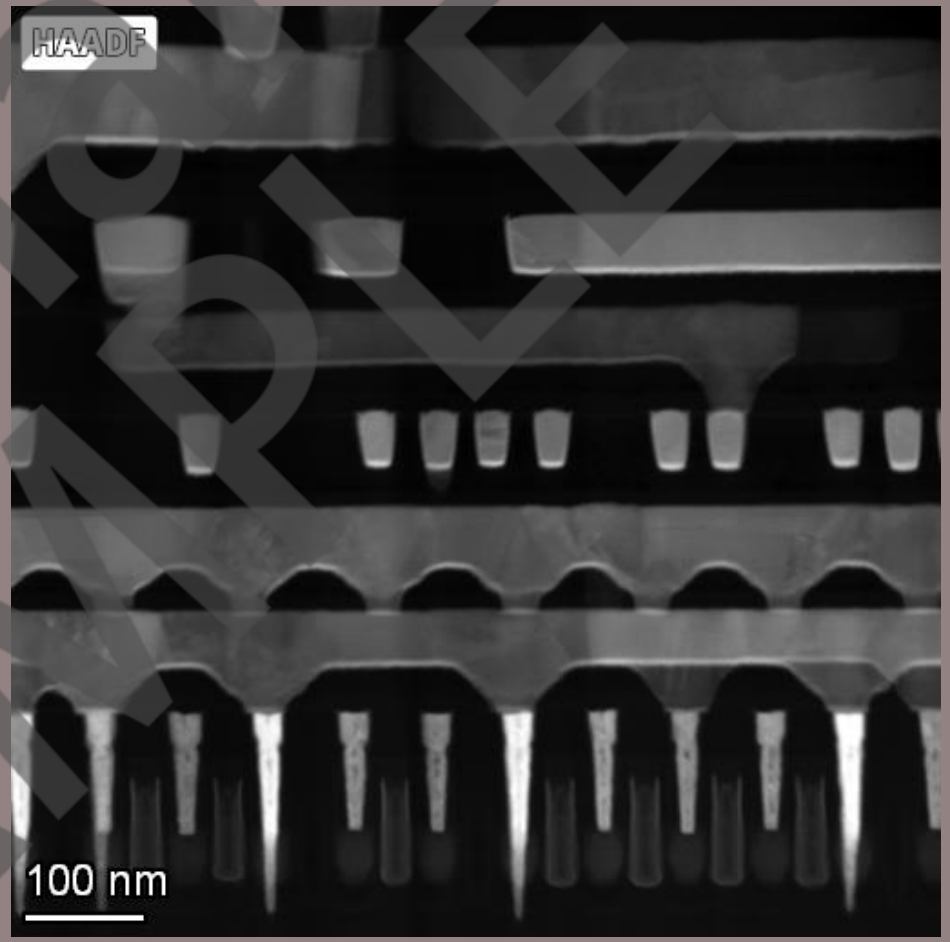
Mixed the DDB and SDB



Process analyze-Nvidia T239-Gate cut-EDS

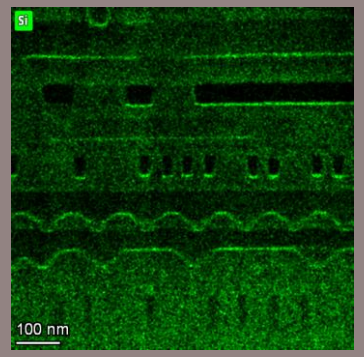


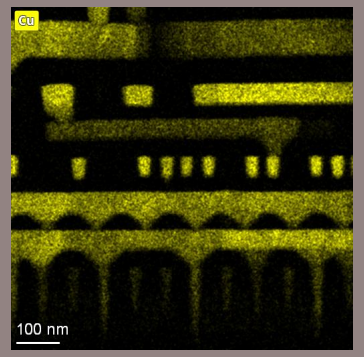
Data From (T239 EDS X 1LA 1008 SI 130 kx ColorMix-net)

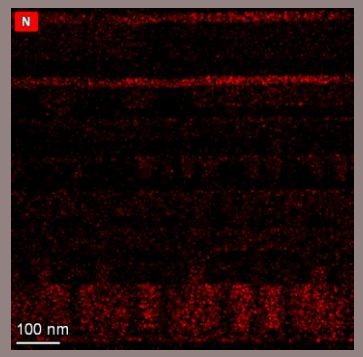


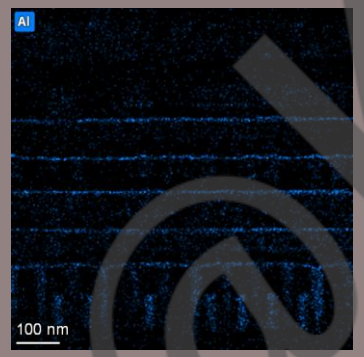
Data From (T239 EDS X 1LA 1008 SI 130 kx HAADF)

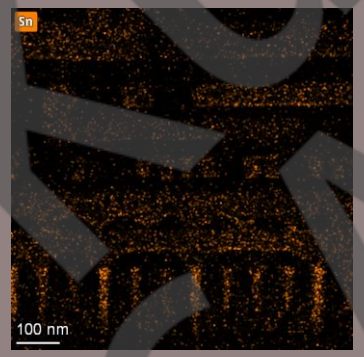
Process analyze-Nvidia T239-Gate cut-EDS

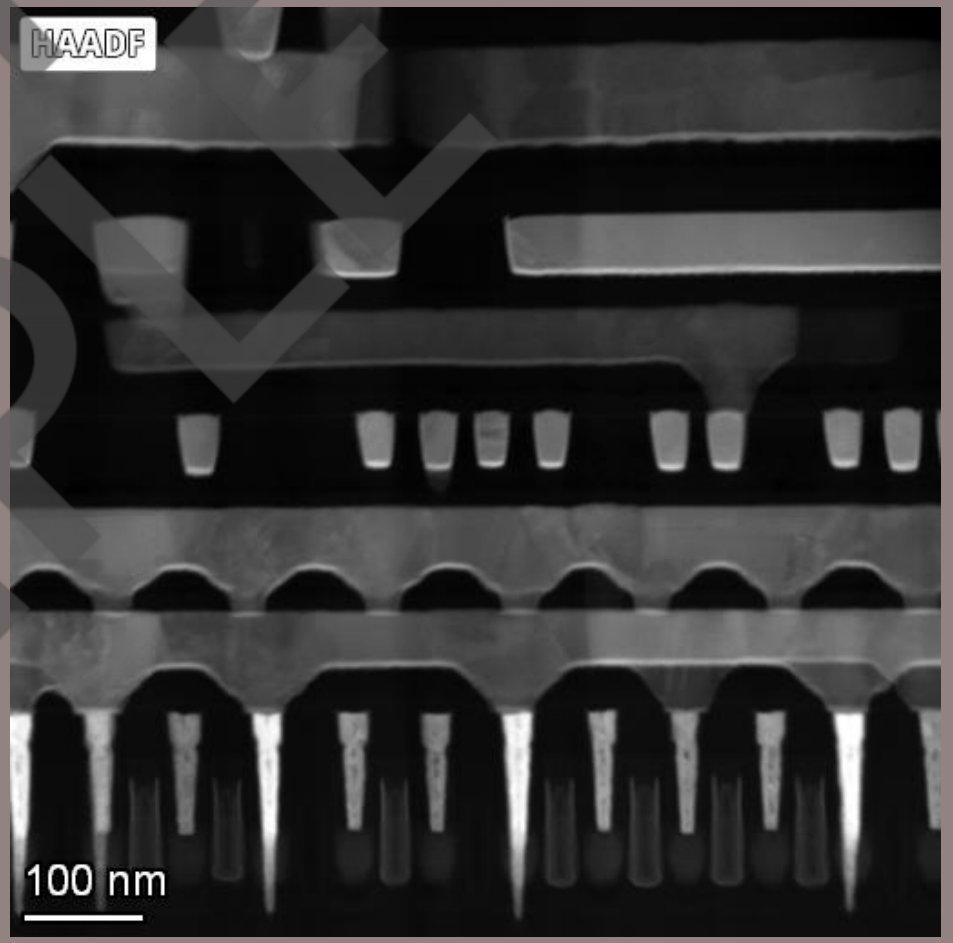








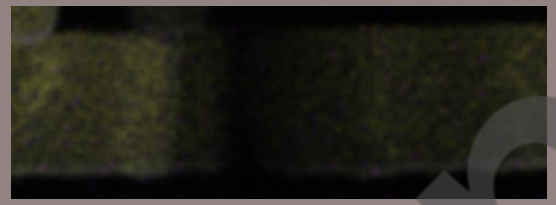




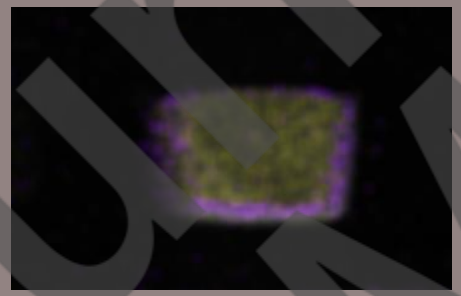
Data From (T239 EDS X 1LA 1008 SI 130 kx HAADF)

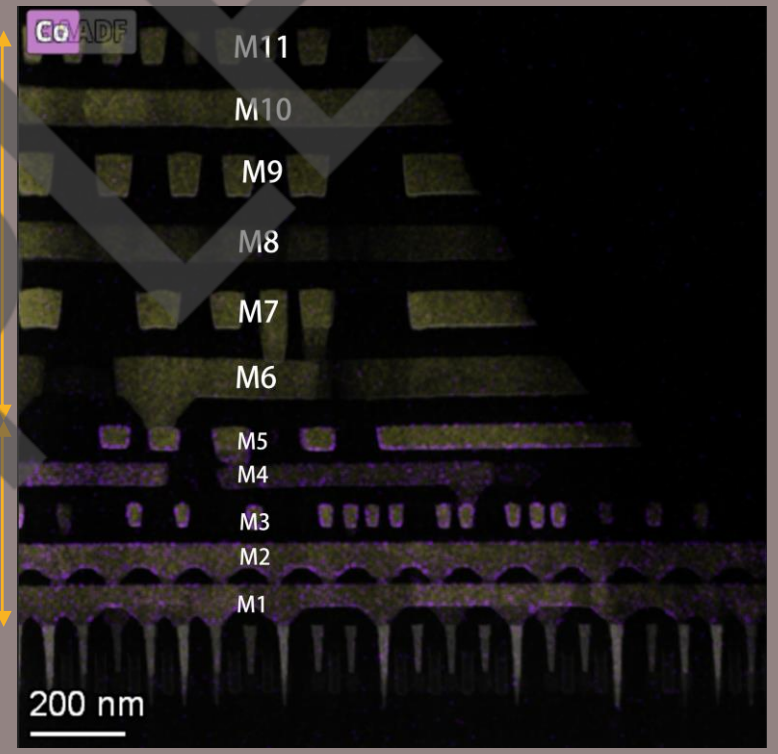
Process analyze-Nvidia T239-Gate cut-EDS

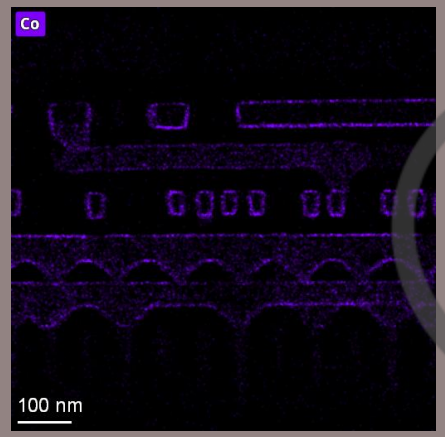
M6-M12 used the Pure Cu

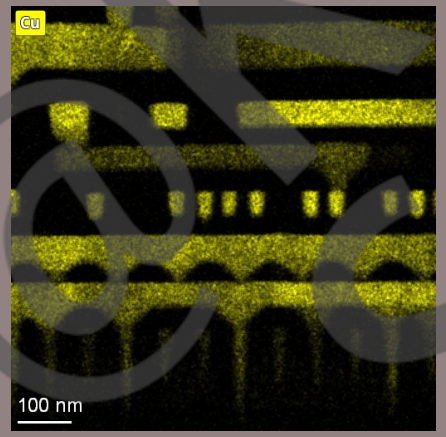


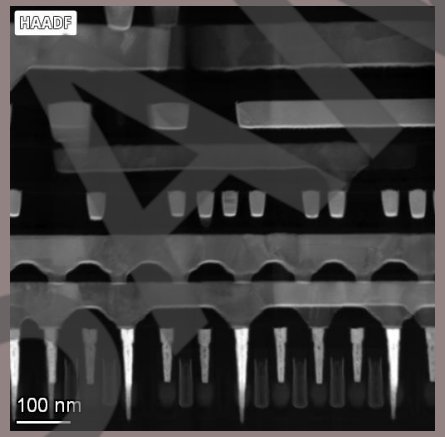
Metal1 – Metal 5 used the Enhanced Cu
Co cladding Cu





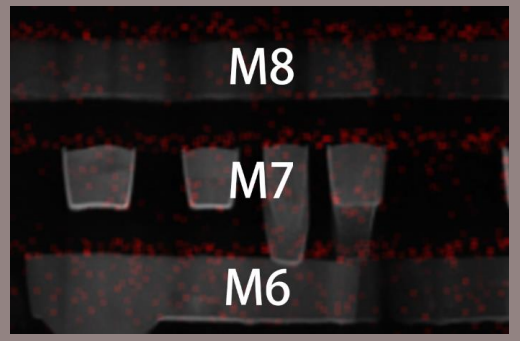


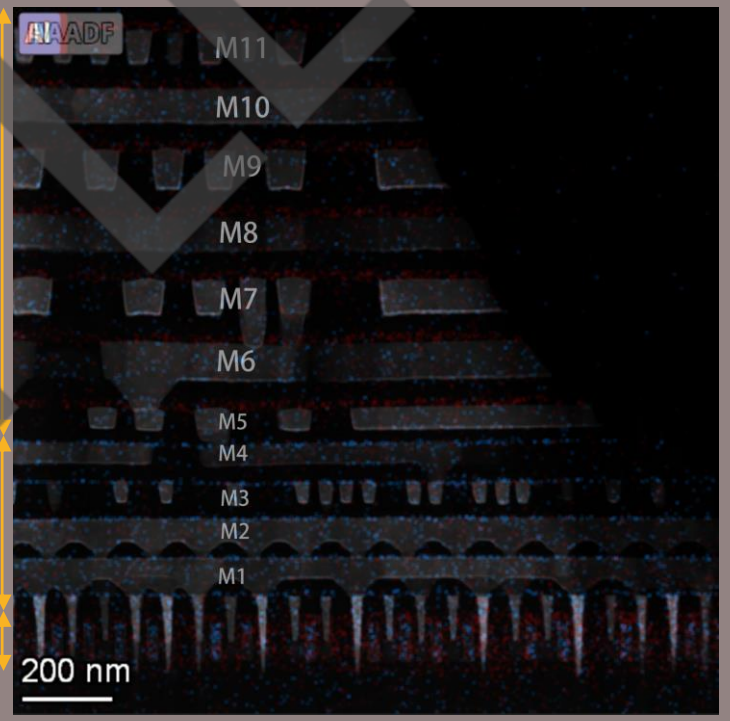




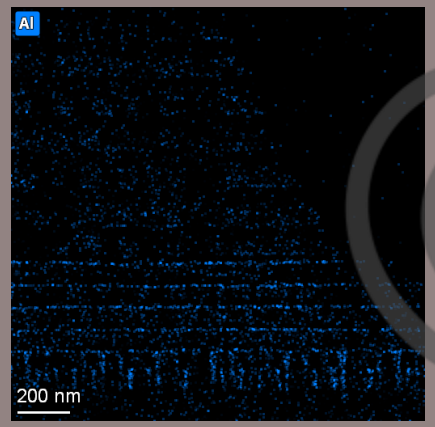
Data From (T239 EDS X 2LA 1024 SI 64000 x HAADF)

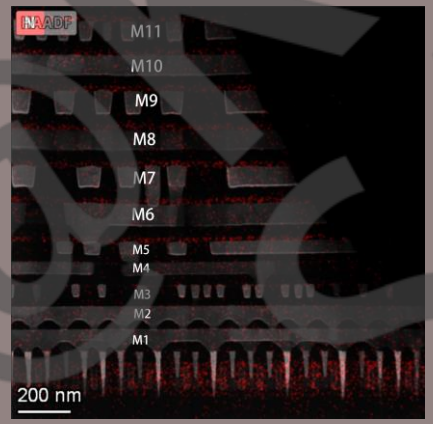
Thin film deposition used From isolation From N on the Top of M5 to M12 and Sub

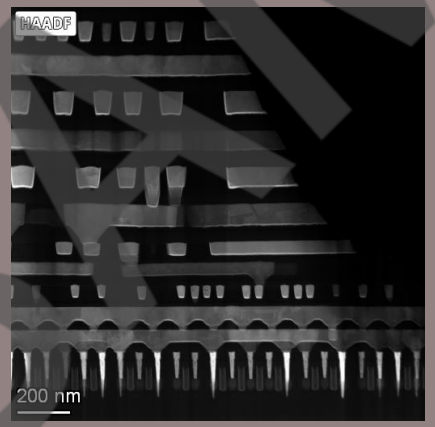




Thin film deposition used From Al on the Top of Contact to M1

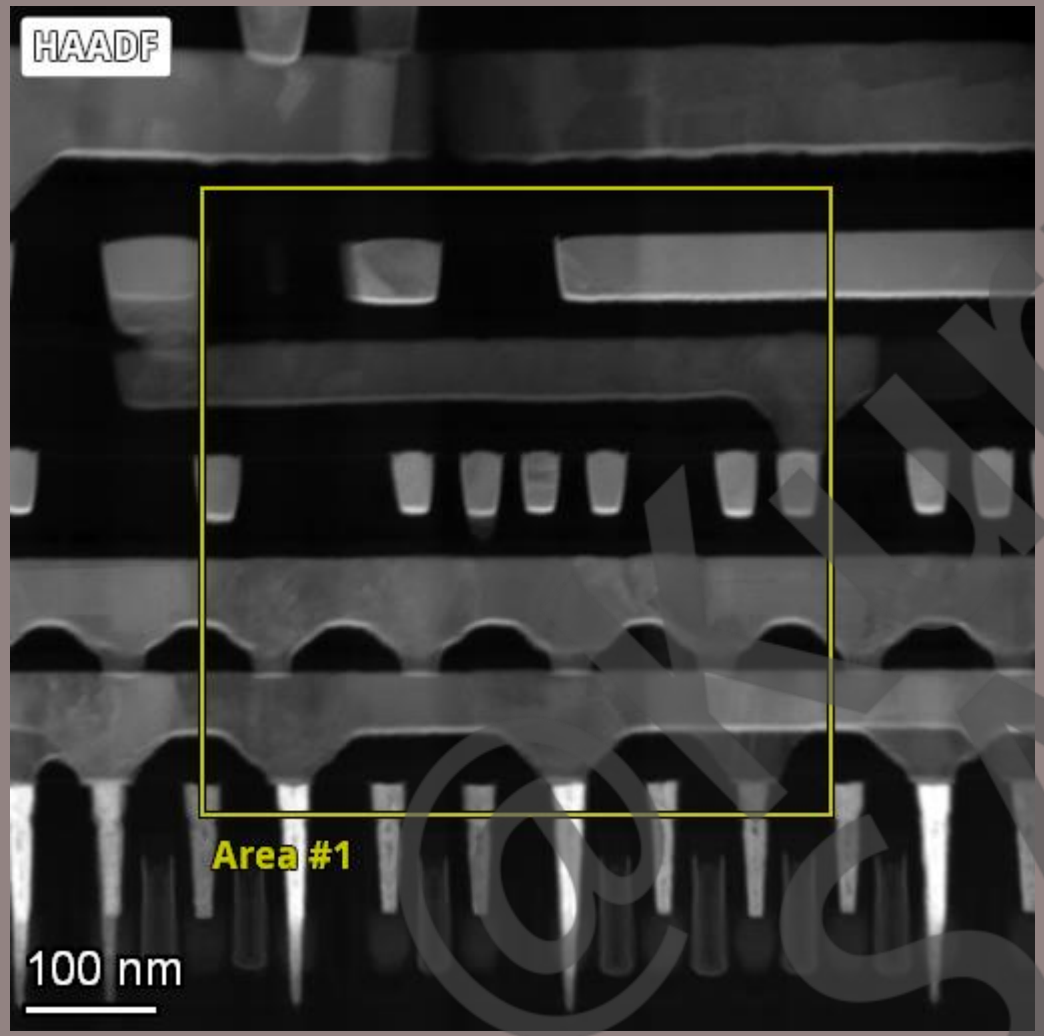




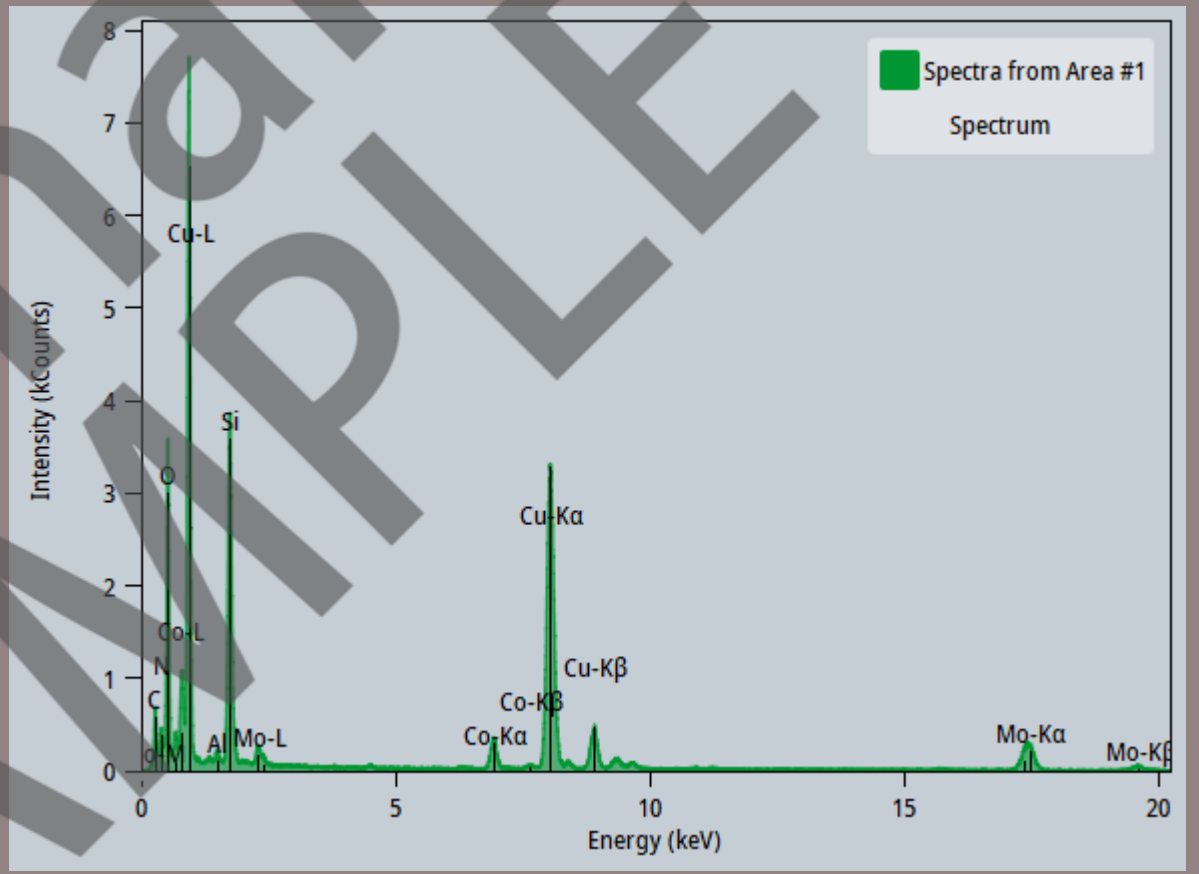


Data From (T239 EDS X 1LA 1008 SI 130 kx HAADF)

Process analyze-Nvidia T239-Gate cut-EDS

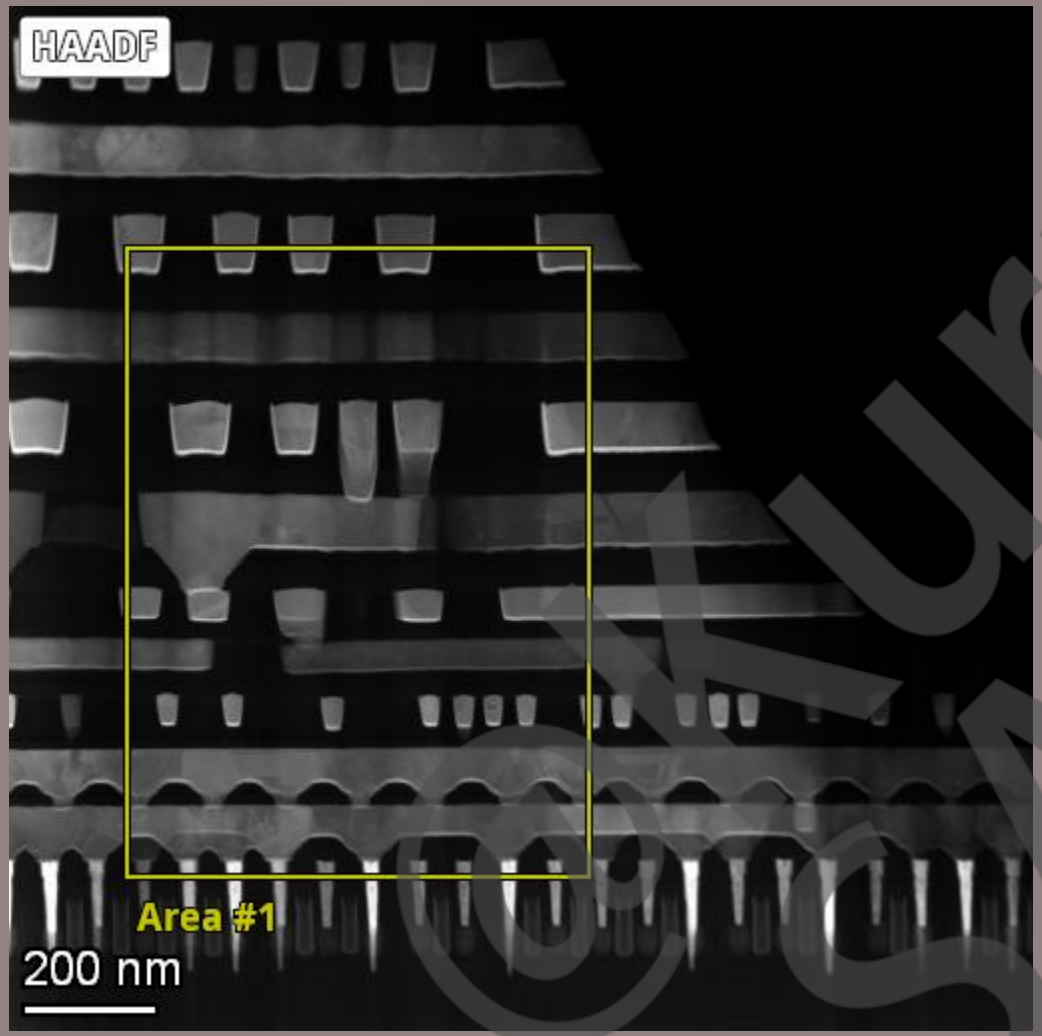


Data From (T239 EDS X 1LA 1008 SI 130 kx ColorMix)

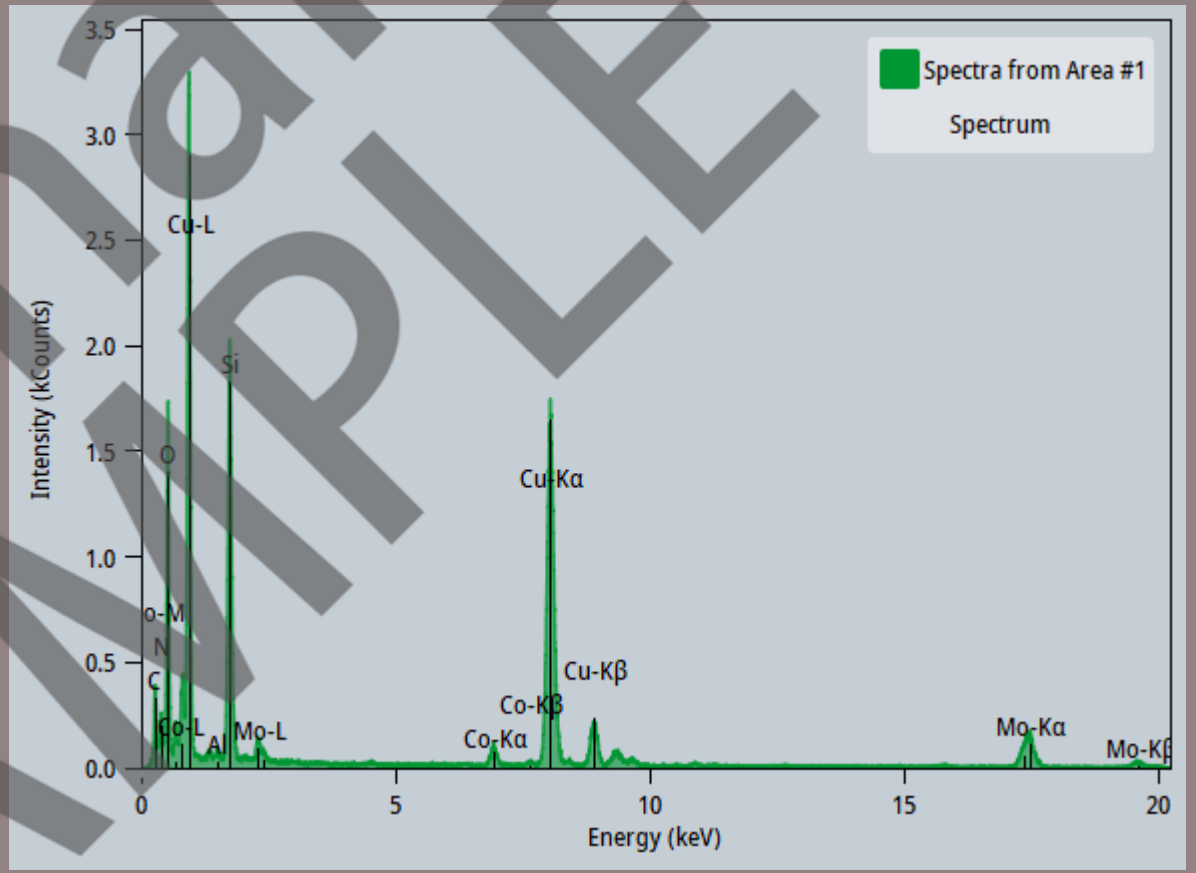


Data From (T239 EDS X 1LA 1008 SI 130 kx)

Process analyze-Nvidia T239-Gate cut-EDS

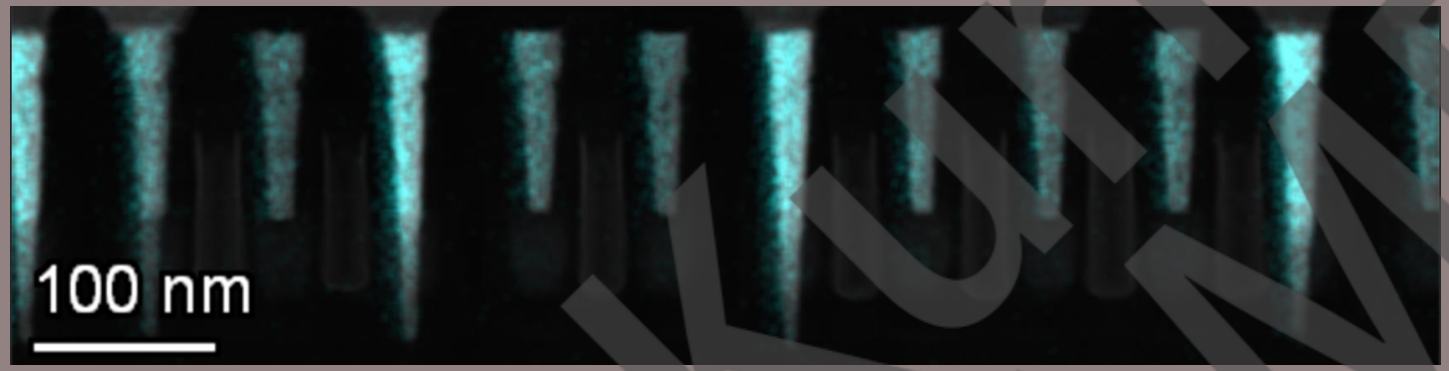


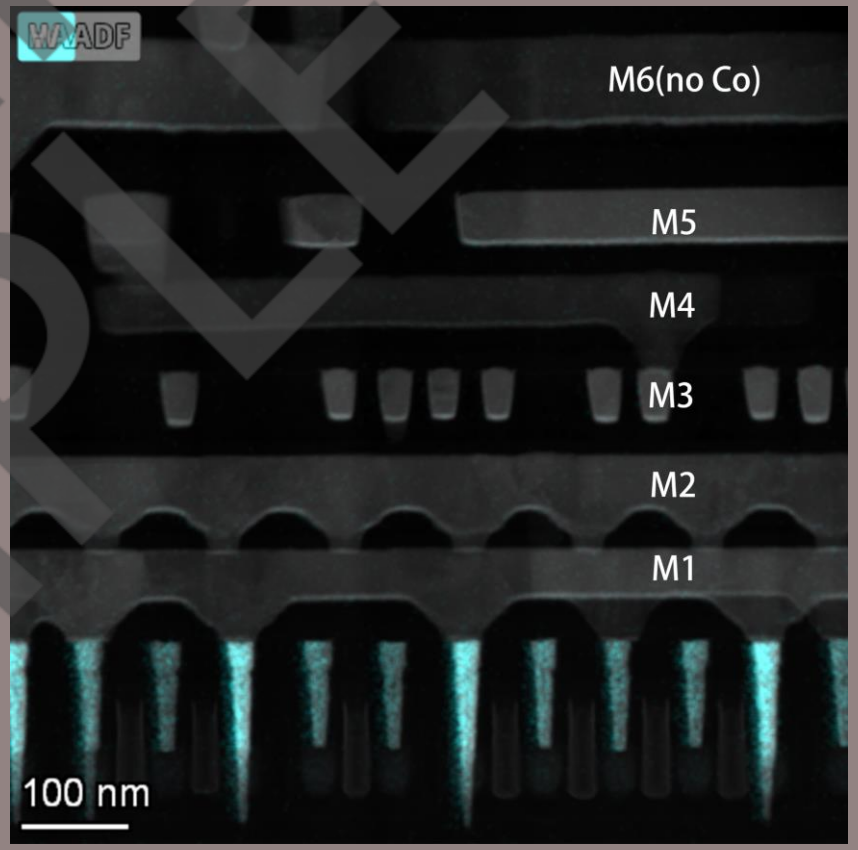
Data From (T239 EDS X 2LA 1024 SI 64000 x ColorMix)



Data From (T239 EDS X 2LA 1024 SI 64000 x)

Uses W to form plugs and contacts





Data From (T239 EDS X 1LA 1008 SI 130 kx HAADF)

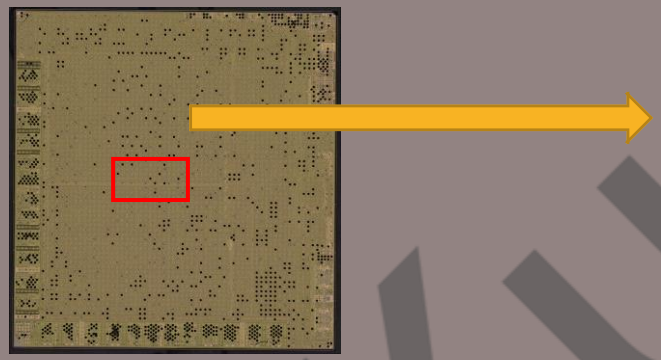
	Pitch	MMP	Element	Isolation(down)
M1	68nm	Gate Pitch	eCu	Aluminium?
M2	48nm	1x	eCu	Aluminium?
M3	48nm	1x	eCu	Aluminium?
M4	48nm	1x	eCu	Aluminium?
M5	80nm	1.66x	eCu	Aluminium?
M6	80nm	1.66x	Cu	Nitride
M7	80nm	1.66x	Cu	Nitride
M8	80nm	1.66x	Cu	Nitride
M9	80nm	1.66x	Cu	Nitride
M10	80nm	1.66x	Cu	Nitride
M11	80nm	1.66x	Cu	Nitride
M12	80nm	1.66x	Cu	Nitride

	Data
Fin Pitch	42nm
Fin number	2+2/3+3
Gate Pitch	68nm
Gate Element	HKMG(W)
2+2 Cell Height	413nm
3+3 Cell Height	413nm
Diffusion Break	MDB
Contact	SAC
Contact Element	W

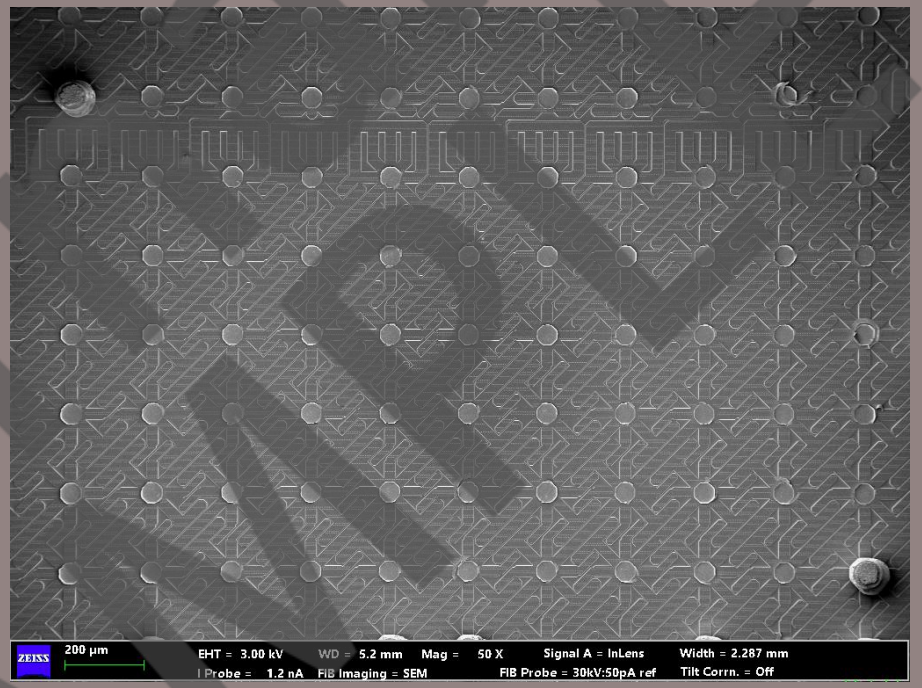
Switch2 soc analyze

Process analyze-Samsung 8nm(8N)

Process analyze-Samsung 8nm



Nvidia GA107 Die photo

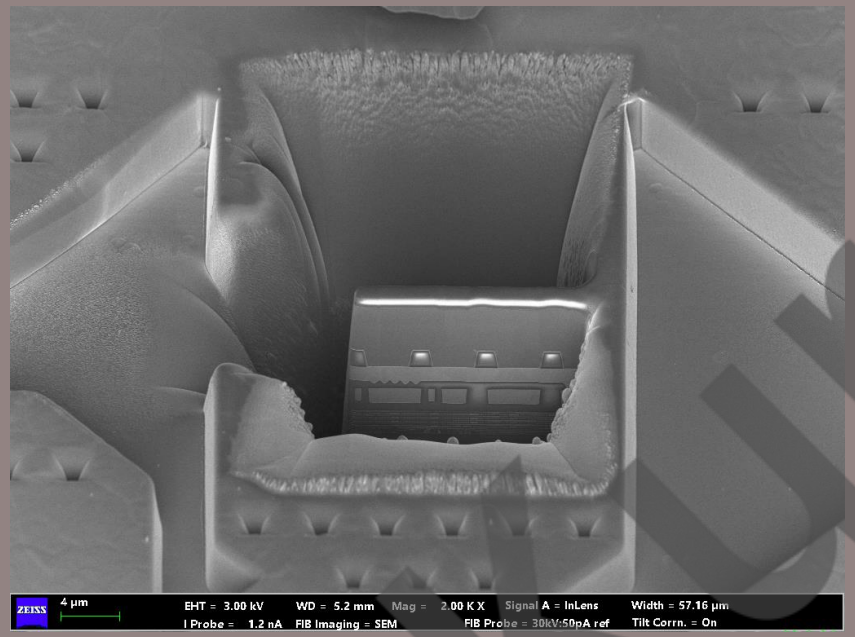


Nvidia GA107 Die photo

Using another chip fabricated in Samsung 8nm (Nvidia GA107) to analyze the fabrication process.

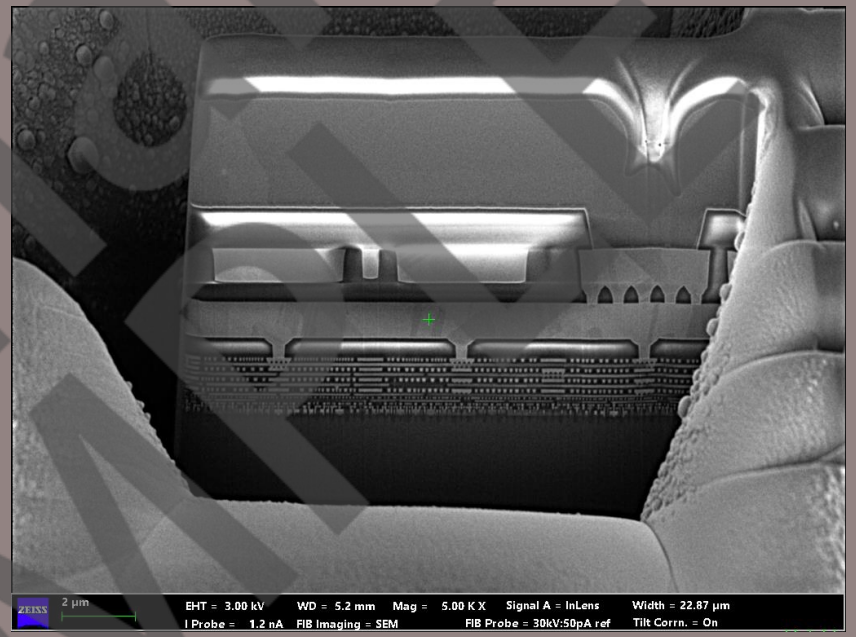
We chose the GPU for process analysis

Process analyze-Samsung 8nm



Data From (GA107 1-02)

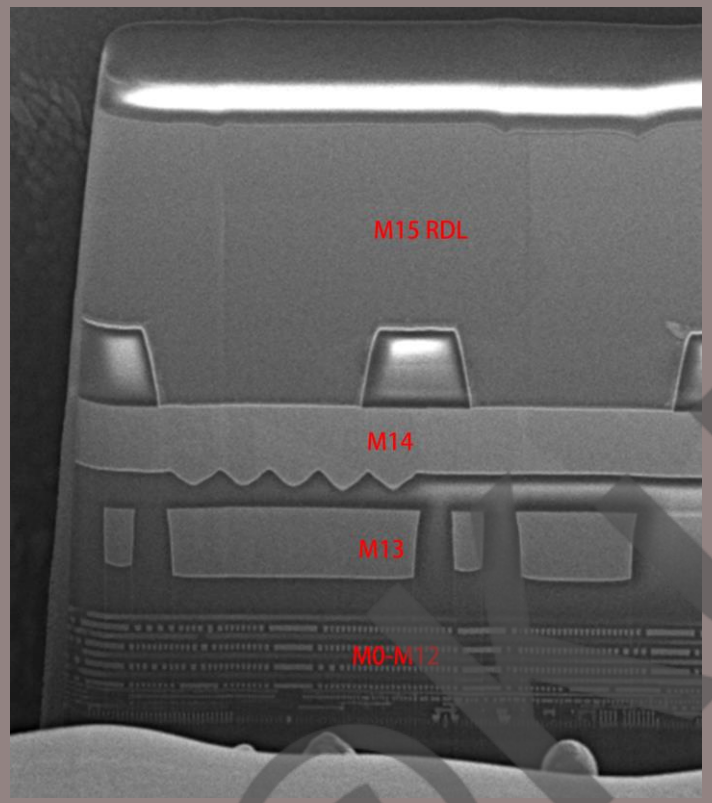
X-Cut(1)



Data From (GA107 2-02)

Y-Cut(2)

Process analyze-Samsung 8nm

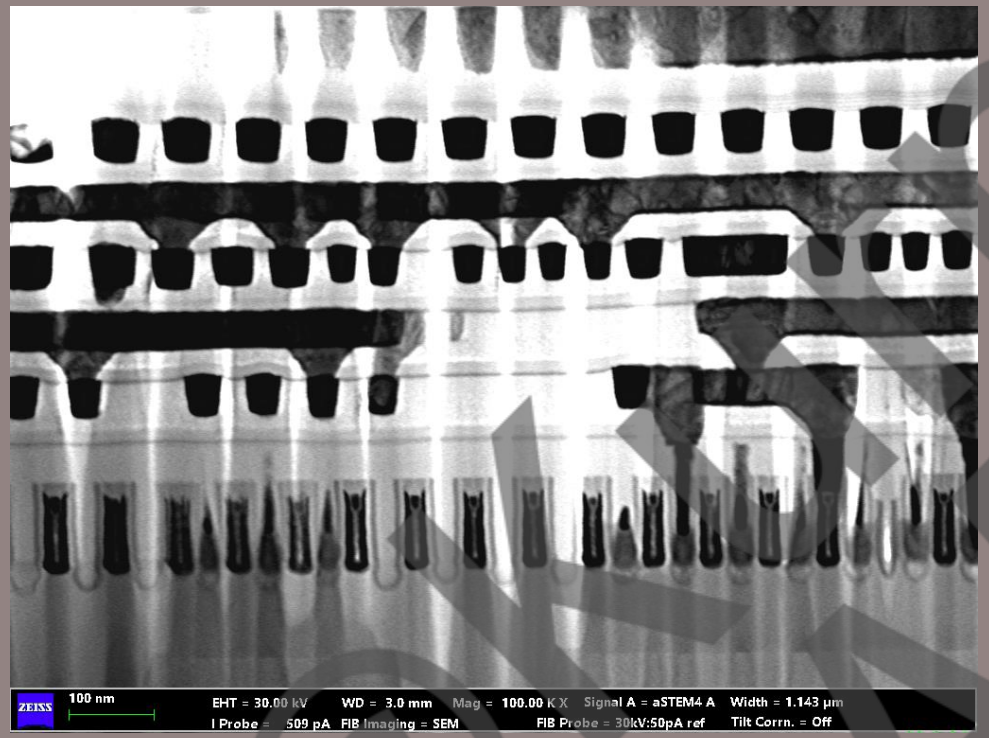


Data From (GA107 1-03)

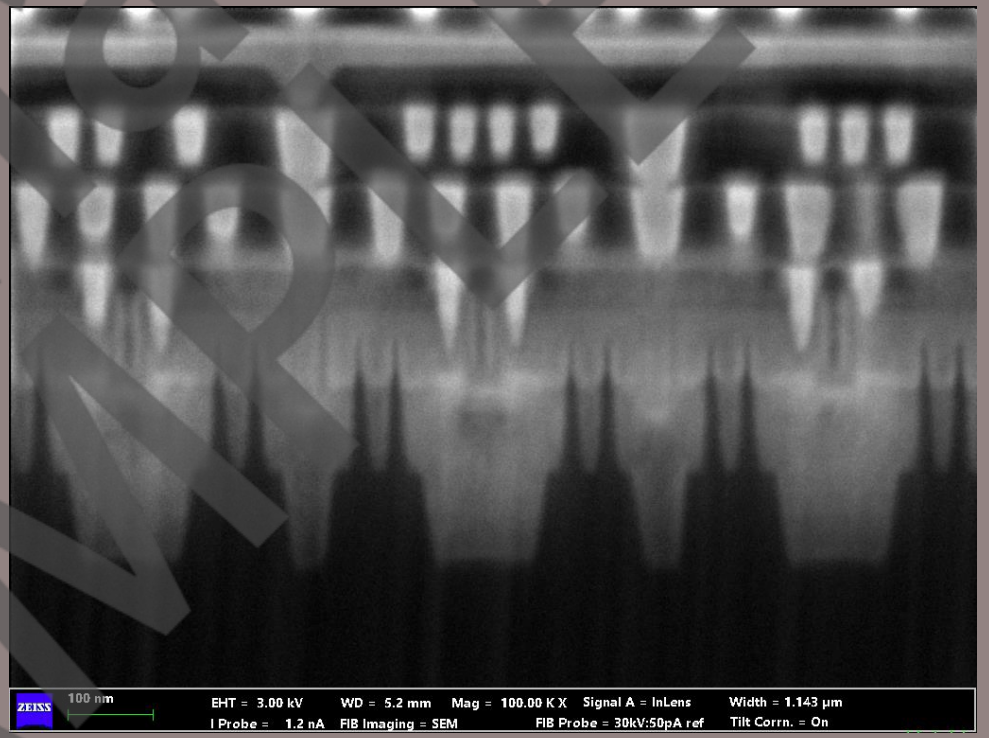
Data From (GA107 EDS-X- 0941 Camera 7000 x Ceta)

In total there are 1Poly 16Metal (15M+1Rdl)

Process analyze-Samsung 8nm



Data From (GA107 1-18)



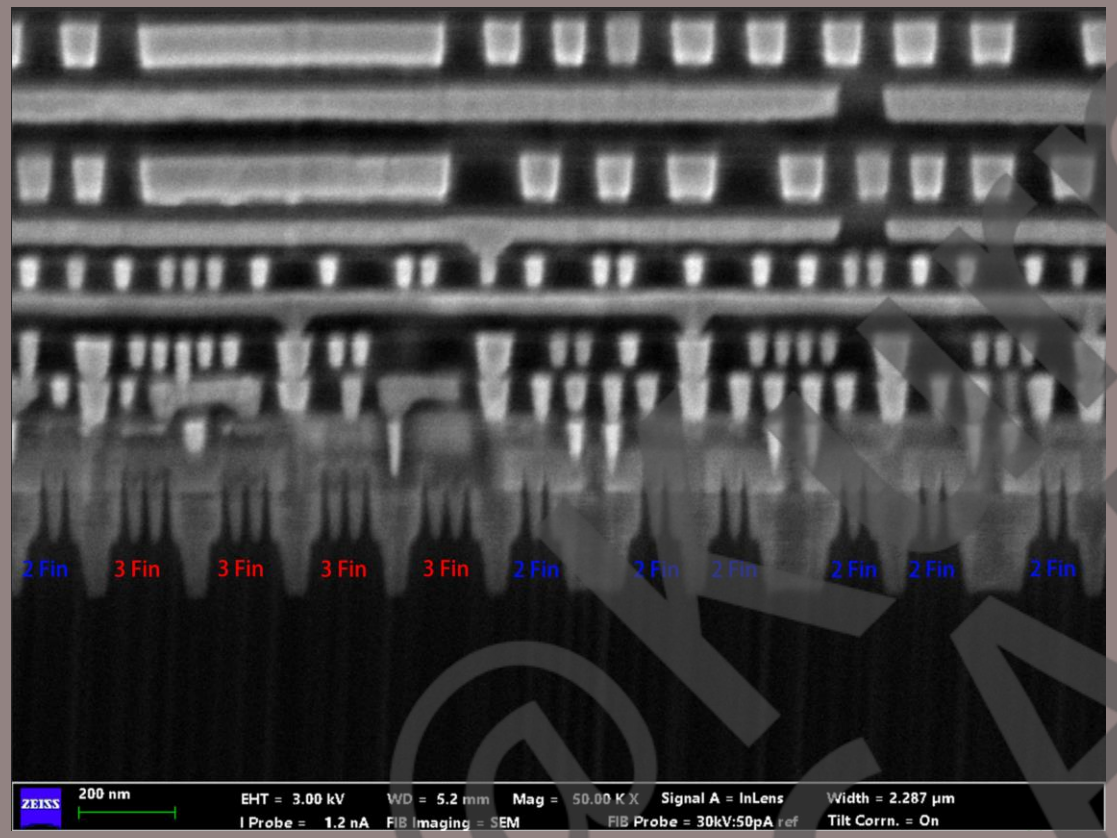
Data From (GA107 2-11)

Gate Cut

Fin Cut

Analyze Fin Cut First

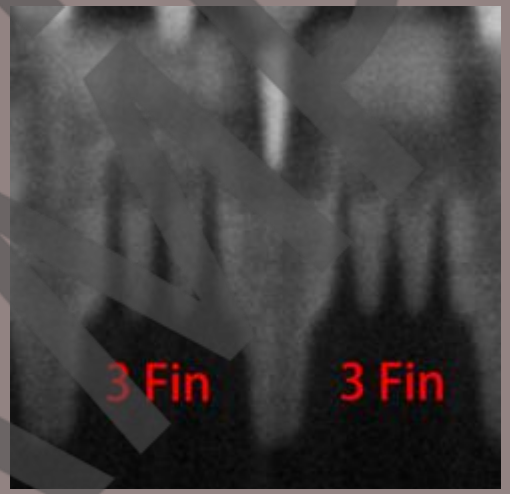
Process analyze-Samsung 8nm-Fin Cut



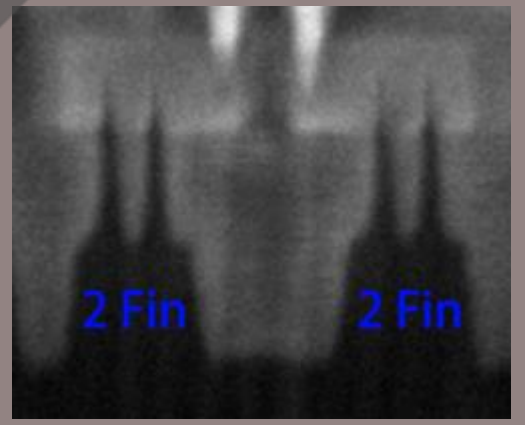
Data From (GA107 2-10)

2 types of fin arrangement from different standard cell libraries

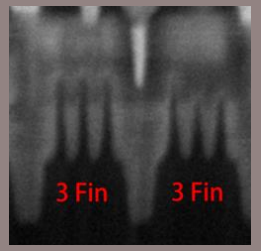
3+3 Fin



2+2 Fin



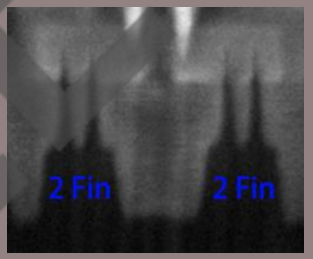
Data From (GA107 2-10)



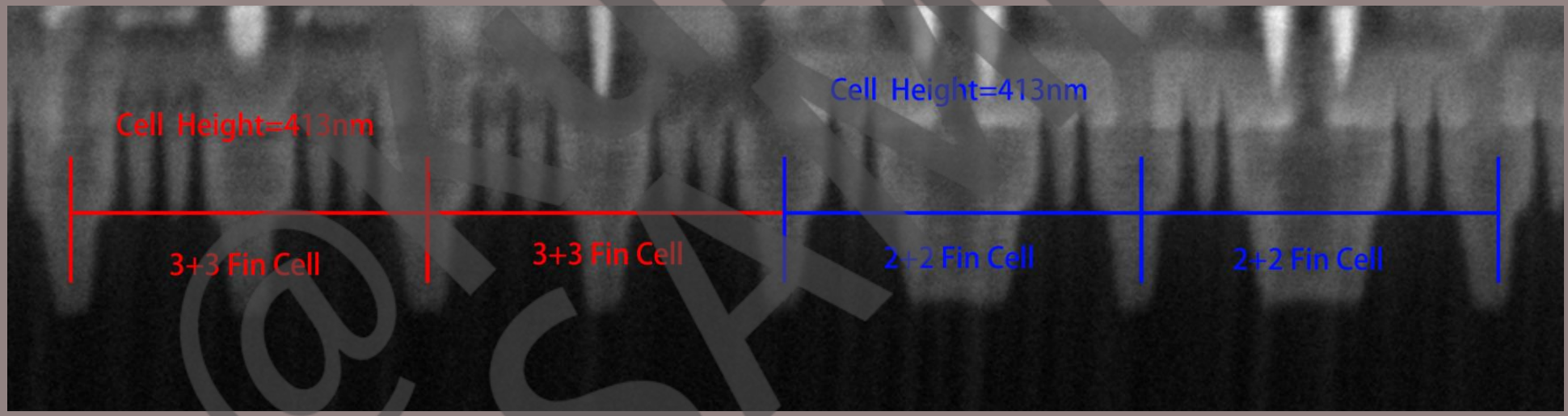
3+3 Fin

In the GA107 die, fabricated in the Samsung 8N node

Both 3+3 and 2+2 cells share the same cell height

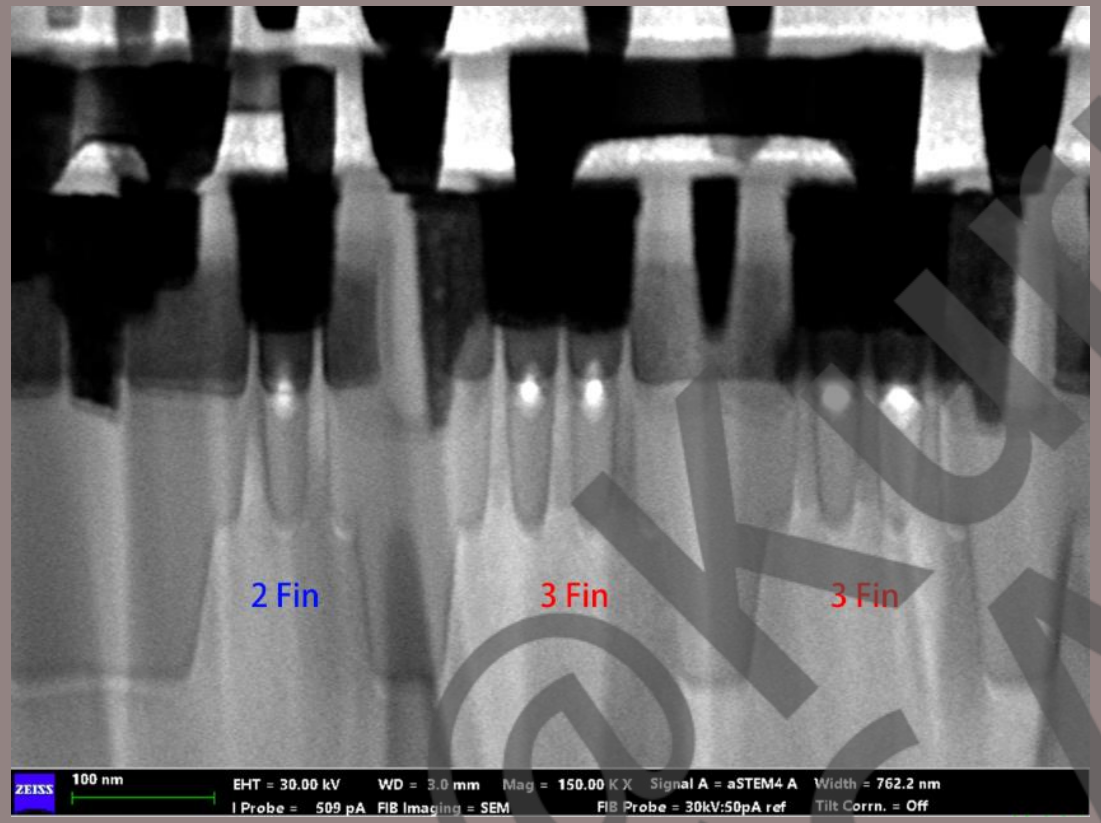


2+2 Fin

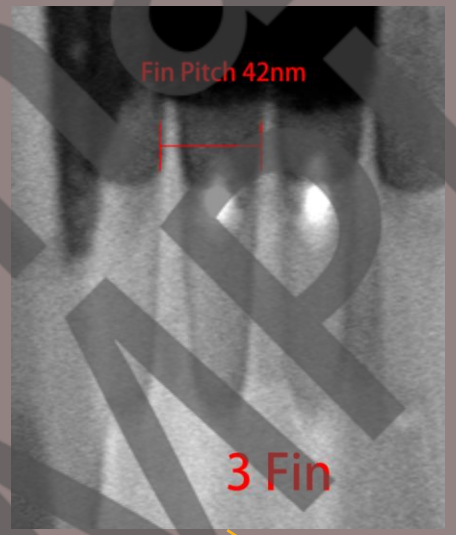


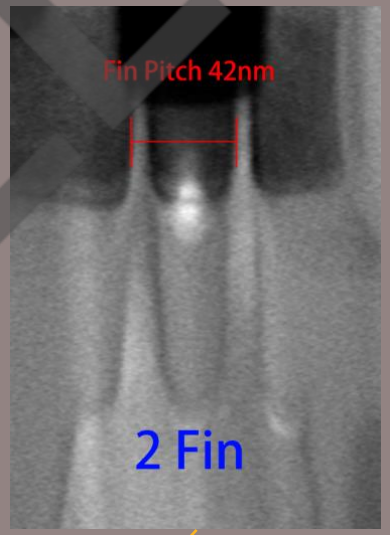
Data From (GA107 2-10)

Process analyze-Samsung 8nm-Fin Cut



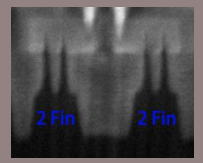
Data From (GA107 2-18)



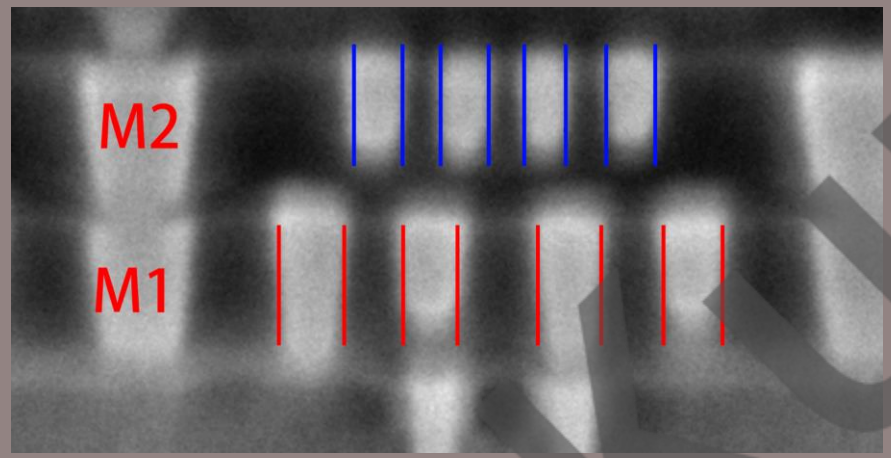


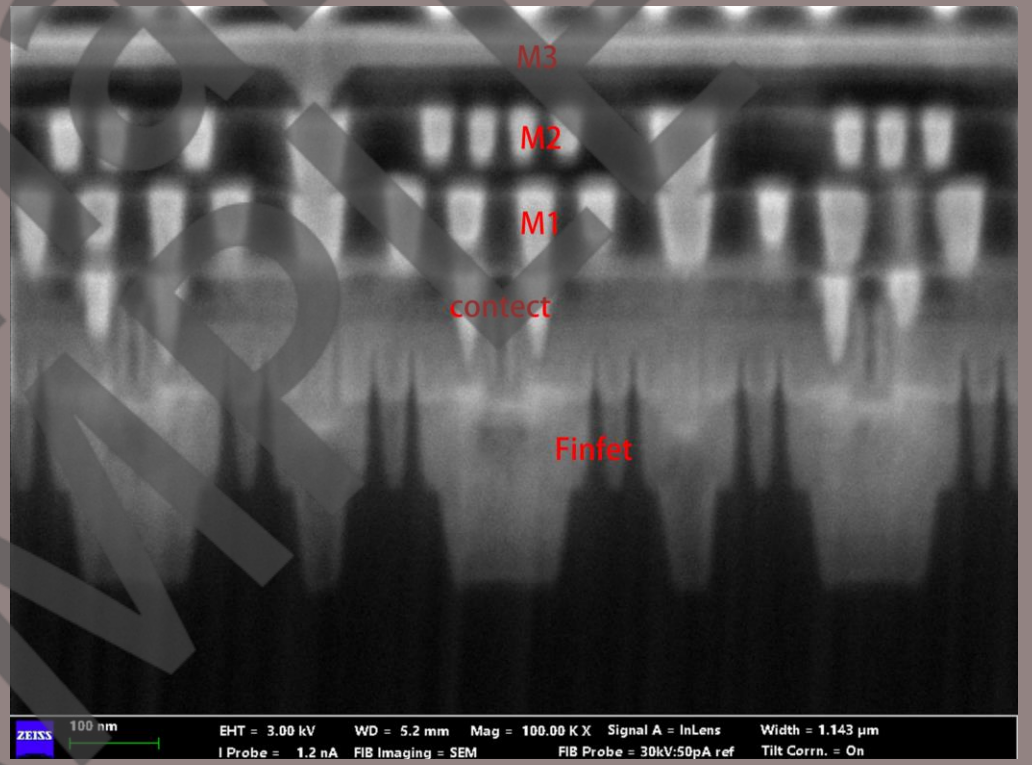
Both libs share the same fin pitch of 42nm

Process analyze-Samsung 8nm-Metal



2+2 Fin area

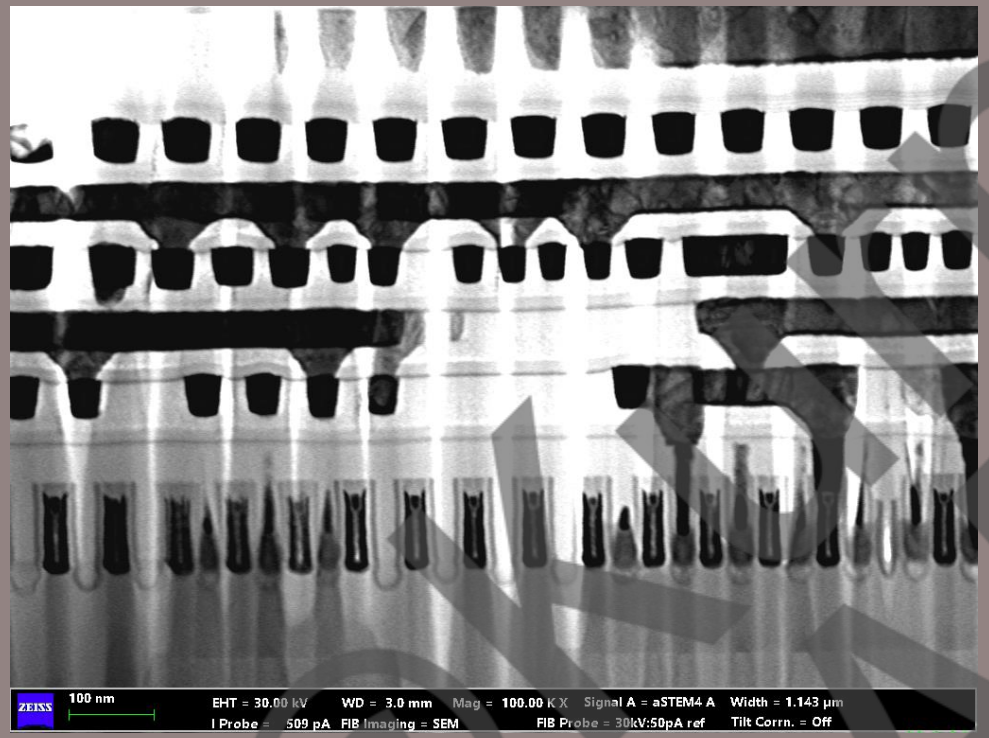




Data From (GA107 2-11)

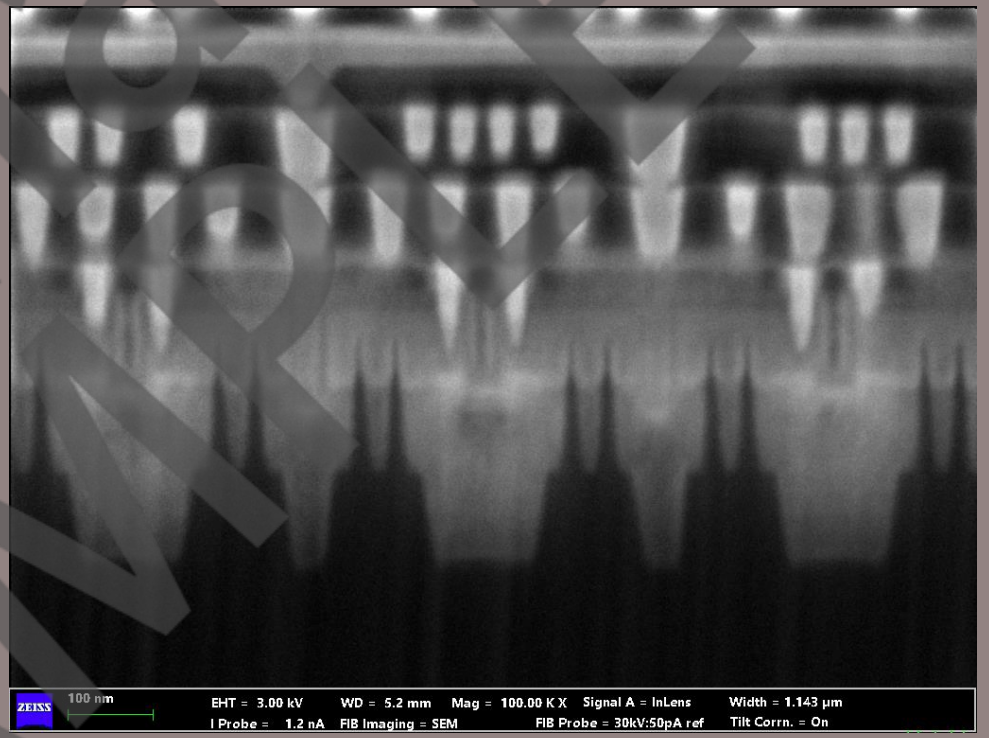
Min Metal Layer From Metal 2
M1 Pitch= 68nm
M2 Pitch= 48nm
contact Pitch=M1 Pitch

Process analyze-Samsung 8nm



Data From (GA107 1-18)

Gate Cut

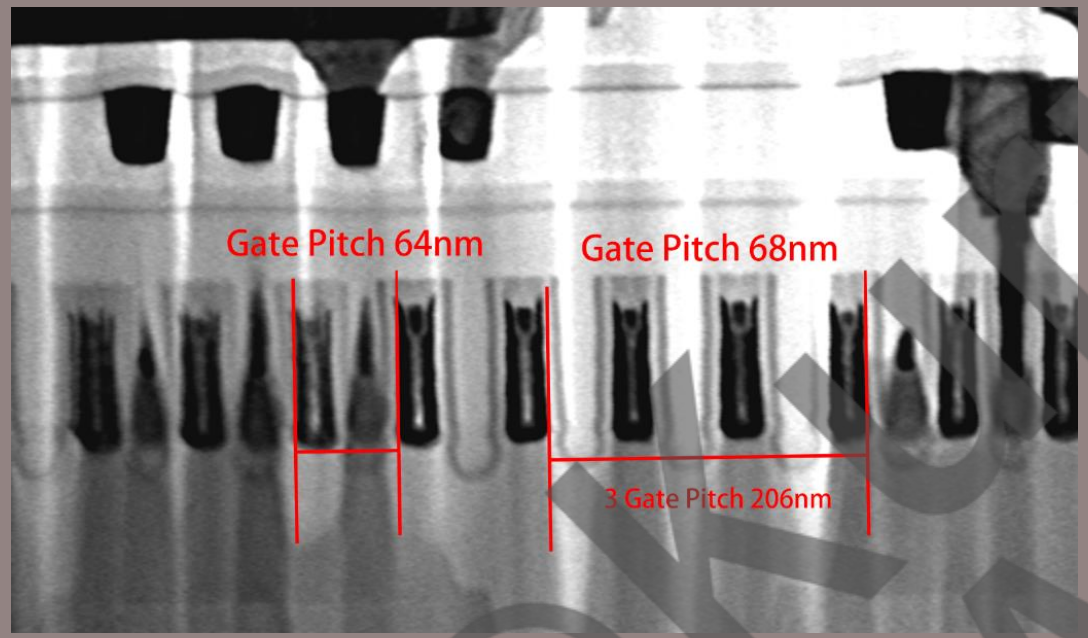


Data From (GA107 2-11)

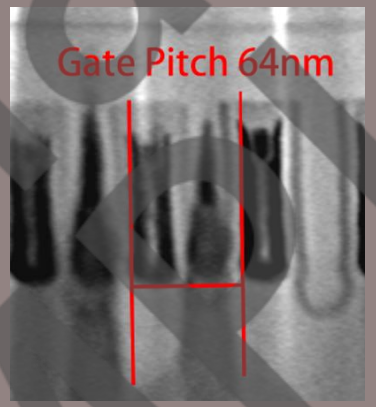
Fin Cut

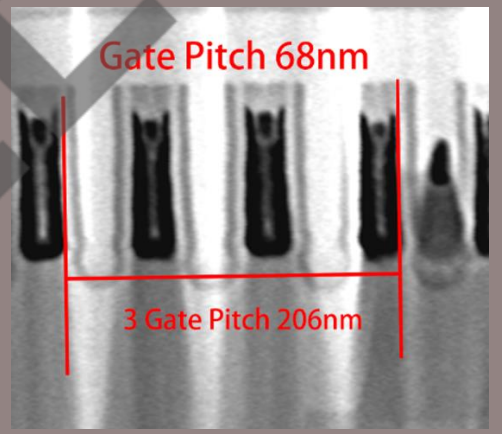
Analyze Gate Cut

Process analyze-Samsung 8nm-Y Cut



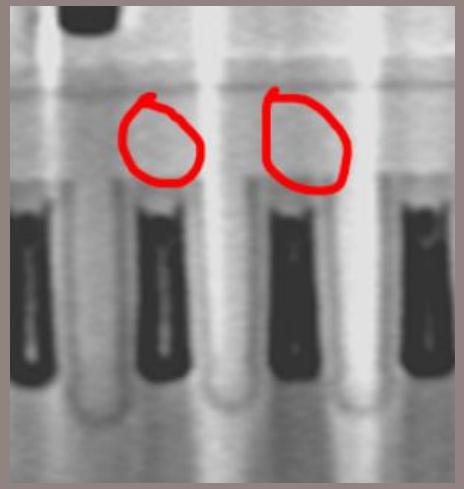
Data From (GA107 I-18)



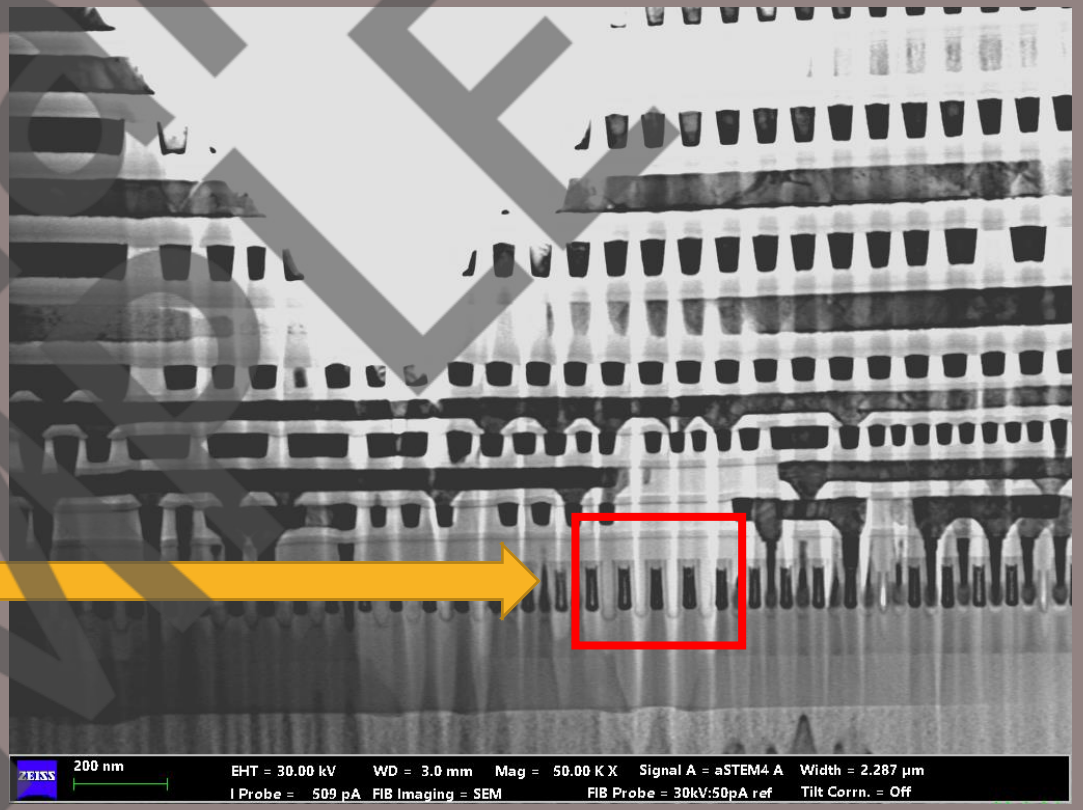


There are two libs with different gate pitches:
CGP 64 and CGP 68

No COAG（contact Over Active Gate）

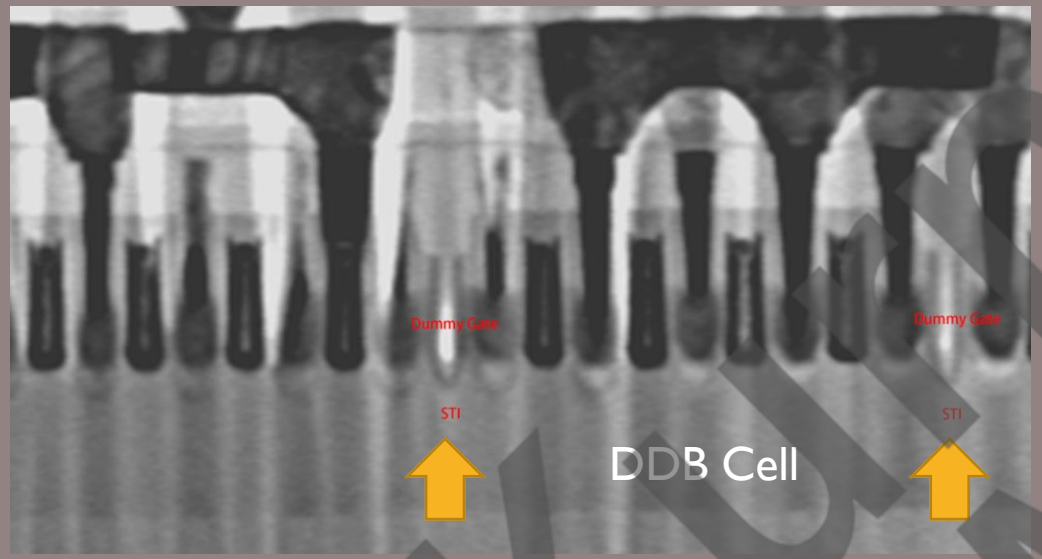


Use Self-Aligned-contact

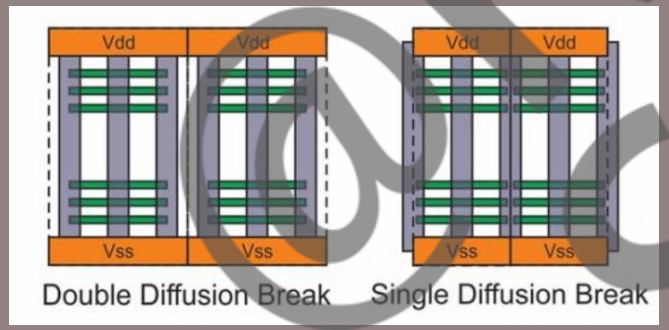


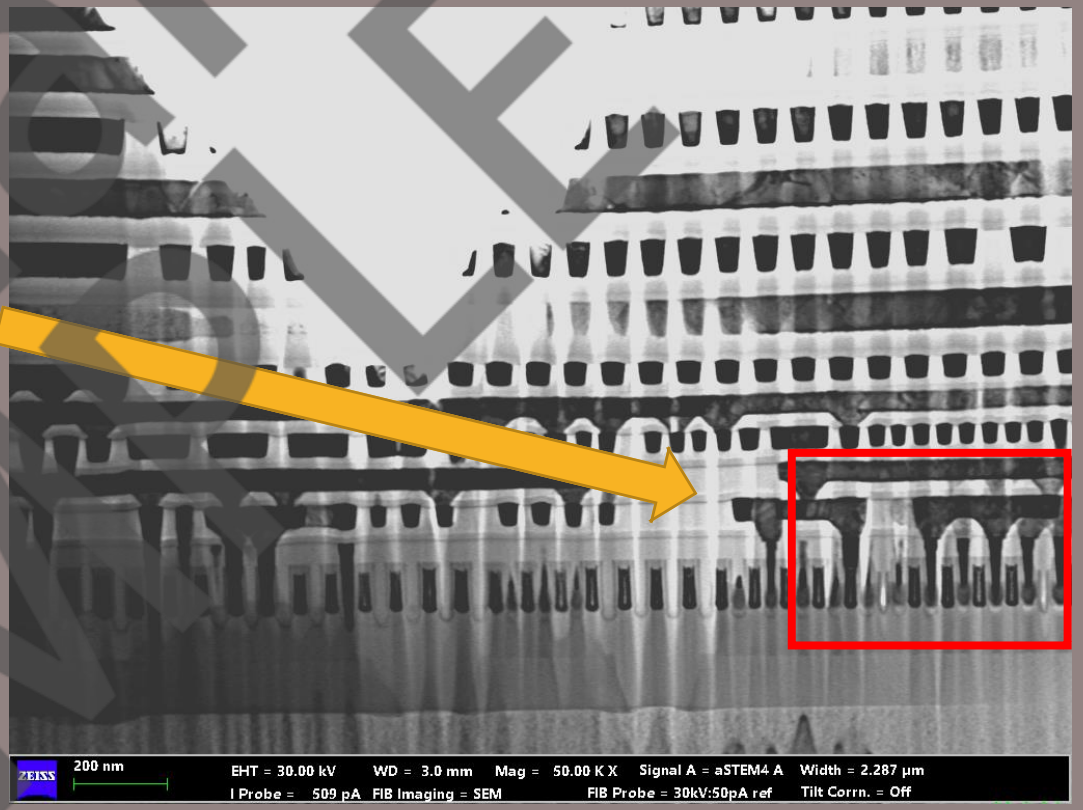
Data From (GA107 1-17)

Process analyze-Samsung 8nm-Y Cut



Mixed Diffusion Break



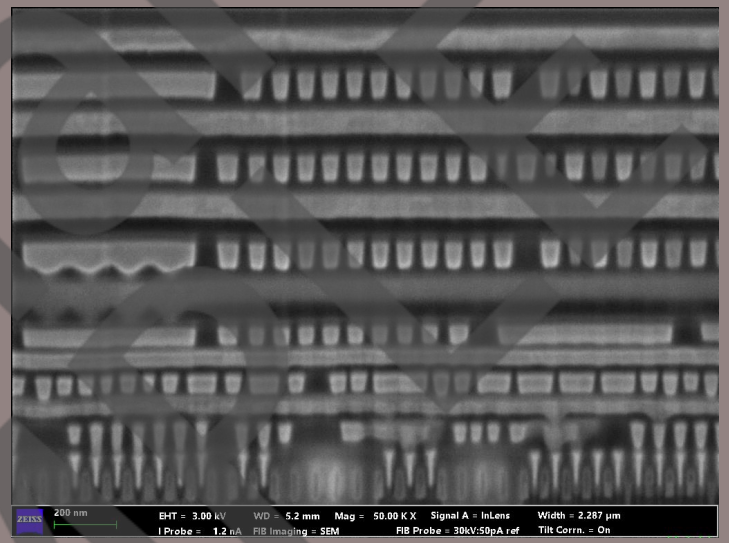


Data From (GA107 1-17)

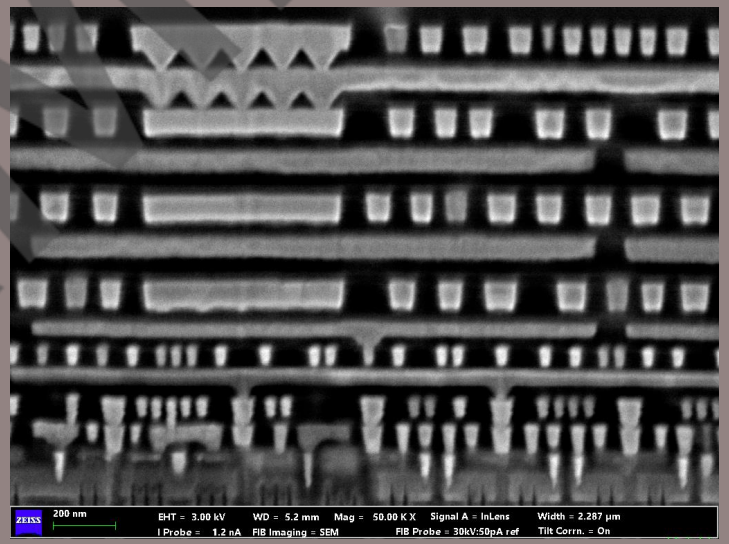
Process analyze-Samsung 8nm-Metal

	Pitch	MMP
M1	68nm	Gate Pitch
M2	48nm	1x
M3	48nm	1x
M4	48nm	1x
M5	80nm	1.66x
M6	80nm	1.66x
M7	80nm	1.66x
M8	80nm	1.66x
M9	80nm	1.66x
M10	80nm	1.66x
M11	80nm	1.66x
M12	80nm	1.66x

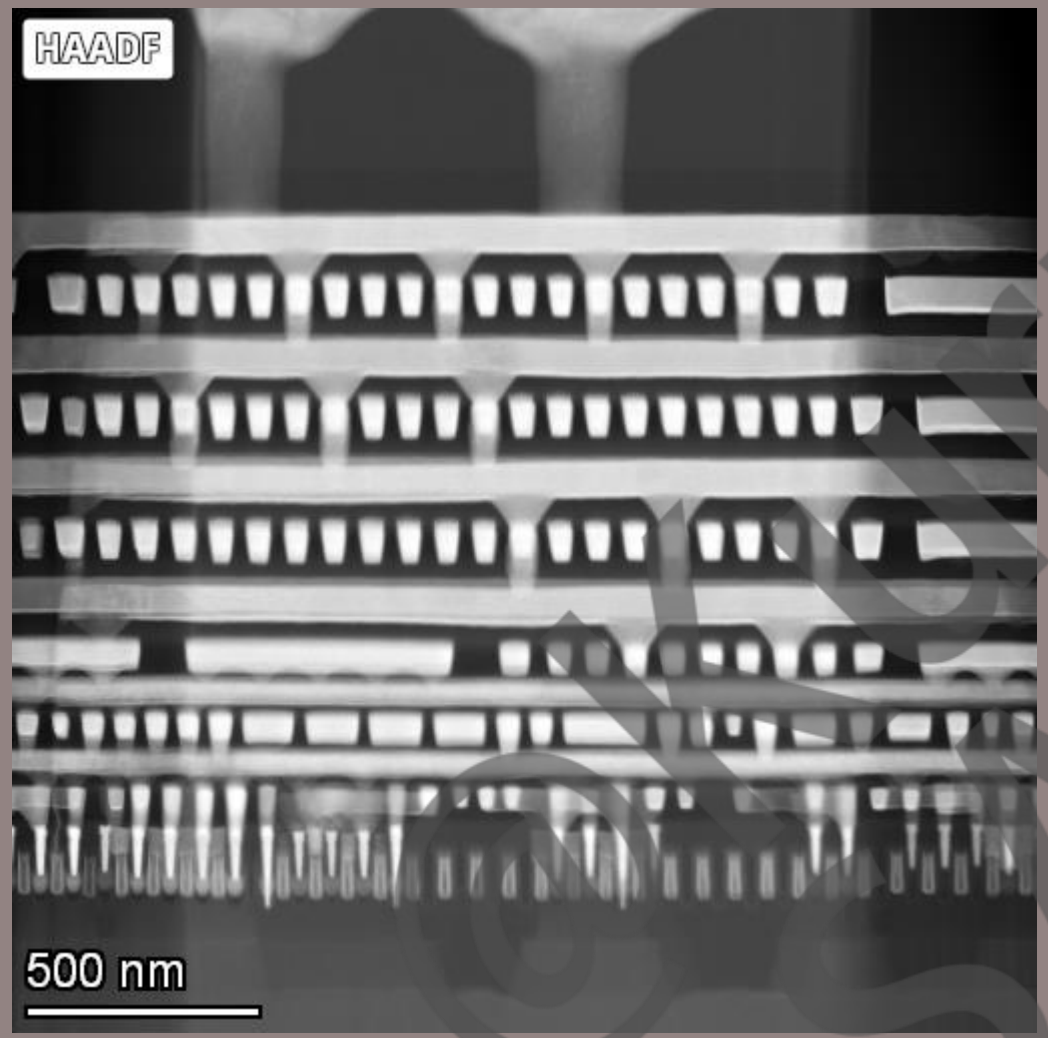
Data From (GA107 1-09)



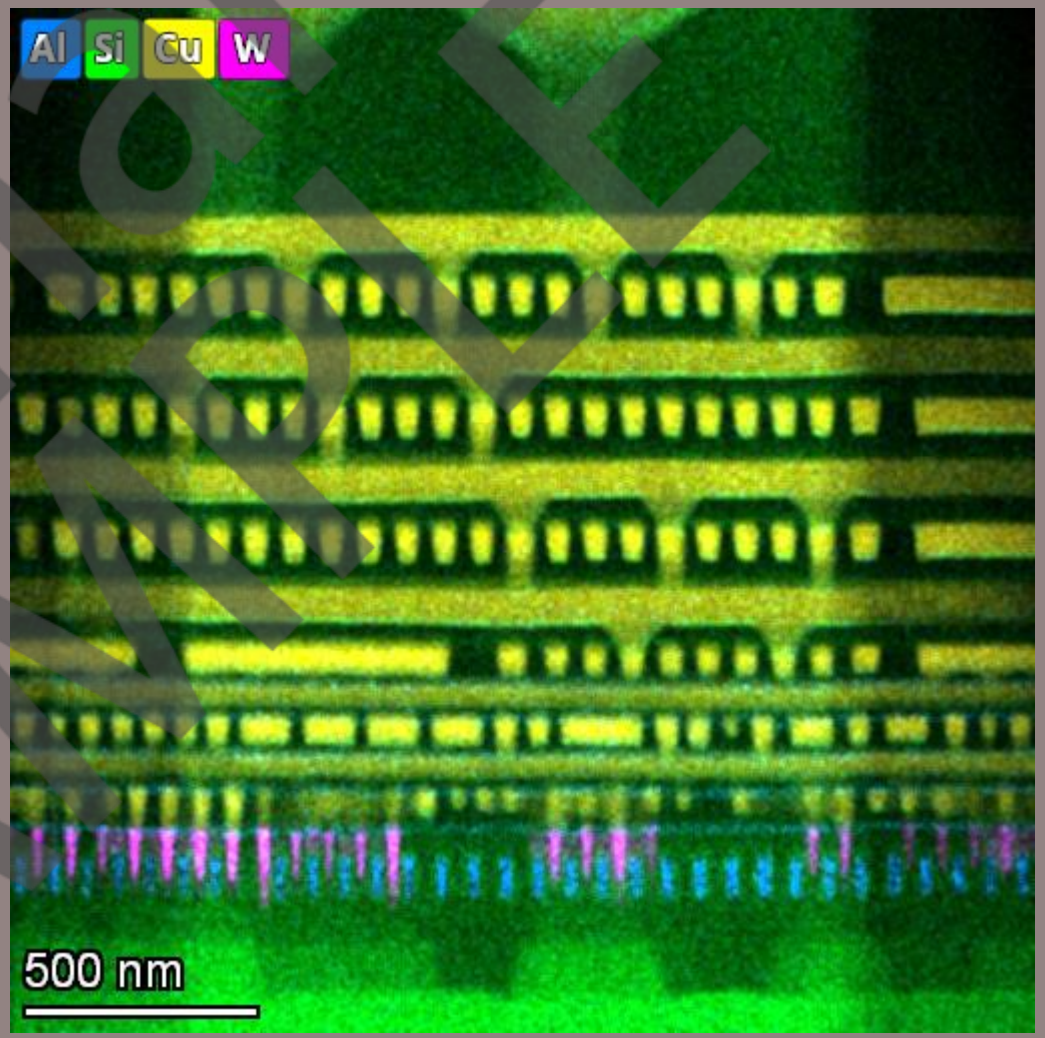
Data From (GA107 2-09)



Process analyze-Samsung 8nm-Gate Cut

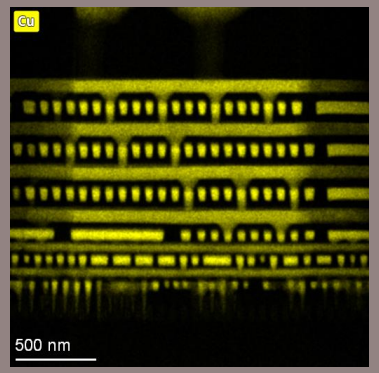


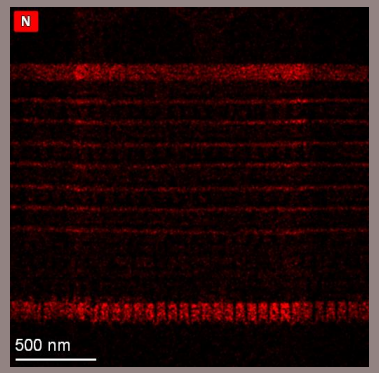
GA107-EDS(0944 SI 45000 x HAADF)

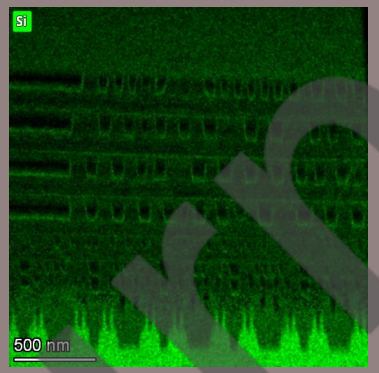


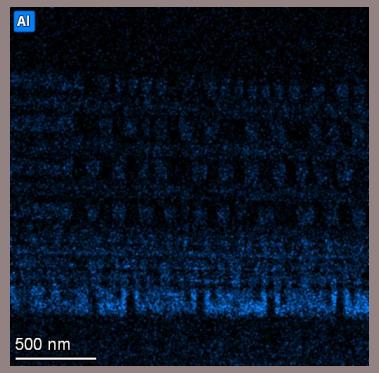
GA107-EDS(0944 SI 45000 x ColorMix-02)

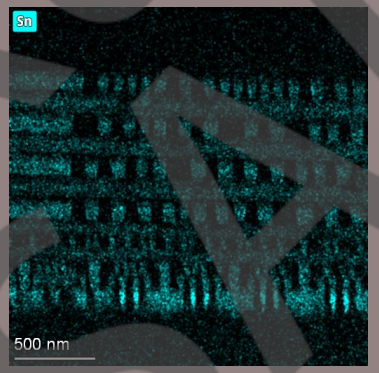
Process analyze-Samsung 8nm-Gate Cut

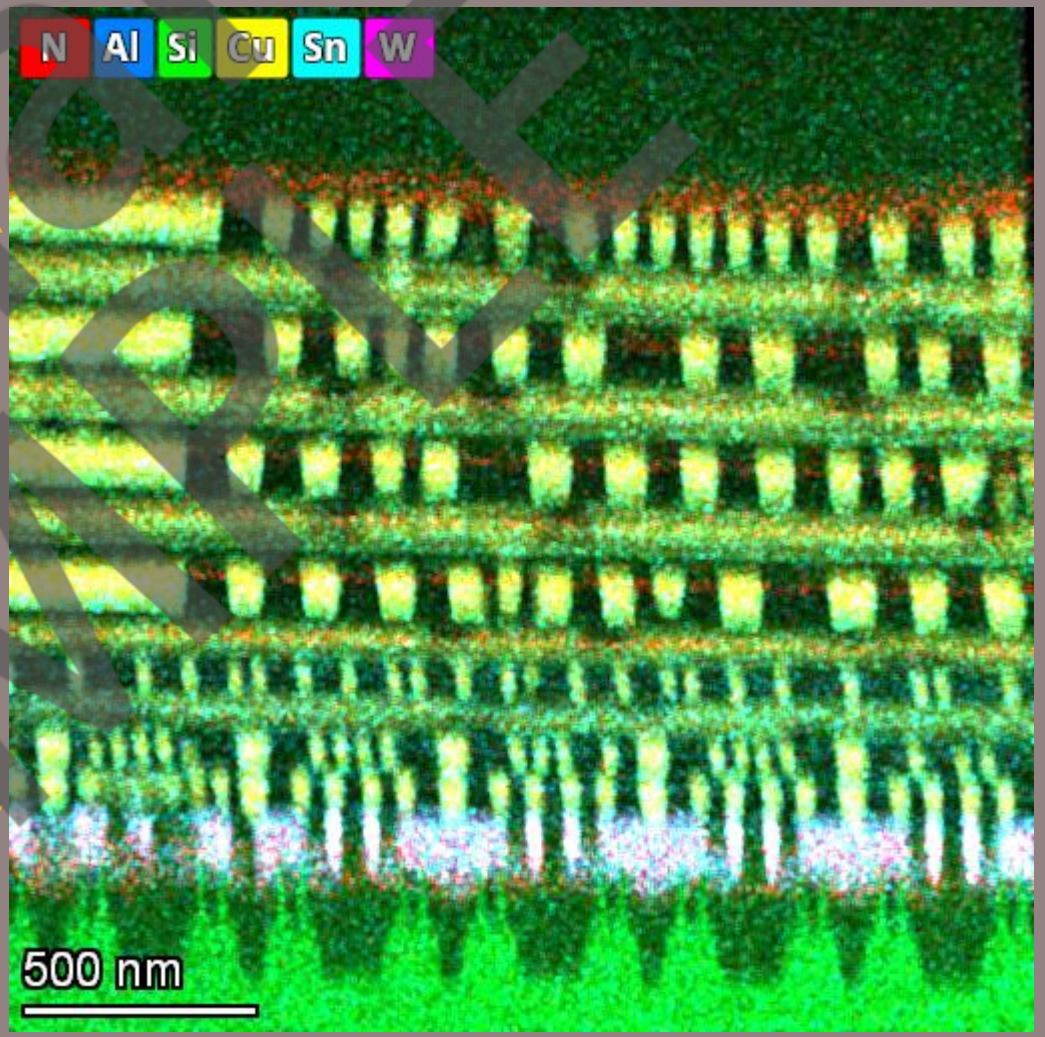






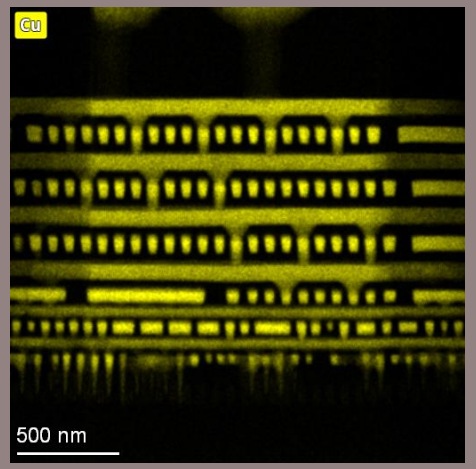


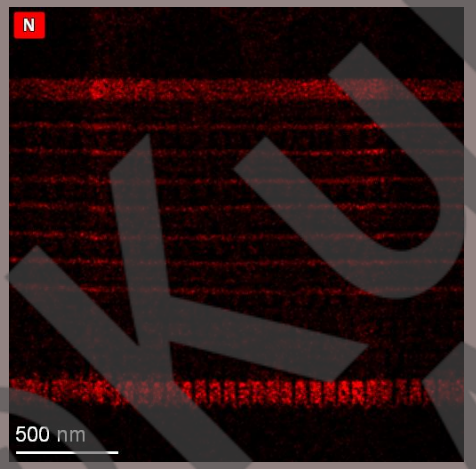




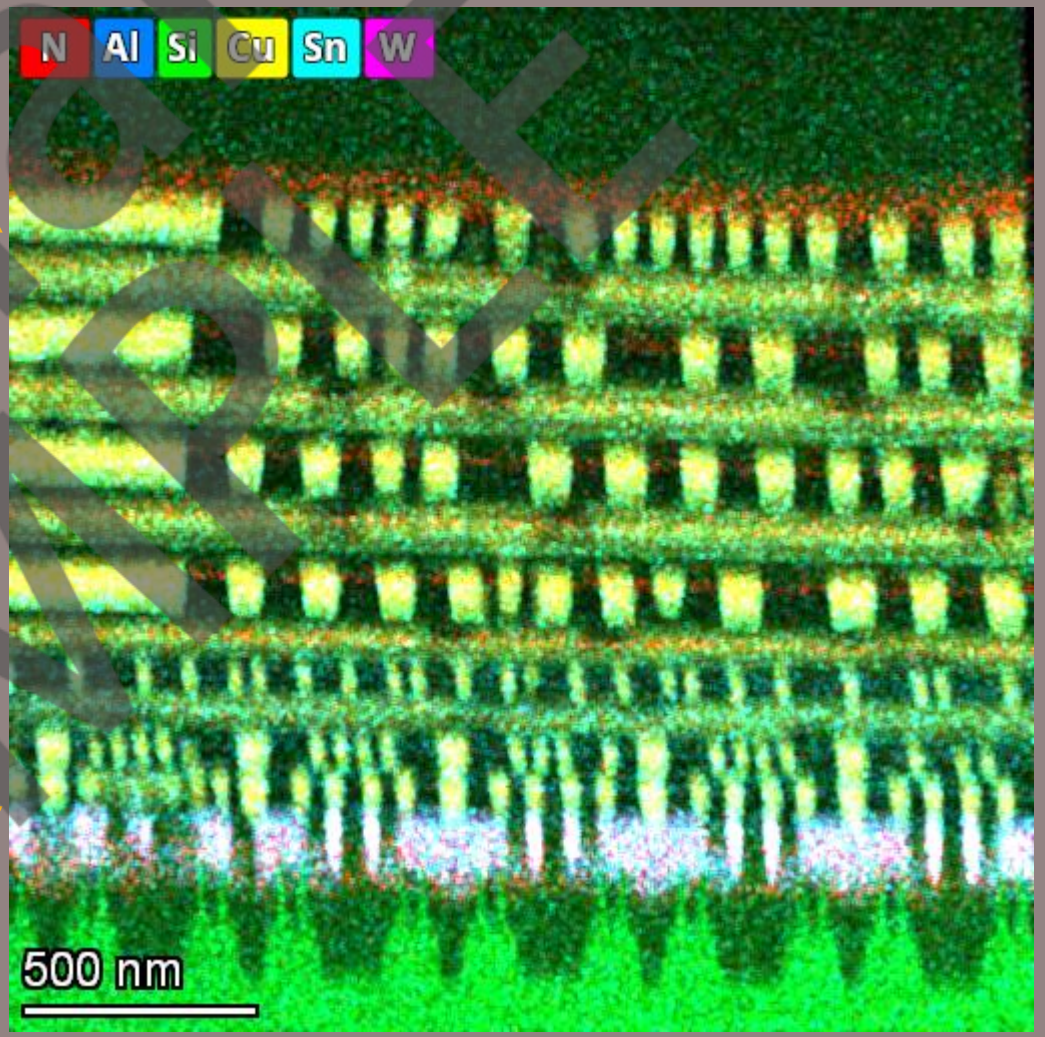
GA107-EDS(0944 SI 45000 x ColorMix-net)

M1-M12 used the Cu



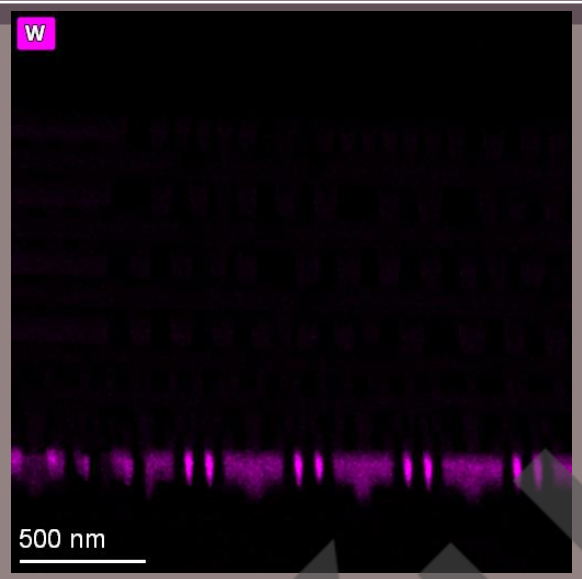


Uses the N to isolation every Layers
(SiN?)

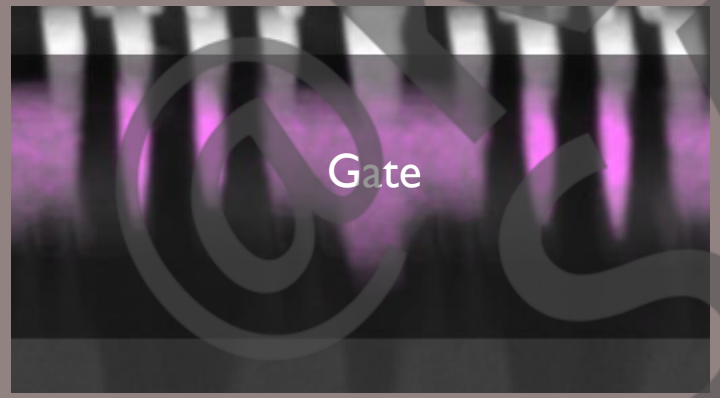


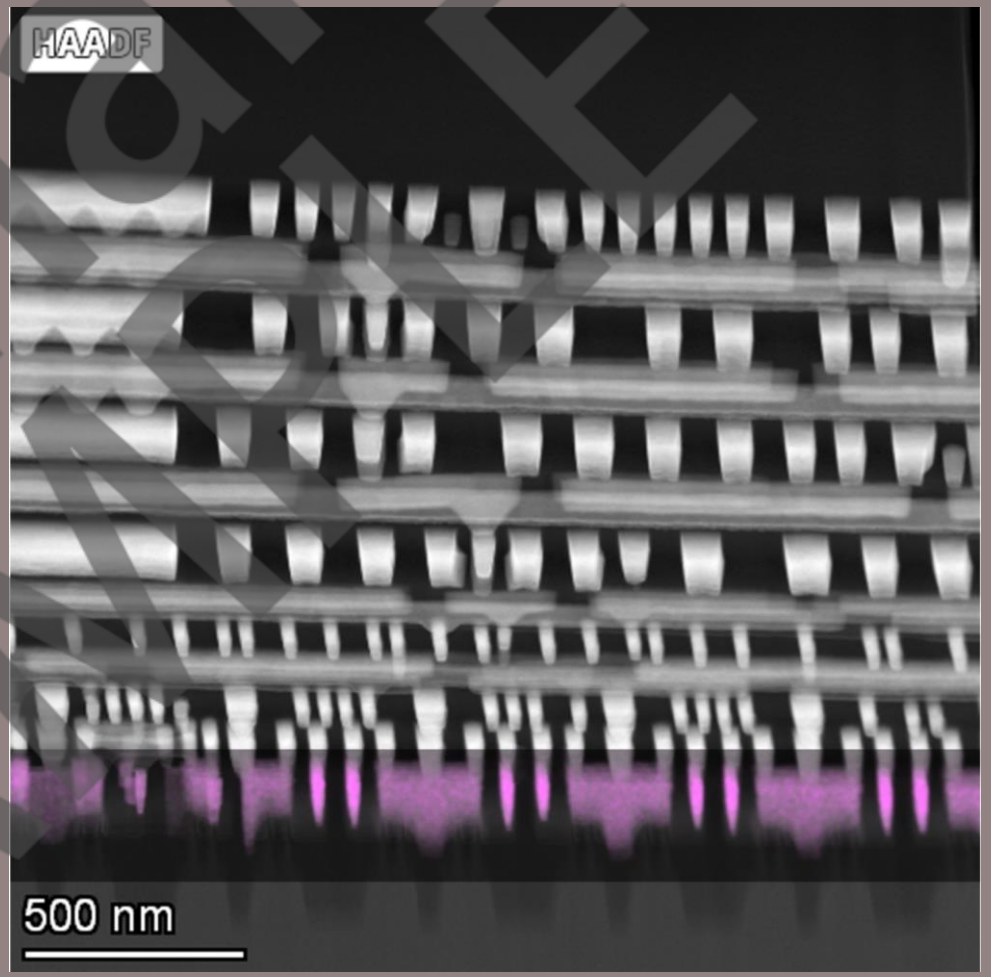
GA107-EDS(0944 SI 45000 x ColorMix-net)

Process analyze-Samsung 8nm-Gate Cut



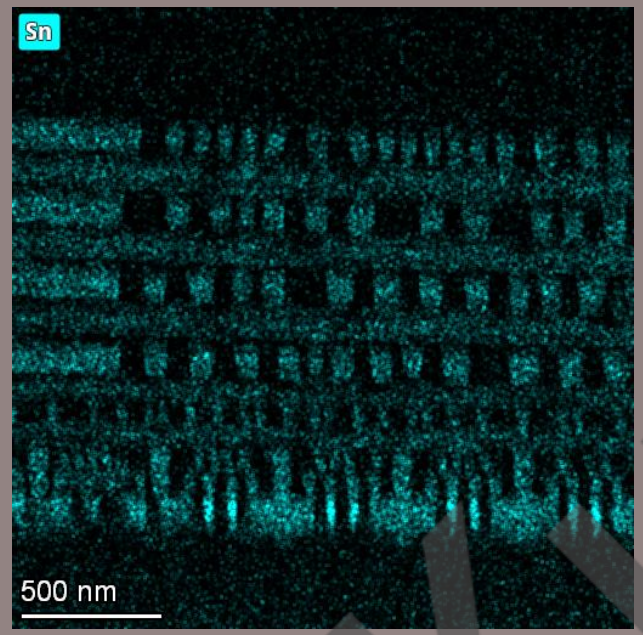
Used the W Gate and contact
It is HKMG(High K Metal Gate)



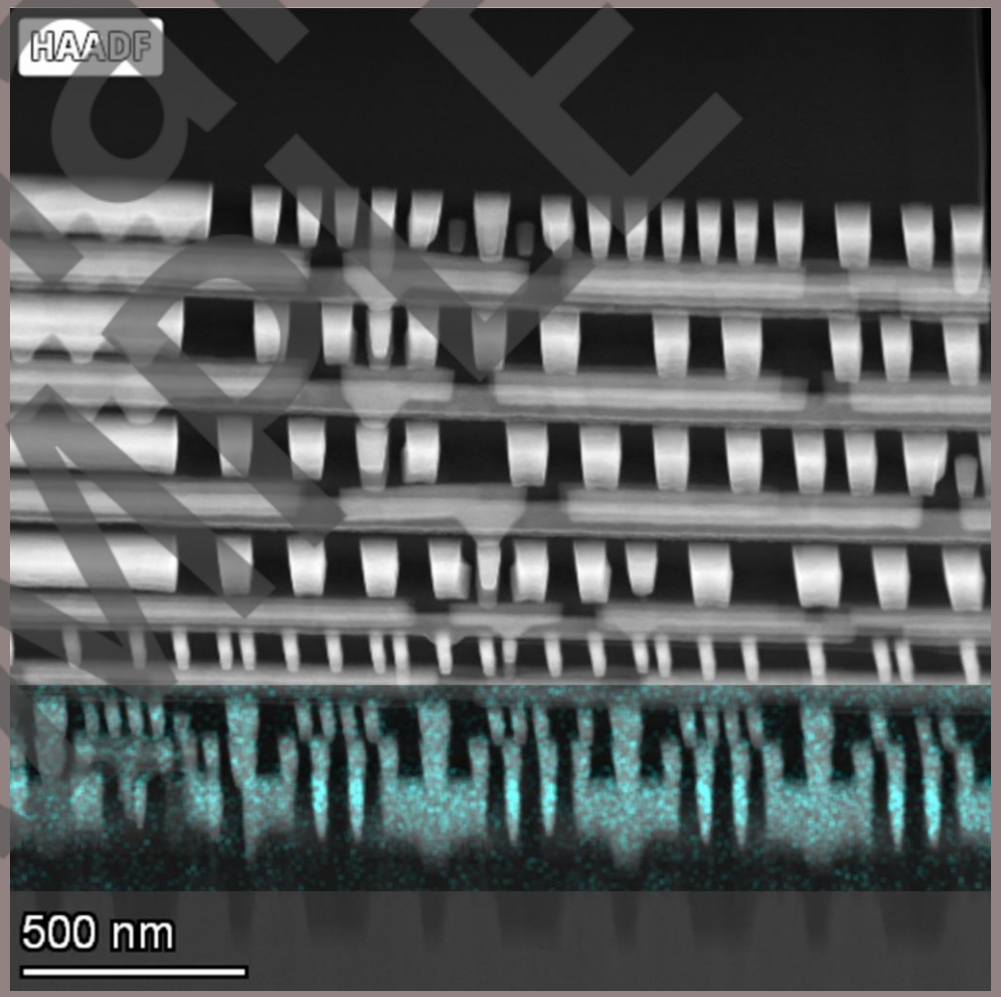


GA107-EDS(0944 SI 45000 x ColorMix-net)

Process analyze-Samsung 8nm-Gate Cut

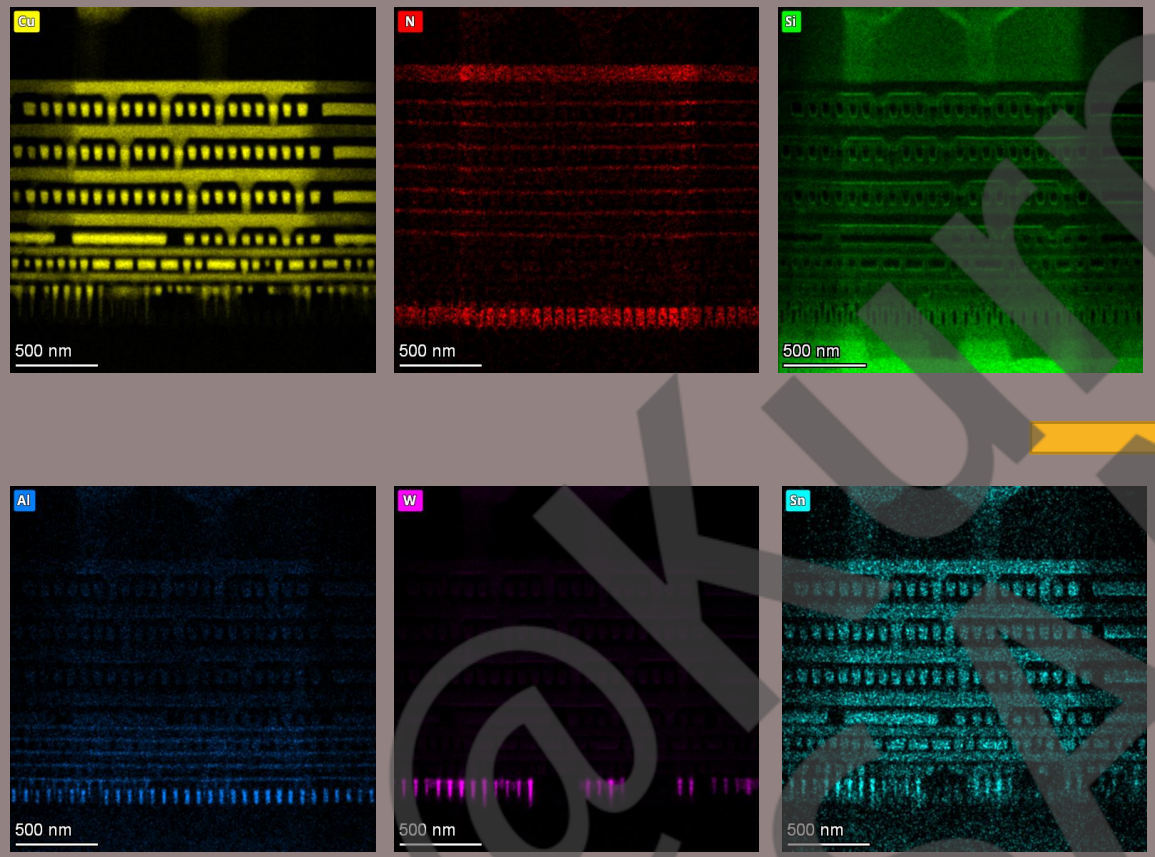


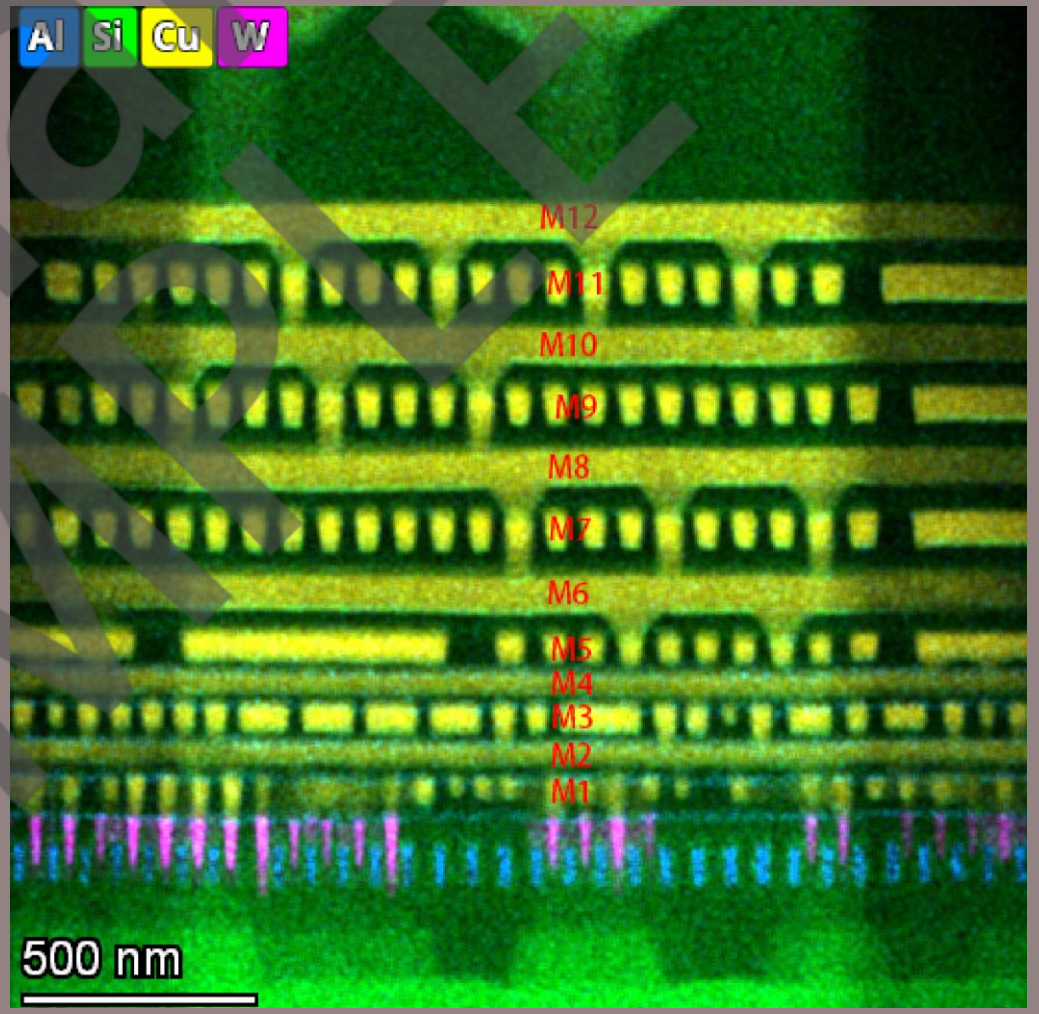
A little bit Sn in the Contact Via?



GA107-EDS(0944 SI 45000 x ColorMix-net)

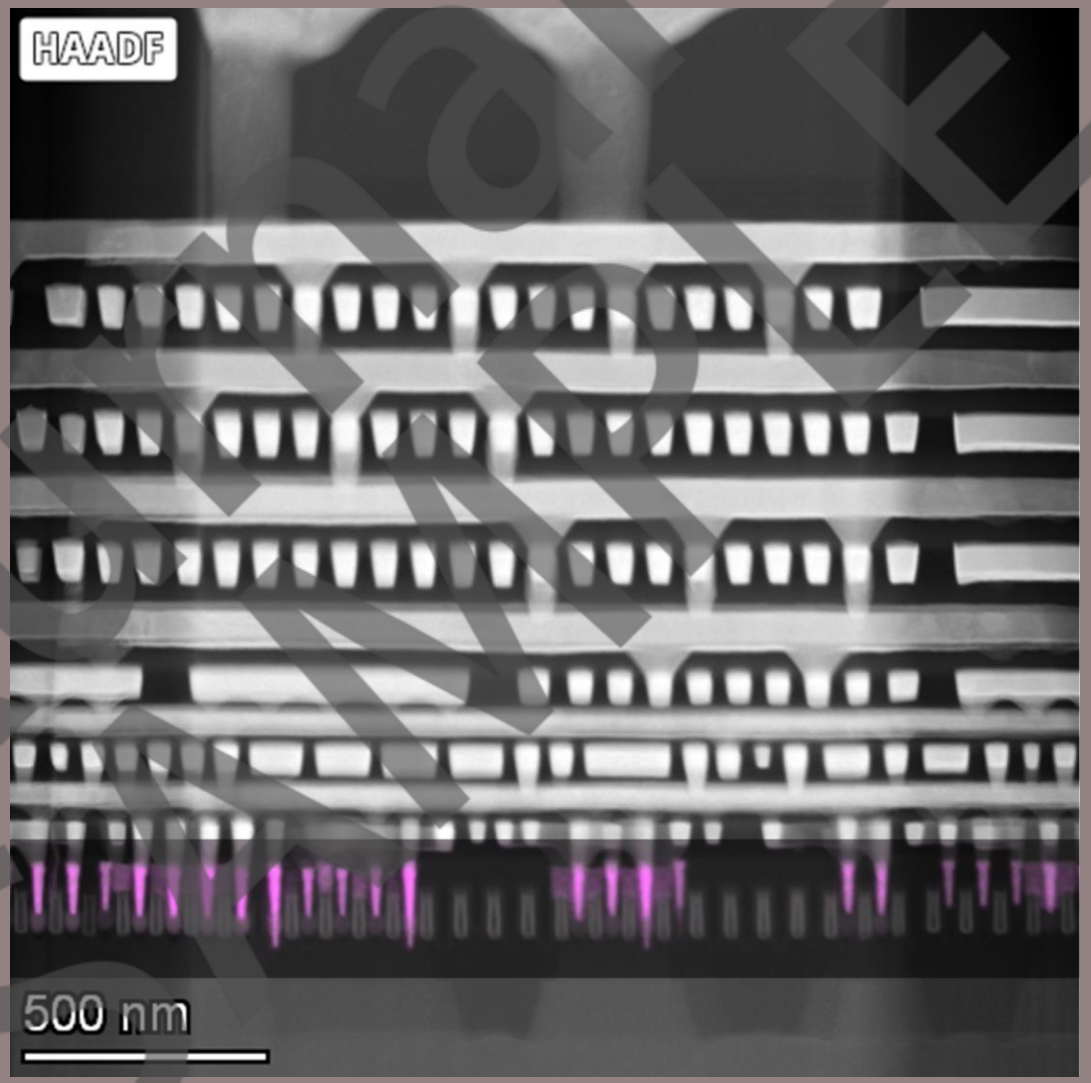
Process analyze-Samsung 8nm-Y Cut





Process analyze-Samsung 8nm-Y Cut

Used the W to contact



Process analyze-Samsung 8nm-Total

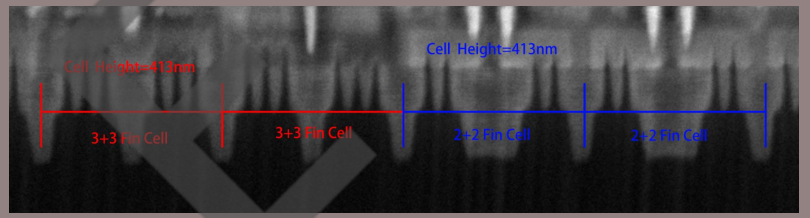
	Pitch	MMP
M1	68nm	Gate Pitch
M2	48nm	1x
M3	48nm	1x
M4	48nm	1x
M5	80nm	1.66x
M6	80nm	1.66x
M7	80nm	1.66x
M8	80nm	1.66x
M9	80nm	1.66x
M10	80nm	1.66x
M11	80nm	1.66x
M12	80nm	1.66x

What we know about
Nvidia GA107 (Samsung 8N) so far

Cell Height for 3+3 is 413nm
Cell Height for 2+2 is 413nm
M2 Pitch= 48nm
Cell Track=8.6Track
Contacted Gate Pitch=64nm/68nm

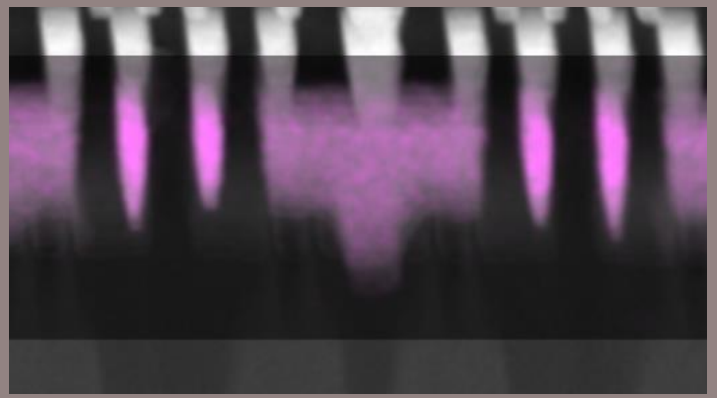
Used the Mixed Diffusion Break
Used the Self-Aligned-contact

Used the W Gate and contact
It is HKMG(High K Metal Gate)



Data From (GA107 2-10)

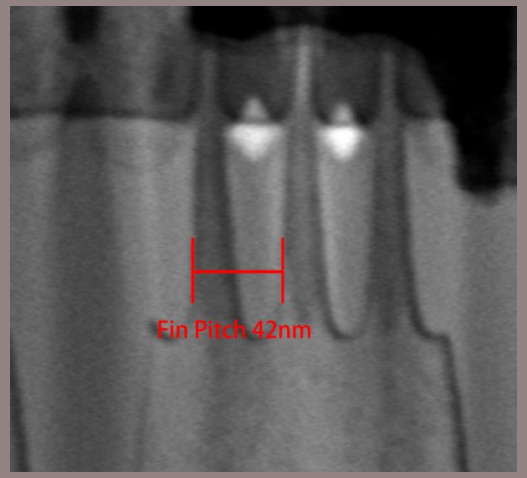
The Cell Track=Cell Height/M2 Pitch
=413nm/48nm
=8.603Track

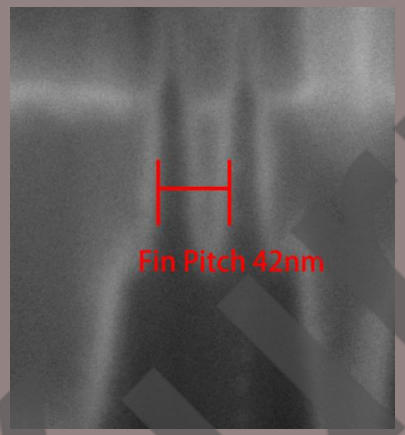


T239 SoC Identification

T239 process identical

T239 process identical-Fin cut

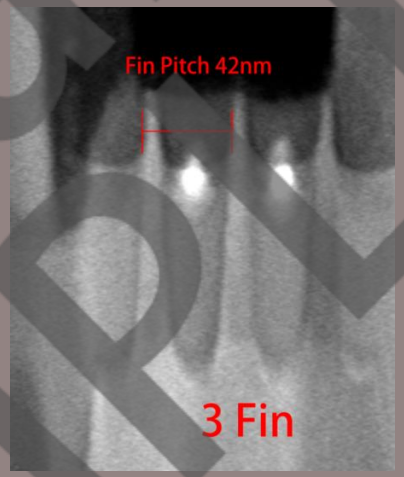


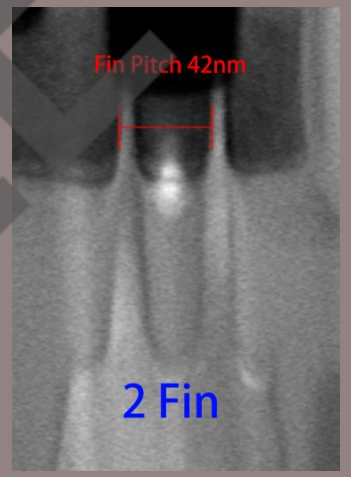


Data From (T239 2-10)

The 2 libs Fin Pitch both 42nm

T239





Data From (GA107 2-18)

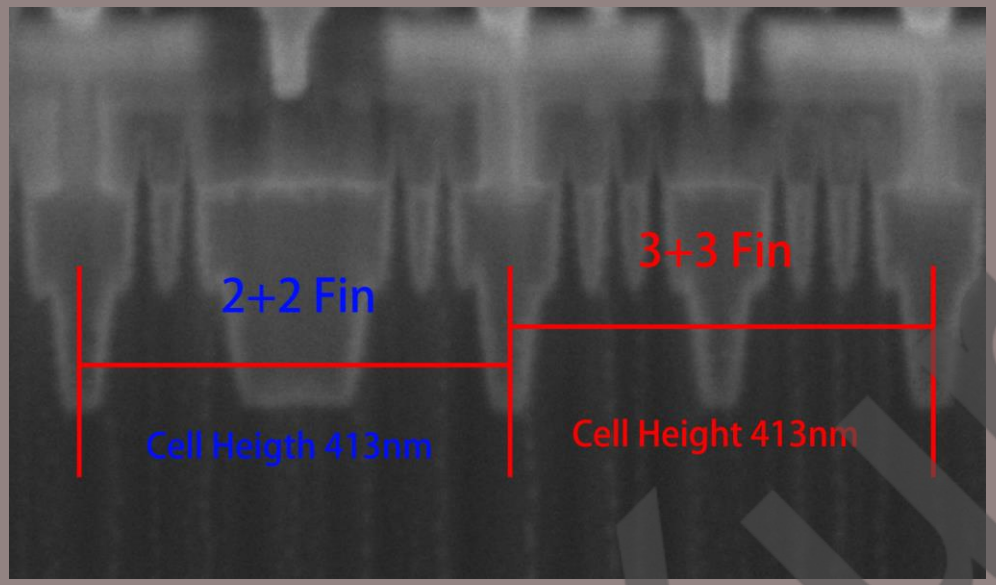
The 2lib Fin pitch both 42nm

GA107

Lib	T239	GA107
2+2 Fin Pitch	42nm	42nm
3+3 Fin Pitch	42nm	42nm

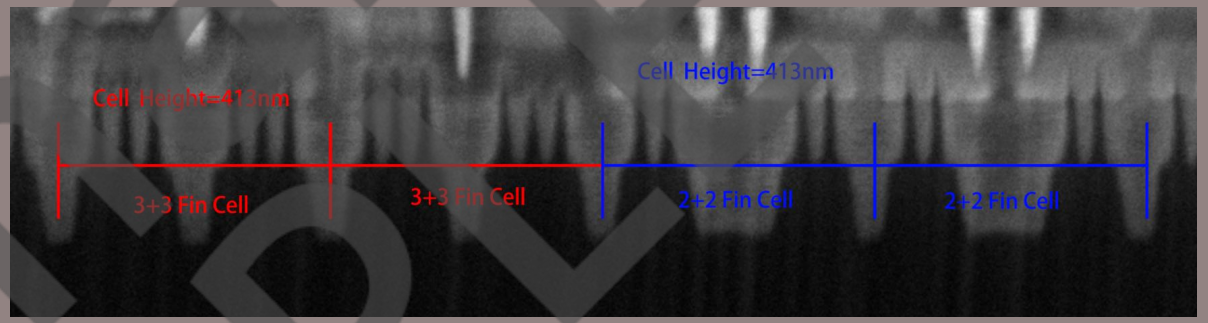
In the Fin cut,
Although GA107 and T239 are both dual-bank (2Fin/3Fin),
the Fin Pitch is same as 42nm.

T239 process identical-Fin cut



The 2 libs Cell Height both 413nm

T239



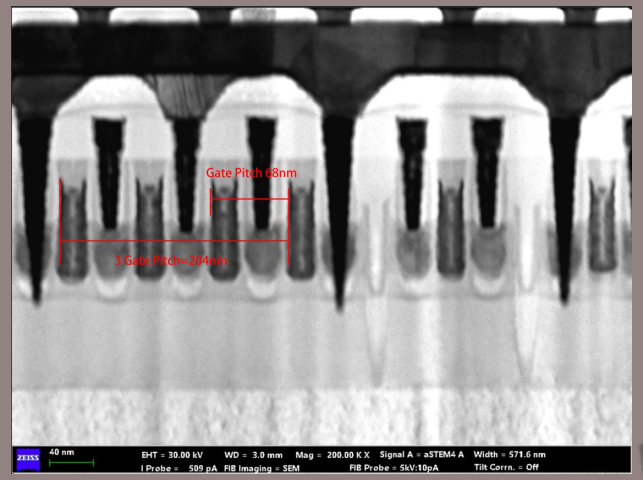
The 2 libs Cell Height both 413nm

GA107

Lib	T239	GA107
2+2 Cell Height	413nm	413nm
3+3 Cell Height	413nm	413nm

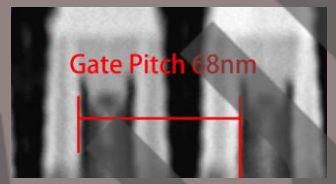
In the Fin cut,
Although GA107 and T239 are both dual-bank (2Fin/3Fin), the Cell Height is same as 413nm.

T239 process identical-Gate cut

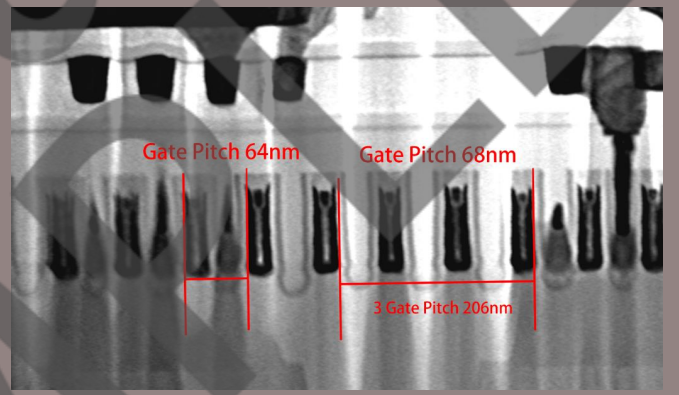


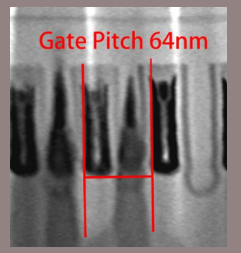
T239

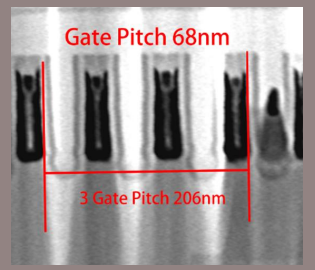
The Gate Pitch= 68nm



The Gate Pitch= 64nm/68nm







GA107

Lib	T239	GA107
Gate Pitch	68nm	64nm/68nm

GA107 and T239 both have the same 68nm Gate Pitch,
But GA107 has an additional 64nm Gate Pitch

T239 process identical-Metal layers

T239	Pitch	MMP
M1	68nm	Gate Pitch
M2	48nm	1x
M3	48nm	1x
M4	48nm	1x
M5	80nm	1.66x
M6	80nm	1.66x
M7	80nm	1.66x
M8	80nm	1.66x
M9	80nm	1.66x
M10	80nm	1.66x
M11	80nm	1.66x
M12	80nm	1.66x

T239 Metal Pitch

The Min Metal Pitch are all equal to 48nm
And the M2 Pitch are all equal to 48nm

GA107	Pitch	MMP
M1	68nm	Gate Pitch
M2	48nm	1x
M3	48nm	1x
M4	48nm	1x
M5	80nm	1.66x
M6	80nm	1.66x
M7	80nm	1.66x
M8	80nm	1.66x
M9	80nm	1.66x
M10	80nm	1.66x
M11	80nm	1.66x
M12	80nm	1.66x

GA107 Metal Pitch

T239 process identical-Total

T239	Data
Fin Pitch	42nm
Fin number	2+2/3+3
Gate Pitch	68nm
Gate Element	HKMG(W)
2+2 Cell Height	413nm
3+3 Cell Height	413nm
Diffusion Break	MDB
Contact	SAC
Contact Element	W

T239 data

The Min Metal Pitch are all equal to 48nm
And the M2 Pitch are all equal to 48nm

GA107	Data
Fin Pitch	42nm
Fin number	2+2/3+3
Gate Pitch	64nm/68nm
Gate Element	HKMG(W)
2+2 Cell Height	413nm
3+3 Cell Height	413nm
Diffusion Break	MDB
Contact	SAC
Contact Element	W

GA107 Data

T239 process identification-summary

Samsung 8N

Samsung	10LPE/LPP	8LPP/LPU	T239	GA107
Fin/GAA	3 Fin	3+2 Fin	3+2 Fin	3+2 Fin
Track	8.75T	8.59T	8.6T	8.6T
Gate Pitch	68nm	64nm/68nm	68nm	64nm/68nm
Fin Pitch	42nm	42nm	42nm	42nm
Min MP	48nm	44nm	48nm	48nm
M2P	48nm	44nm	48nm	48nm
Cell H (Min)	420nm	378nm	413nm	413nm
SDB/DDB	SDB	SDB	SDB	SDB
CB-RX	SAC	SAC	SAC	SAC
Logic Density (MTr)	51.6Mtr/mm2	60.92/Mtr/mm2	52.47Mtr/mm2	55.75Mtr/mm2

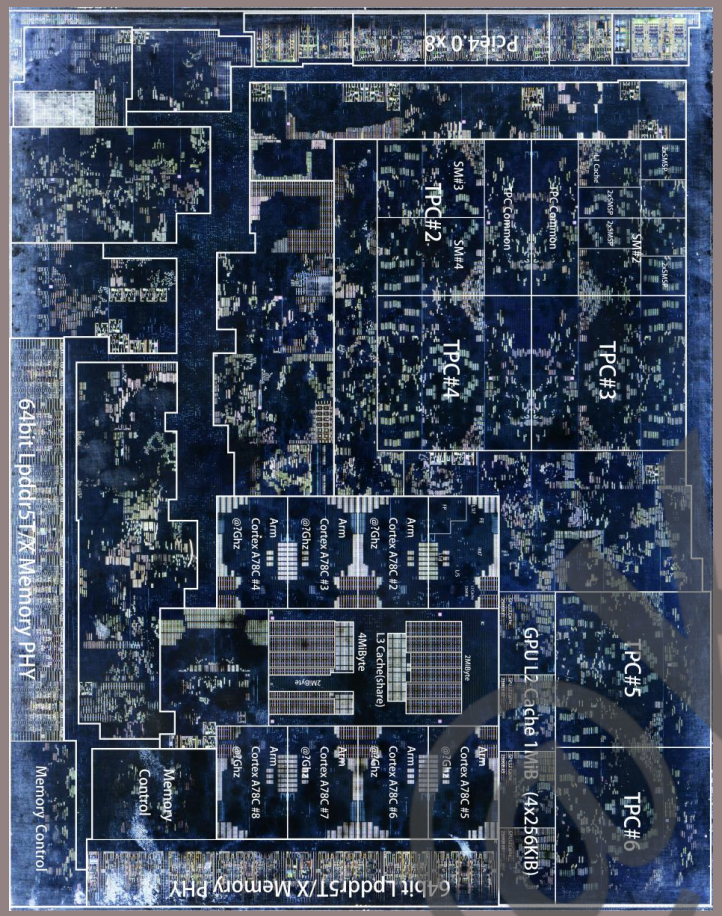
T239 uses the same Samsung 8N process as GA107.

Samsung 8N is a derivative of Samsung 10LPP

Which includes some of the process features of 8LPP (such as 2+2Fin),

But it is not completely equal to Samsung 8LPP

T239 process identification-summary



Diesize=207.35 mm2

In sealring area=202.4mm2

IO PHY(LPDDR) area 7.2x2=14.4mm2
IO PHY(PCIE)area=5.557mm2
IO PHY USB …area=1.085mm2

Only Logic area=181.358mm2

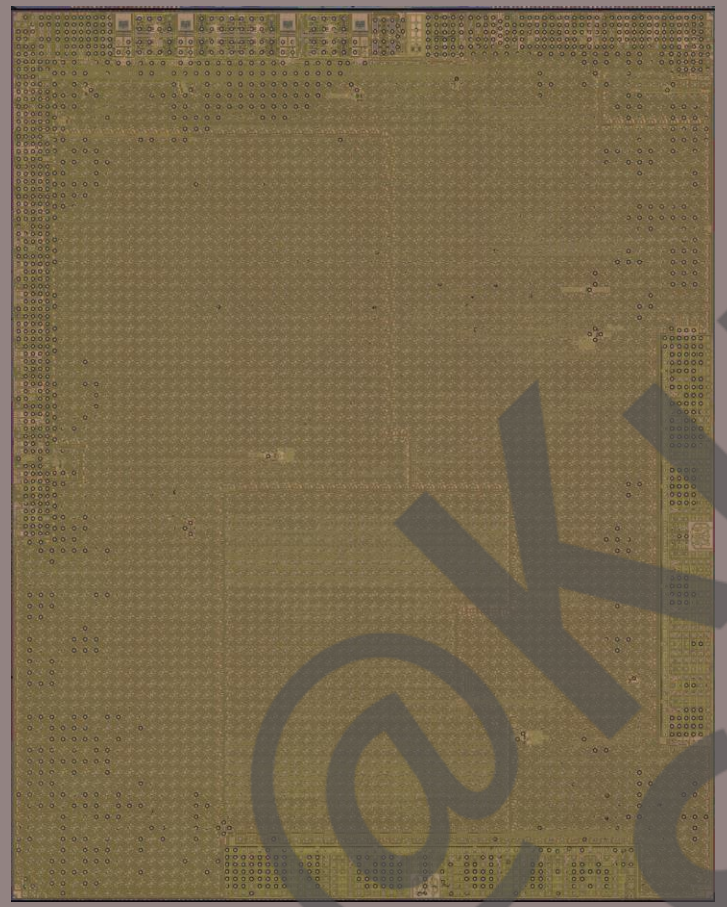
Maximum have: 10.88billion (108.79亿)Transistors
Minimum have: 9.516Billion (95.158亿)Transistors

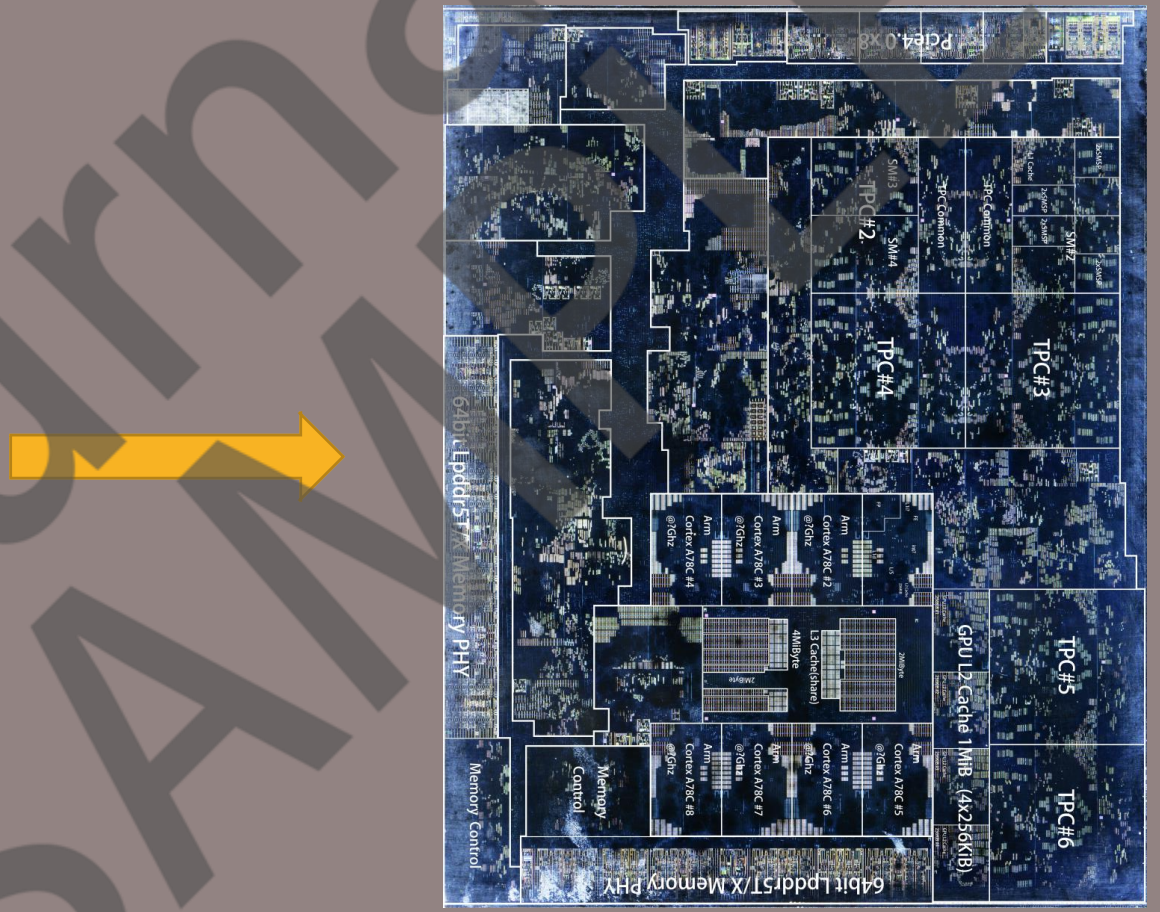
Samsung	T239
Fin/GAA	3+2 Fin
Track	8.6T
Gate Pitch	68nm
Fin Pitch	42nm
Min MP	48nm
M2P	48nm
Cell H (Min)	413nm
SDB/DDB	SDB
CB-RX	SAC
Logic Density (MTr)	52.47Mtr/mm2

Switch2 soc analyze

Dieshot analyze

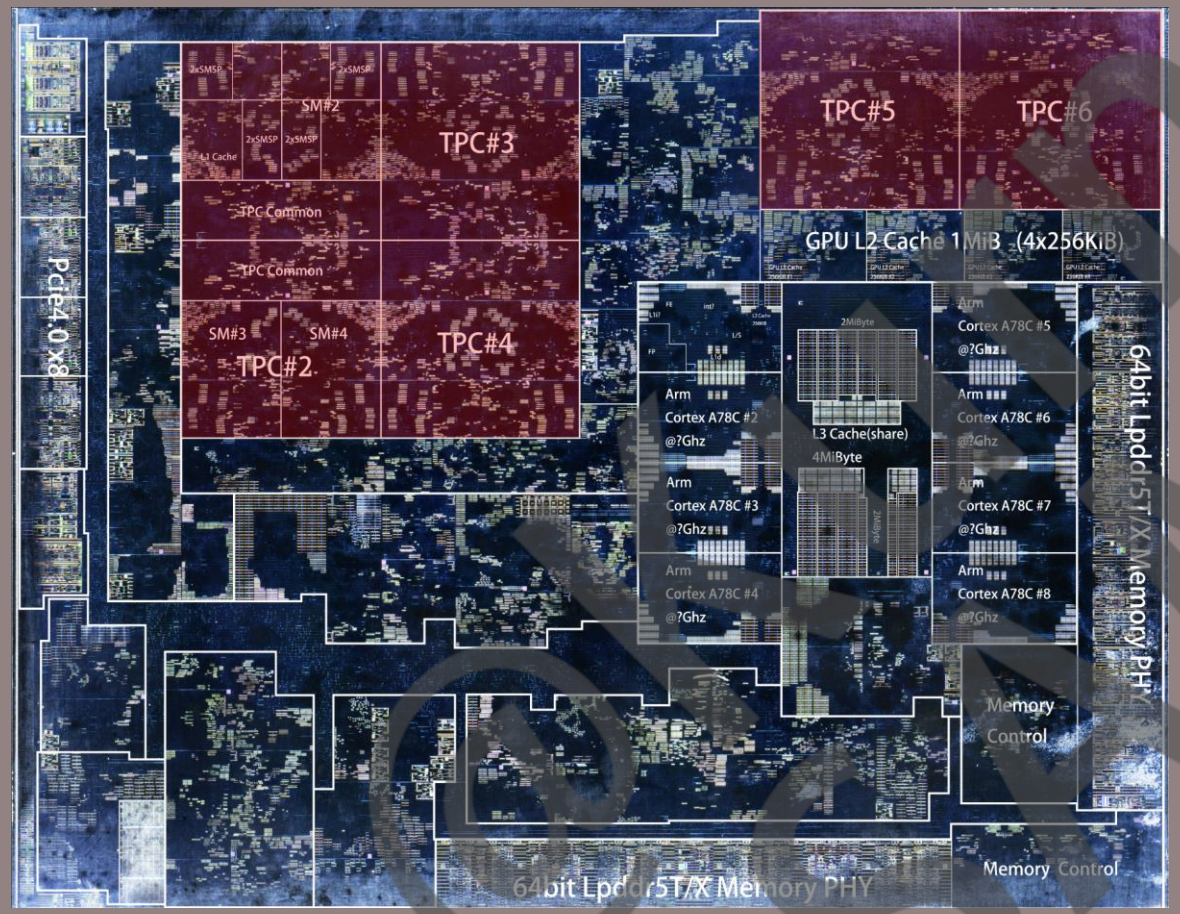
T239 Die shot analyze





T239 Die shot analyze

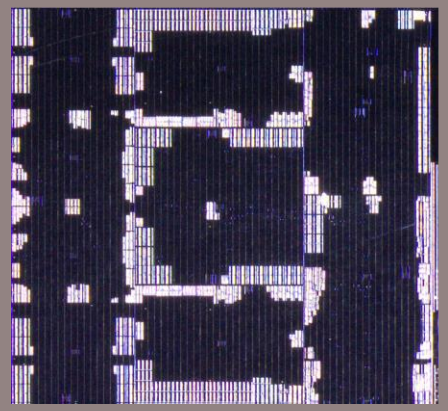
T239 Die shot analyze-GPU



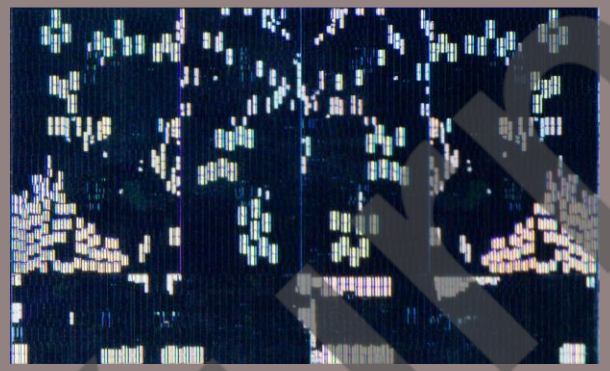
The T239 have 6 TPC GPU
1 TPC have 2 SM
1 SM have 128Cuda cores

So T239 GPU have 1536 Cuda cores

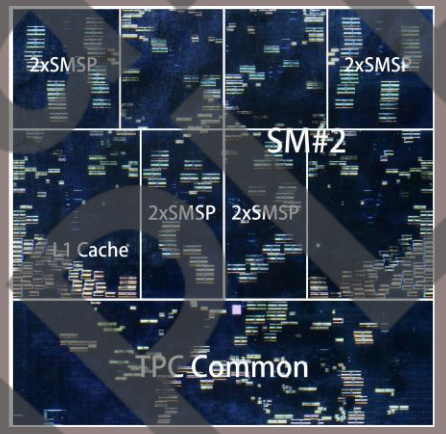
T239 Die shot analyze-GPU



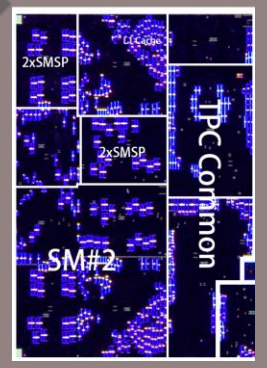
GA102



Orin



T239

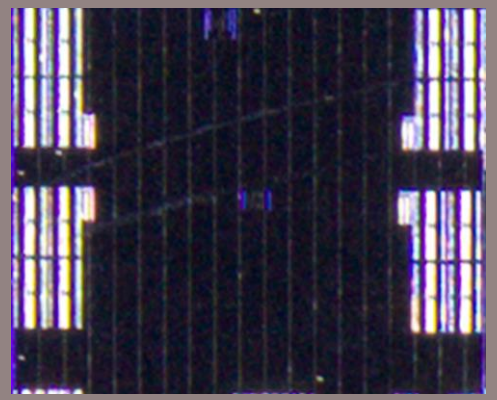


AD102

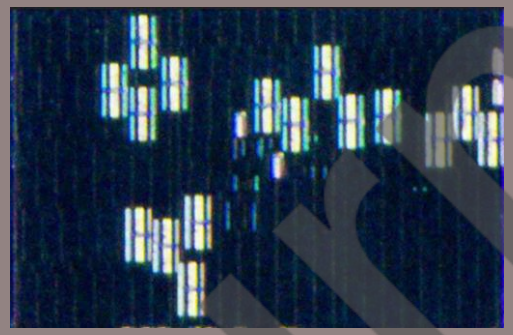
For TPC, although GA102/Orin/T239 all belong to the Nvidia Ampere family, it is obvious that the layout is inconsistent.

Orin and T239 GPUs are more similar to Nvidia's Ada layout

T239 Die shot analyze-GPU

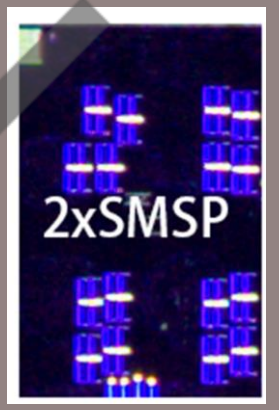


GA102 SMSP



Orin SMSP

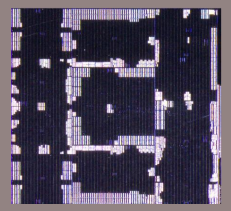
T239 SMSP



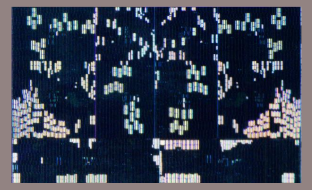
AD102 SMSP

Especially the layout inside SM, are more are more similar to Nvidia's Ada layout

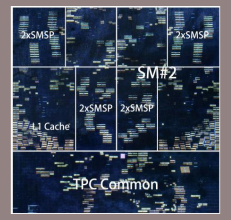
T239 Die shot analyze-GPU



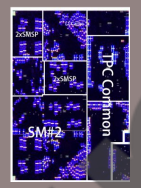
GA102



Orin

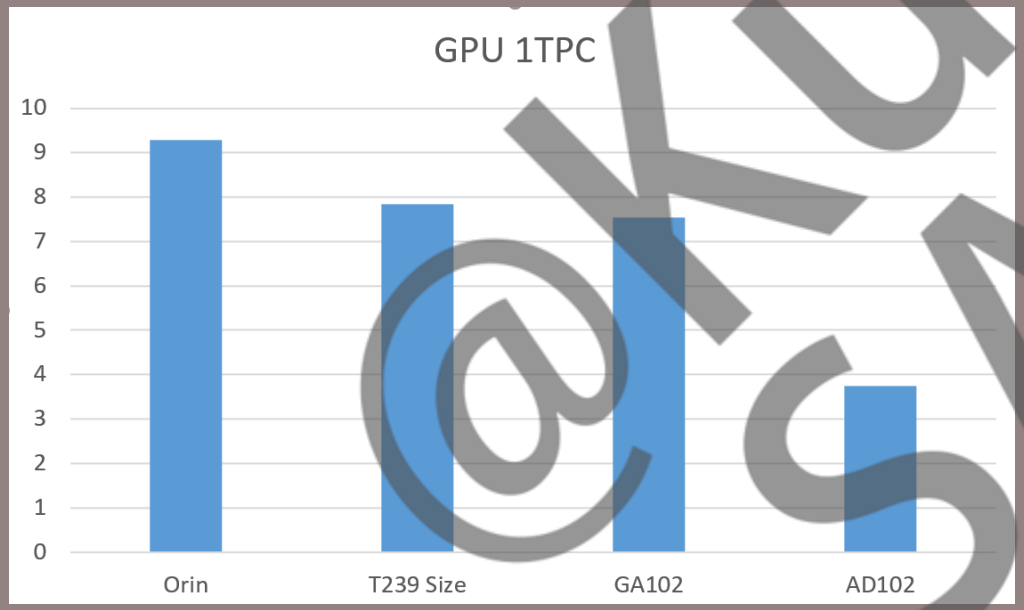


T239



AD102

The three figures on the left
are the same architecture (Nvidia Ampere)
implemented in the same process (Samsung 8N)
The 4th figure shows Nvidia Ada implemented in TSMC N4

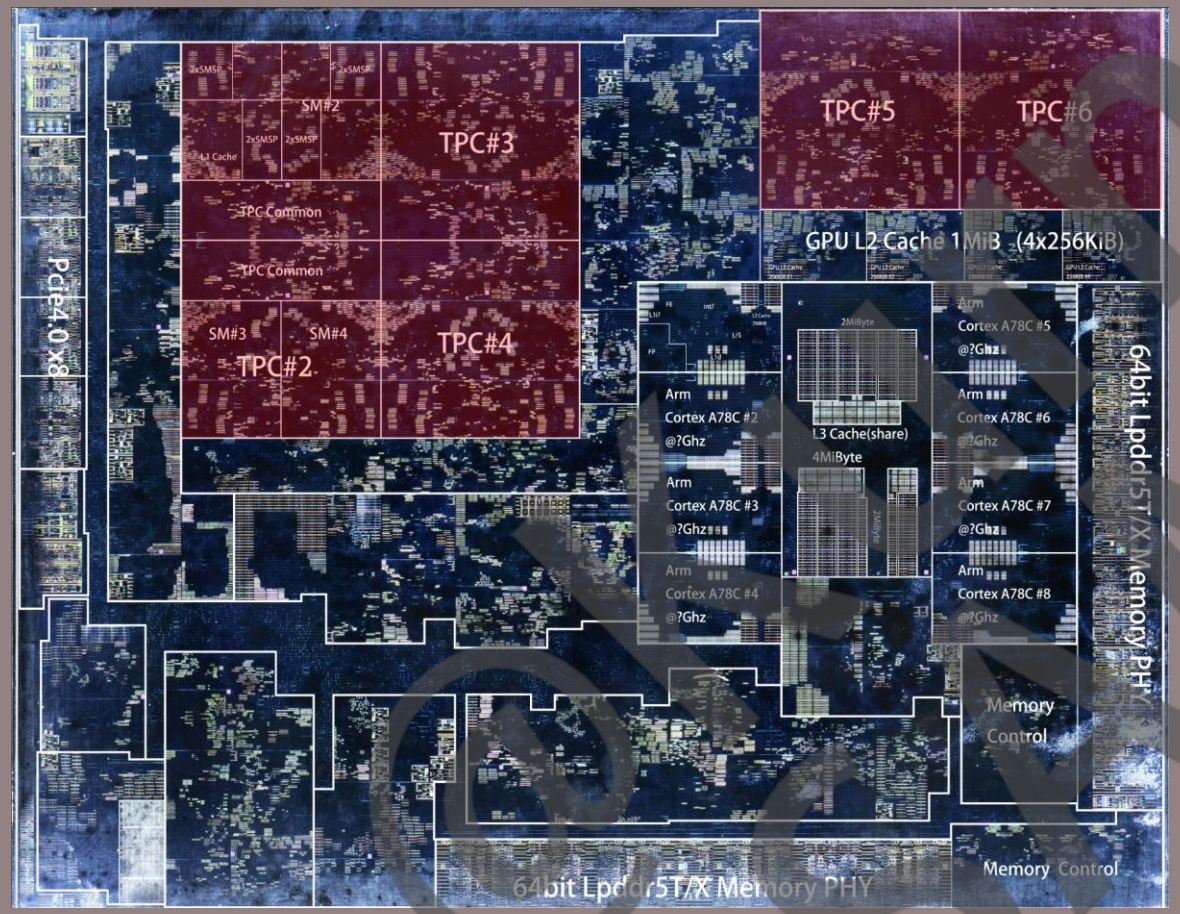


	Orin	T239 Size	GA102	AD102
GPU 1TPC	9.29	7.83	7.542	3.7365
GPU 1SM	3.47	2.71	2.57	1.2

But according to TPC internal mapping data,
it is clear that Orin has the largest GPU TPC/SM area,
followed From T239, and then GA102

The area of the AD102 using advanced technology
is almost half of that of the GA102.

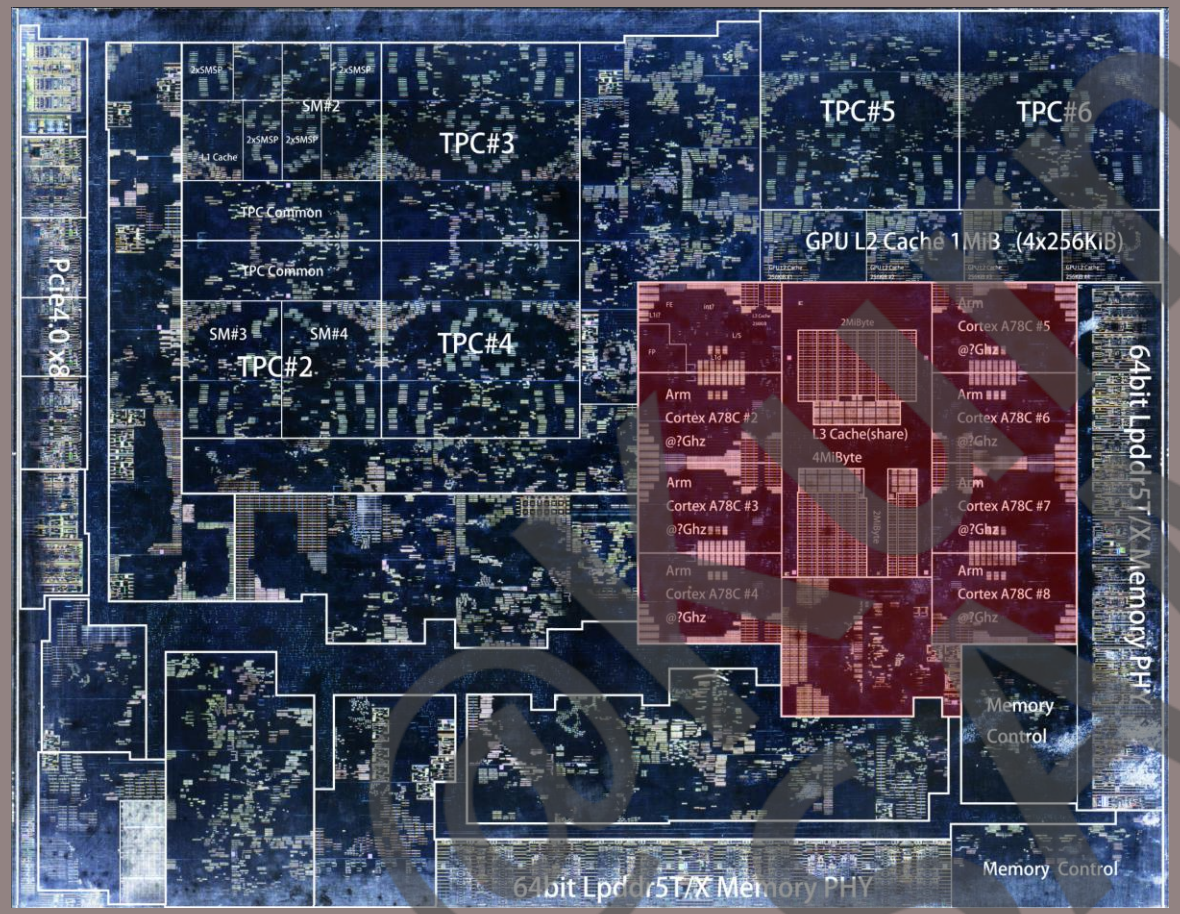
T239 Die shot analyze-GPU



T239 Size	
GPU All	88.349
GPU 1TPC	7.83
just TPC	46.98
GPU 1SM	2.71
GPU 2XSM	0.592

Some size data in this graph

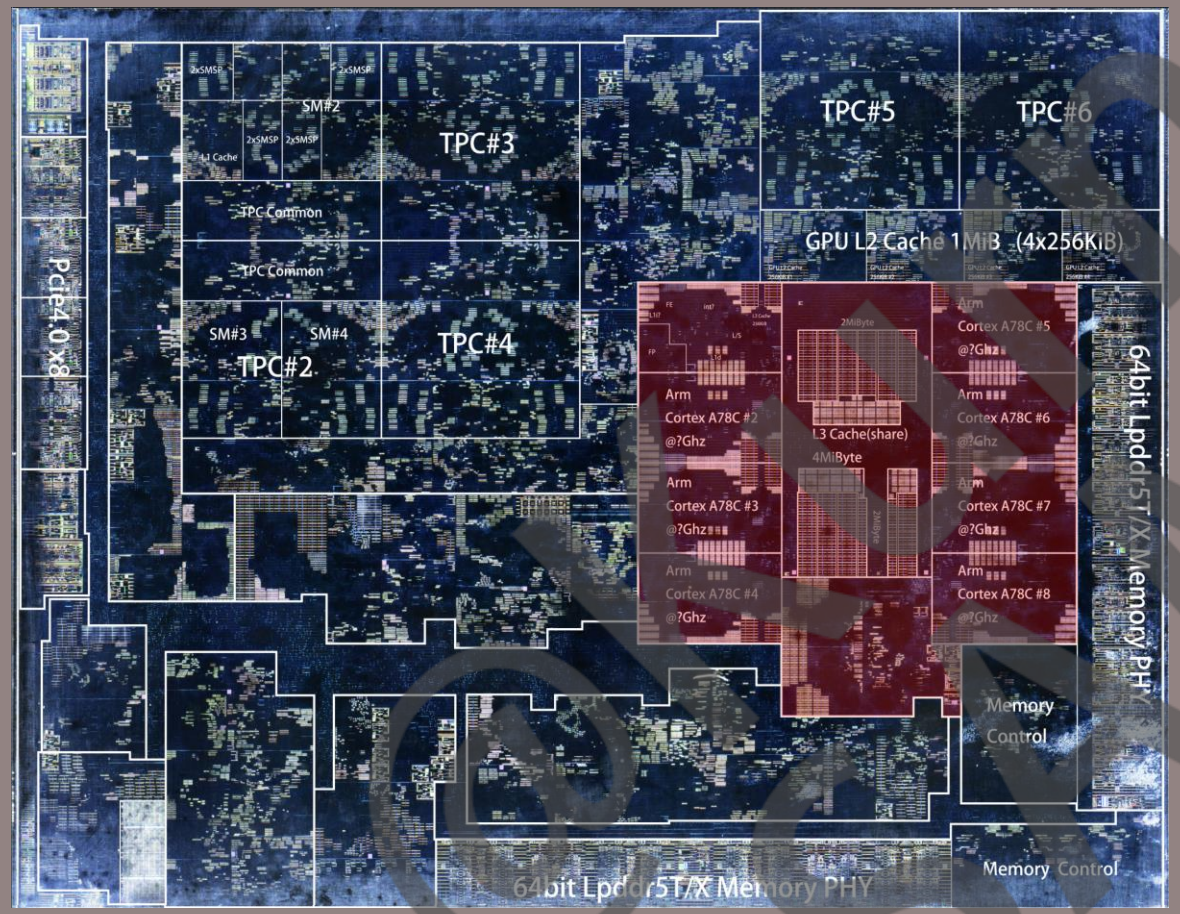
T239 Die shot analyze-CPU



This area is CPU Cluster

Have 8 Arm A78C Core

T239 Die shot analyze-CPU



Nvidia Orin

T239

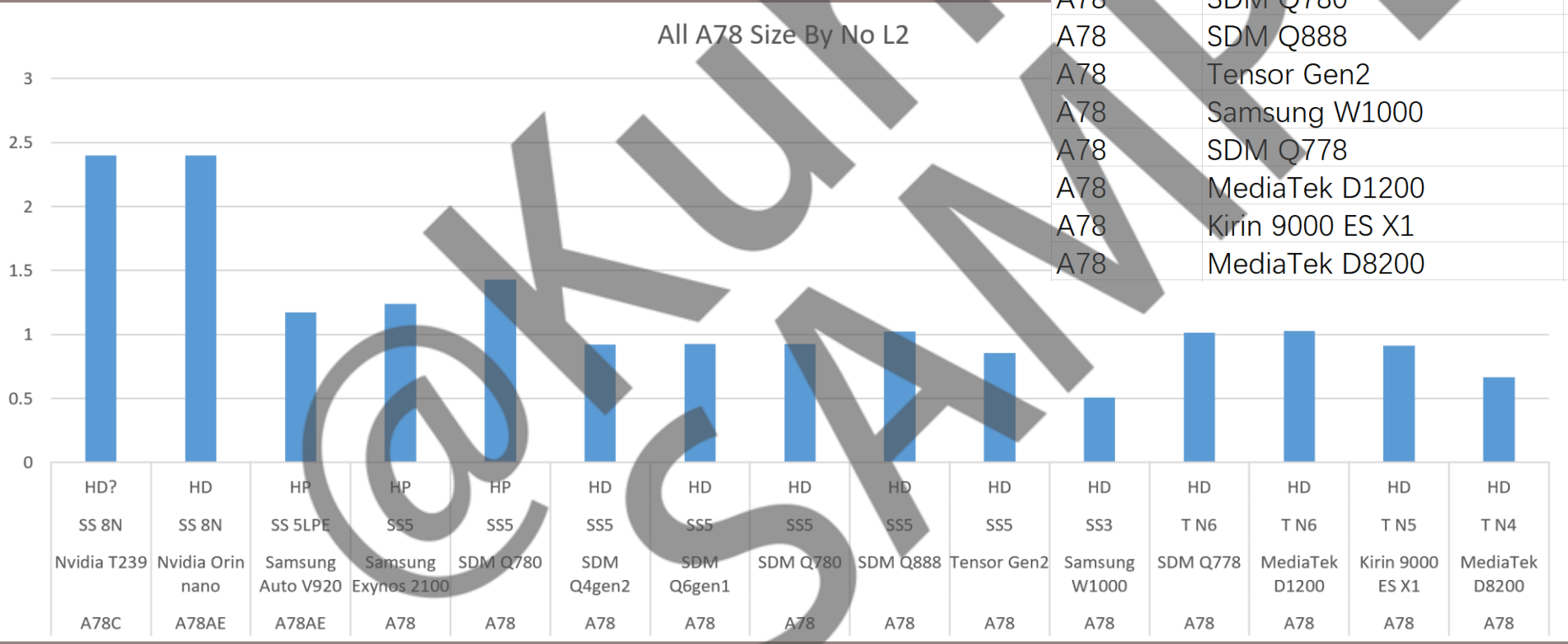
A78AE A78C

Orin		T239 Size	
CPU+L2	2.6	CPU+L2	2.56
CPU Only	2.4	CPU Only	2.4

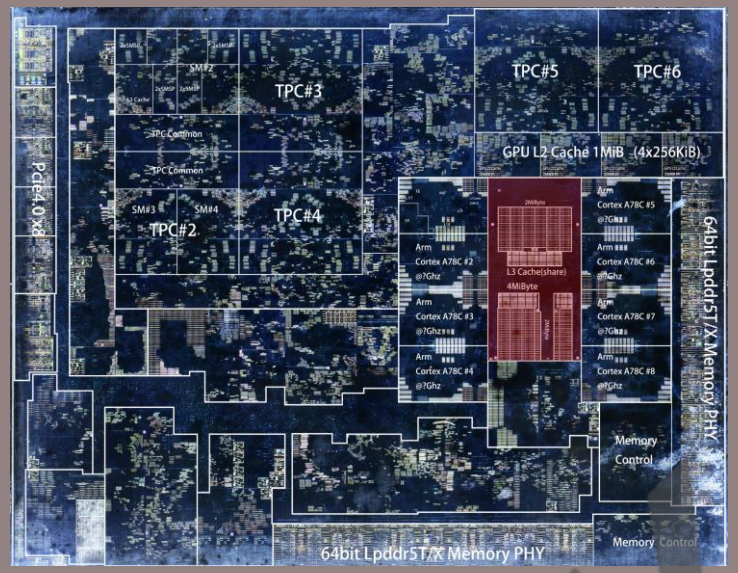
The Orin A78AE Core size is the same as T239 A78C Core size

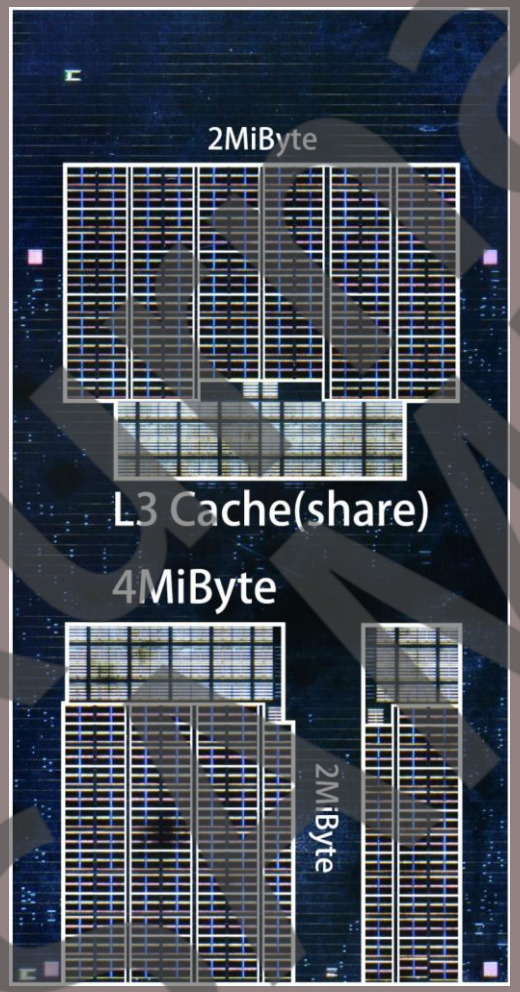
Some A78 sizes in different processes

IP	Name	Process	Lib	size （No L2）
A78C	Nvidia T239	SS 8N	HD?	2.4
A78AE	Nvidia Orin nano	SS 8N	HD	2.4
A78AE	Samsung Auto V920	SS 5LPE	HP	1.174
A78	Samsung Exynos 2100	SS5	HP	1.238
A78	SDM Q780	SS5	HP	1.427
A78	SDM Q4gen2	SS5	HD	0.921
A78	SDM Q6gen1	SS5	HD	0.926
A78	SDM Q780	SS5	HD	0.925
A78	SDM Q888	SS5	HD	1.021
A78	Tensor Gen2	SS5	HD	0.853
A78	Samsung W1000	SS3	HD	0.507
A78	SDM Q778	T N6	HD	1.015
A78	MediaTek D1200	T N6	HD	1.028
A78	Kirin 9000 ES X1	T N5	HD	0.913
A78	MediaTek D8200	T N4	HD	0.667



T239 Die shot analyze-CPU





This area is CPU L3 Cache

In total there are
2x2MiB=4MiB of L3 cache shared by 8 cores.

Based on the shared L3 design,
we can confirm that those CPUs are A78C cores.

A78:1-8Core/cluster
A78AE:1-4Core/cluser
A78C:8Core/Cluster

Chip price and IF line

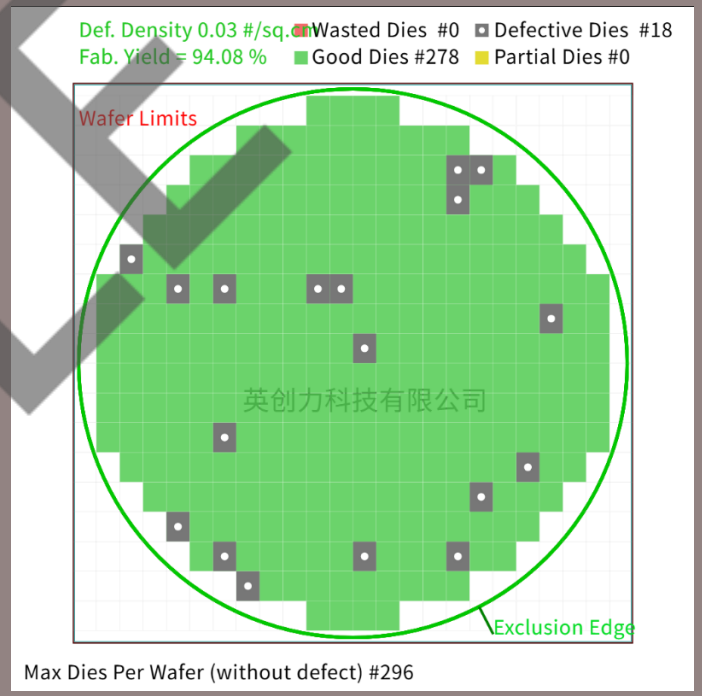
T239 Price with IF Line

T239 Price

Diesize: 207.35mm2
(12.76mm x 16.25mm)

DPW Nb: 296

D0(if)=0.03
Yield=94.08%



We know the Chip Process is Samsung 8N
For that, We can know the Chip Price

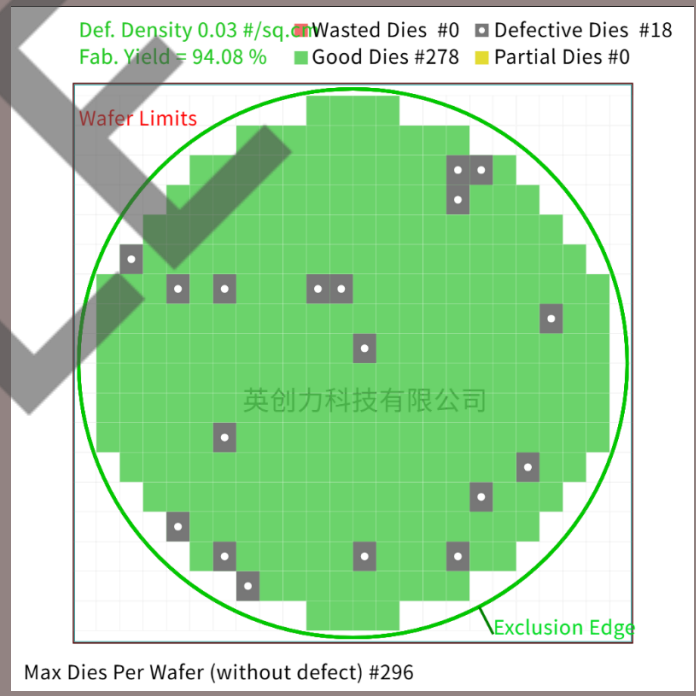
T239 Price

Table 9: Calculation of foundry sale price per chip in 2020 by node

Line	Node (nm)	90	65	40	28	20	16/12	10	7	5
1	Mass production year and quarter[220]	2004 Q4	2006 Q4	2009 Q1	2011 Q4	2014 Q3	2015 Q3	2017 Q2	2018 Q3	2020 Q1
2	Capital investment per wafer processed per year	$4,649	$5,456	$6,404	$8,144	$10,356	$11,220	$13,169	$14,267	$16,746
3	Net capital depreciation at start of 2020 (25.29% / year)	65%	65%	65%	65%	65%	65%	55.1%	35.4%	0.0%
4	Undepreciated capital per wafer processed per year (remaining value at start of 2020)	$1,627	$1,910	$2,241	$2,850	$3,625	$3,927	$5,907	$9,213	$16,746
5	Capital consumed per wafer processed in 2020	$411	$483	$567	$721	$917	$993	$1,494	$2,330	$4,235
6	Other costs and markup per wafer	$1,293	$1,454	$1,707	$2,171	$2,760	$2,990	$4,498	$7,016	$12,753
7	Foundry sale price per wafer	$1,650	$1,937	$2,274	$2,891	$3,677	$3,984	$5,992	$9,346	$16,988
8	Foundry sale price per chip	$2,433	$1,428	$713	$453	$399	$331	$274	$233	$238

Yield=94.8%
D0=0.03
Wafer Price=5992USD

Die price =21.517USD

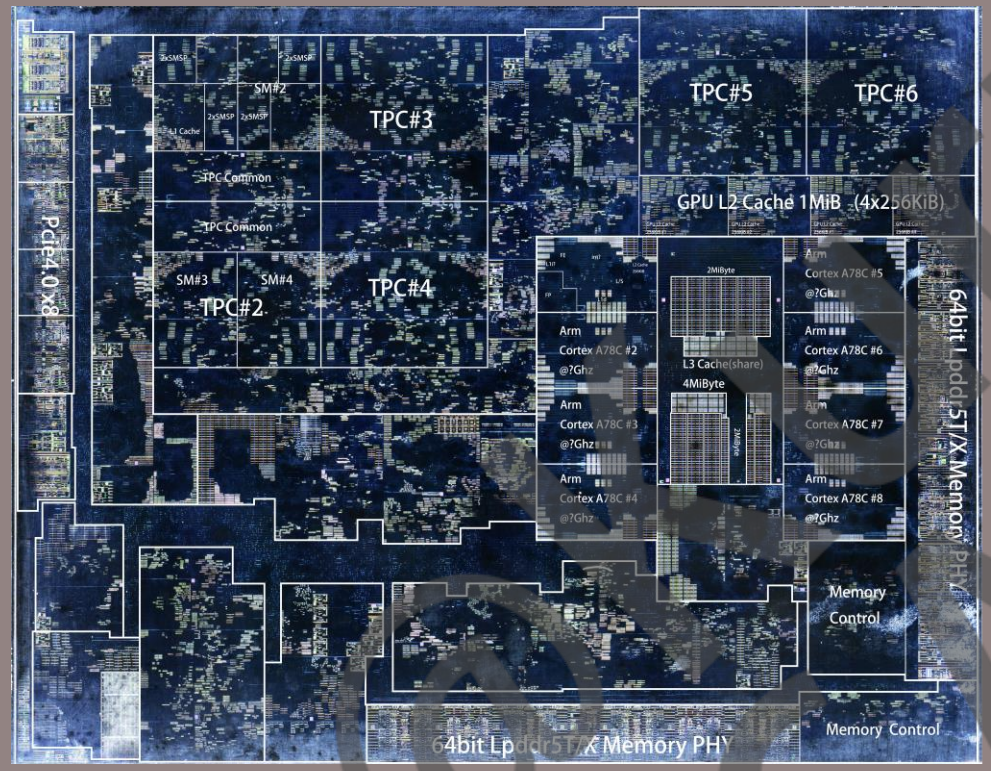


Max Dies Per Wafer (without defect) #296

T239 IF line

Diesize: 207.35mm2

(12.76mm x 16.25mm)



Diesize<100mm2

What if just a joke

If Nvidia T239 used TSMC N4
What is the area of this die?
Estimated to be within 100mm2