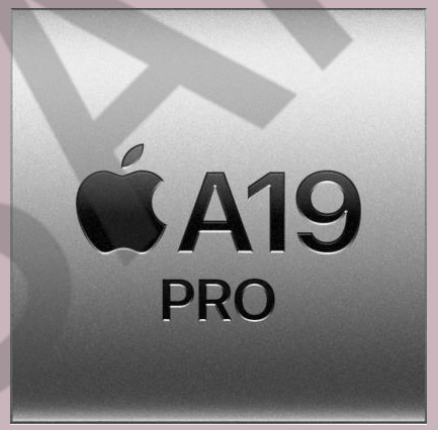
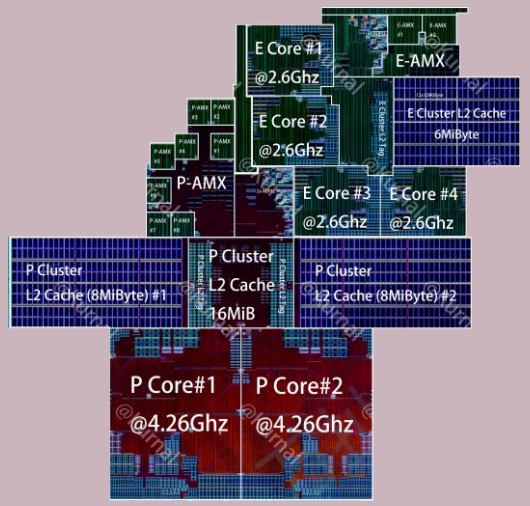
APPLE A19Pro

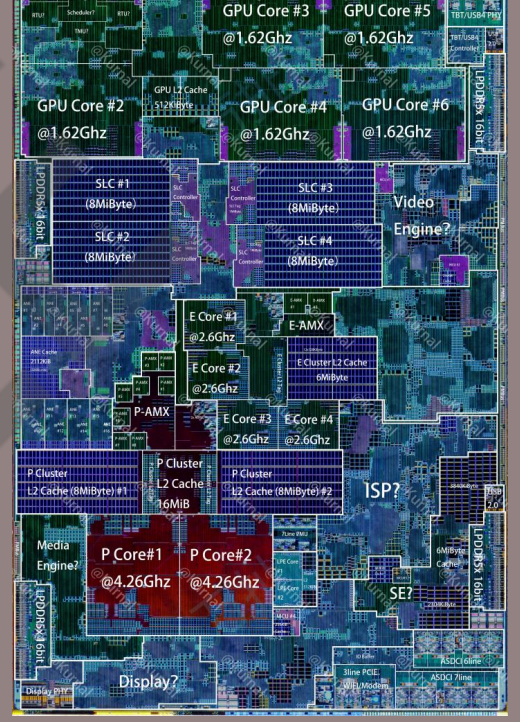
On Chip analyze

V0

@Kurnal







Version of this Report

Version	Date	Updates	Author
V0.1	2025/12/06 19: 05	Working	Kurnal
V1.0	2025/12/20 19:46	Finish	Kurnal

About Authors

This Report is made From @Kurnal

BiliBili: @Kurnal
X: @Kurnalsalts
WeChat: KurnalWeChat

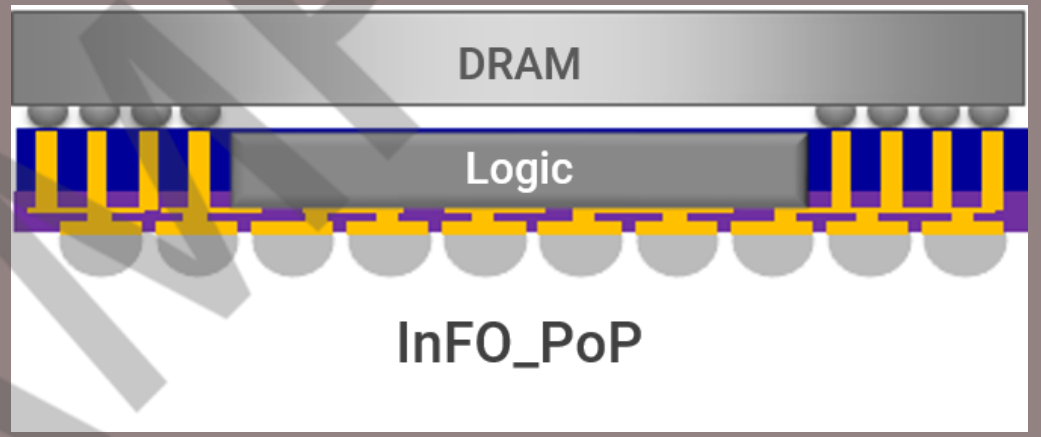
Package analyze

Apple A19Pro

Package analyze

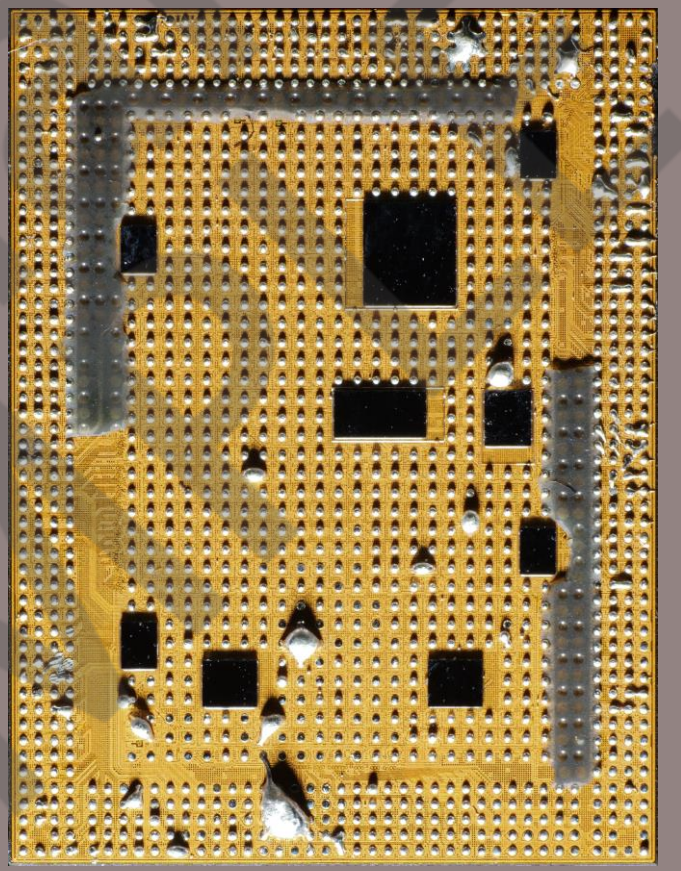
Package Frontside

Package Type: TSMC Info-PoP
Package size: 16.00mm x 12.60mm
Package thickness: 0.95mm



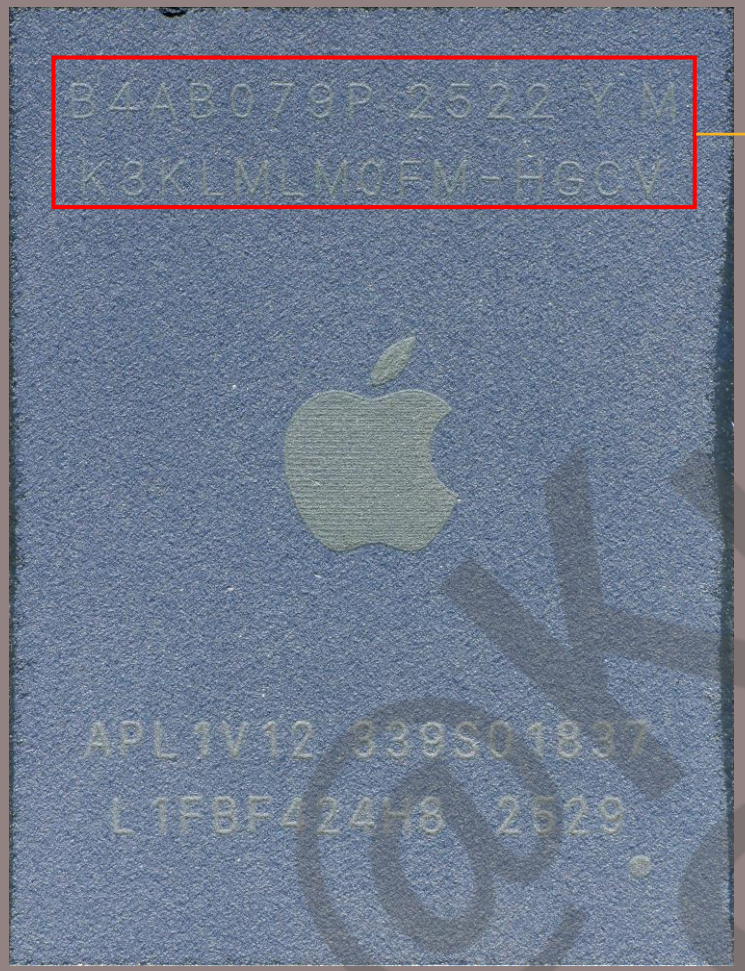
Package analyze

Package Frontside



Package Backside

Package analyze-Die mark



Package Frontside

B4AB079P-2522Y M
K3KLMLM0FM-HGCV

2522: Year 2025,Week 22

K3KLMLM0FM: Samsung 12GB LPDDR5X

Package analyze-Die mark

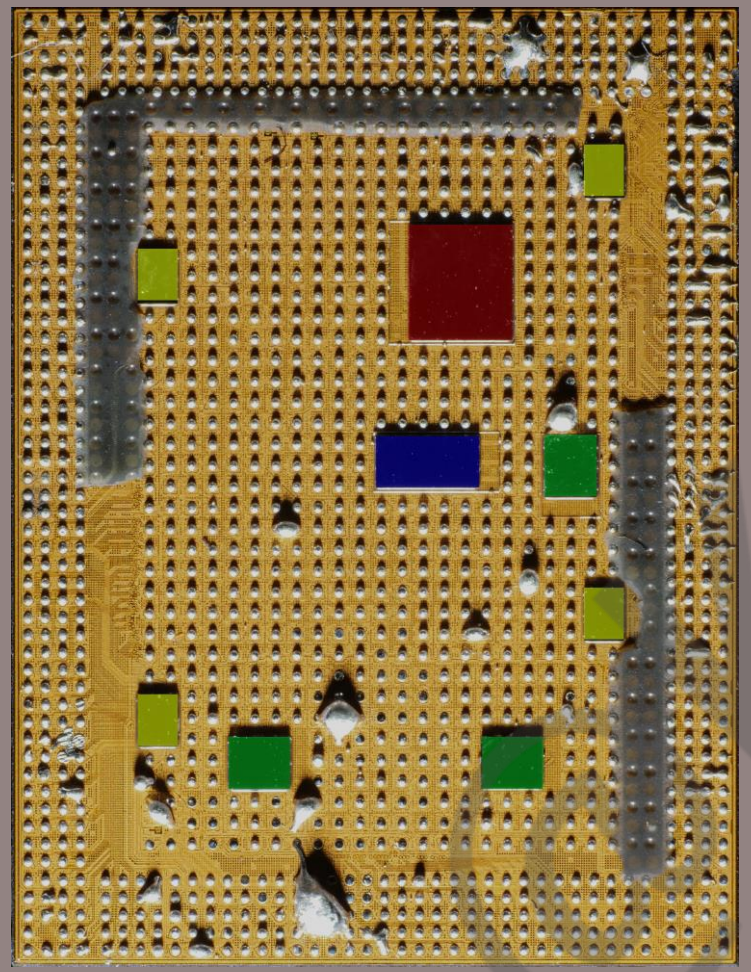
Package Frontside

APL1V12 339S01837
L1FBF424H8 2529

Product name: APL 1V12

Made/Package data: Year 2025 Week 29

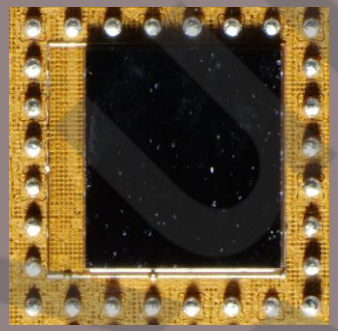
Package analyze



Package Backside

IPDS Type number: 4
IPDs Number: 9

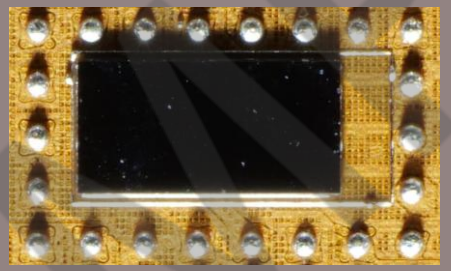
IPDs #1



Size: 1.91 x 1.78

Nb: 1

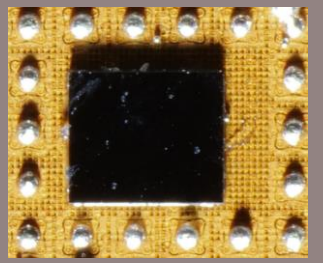
IPDs #2



Size: 0.86 x 1.78

Nb: 1

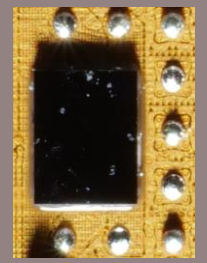
IPDs #3



Size: 0.90 x 1.02

Nb: 3

IPDs #4



Size: 0.70 x 0.86

Nb: 4

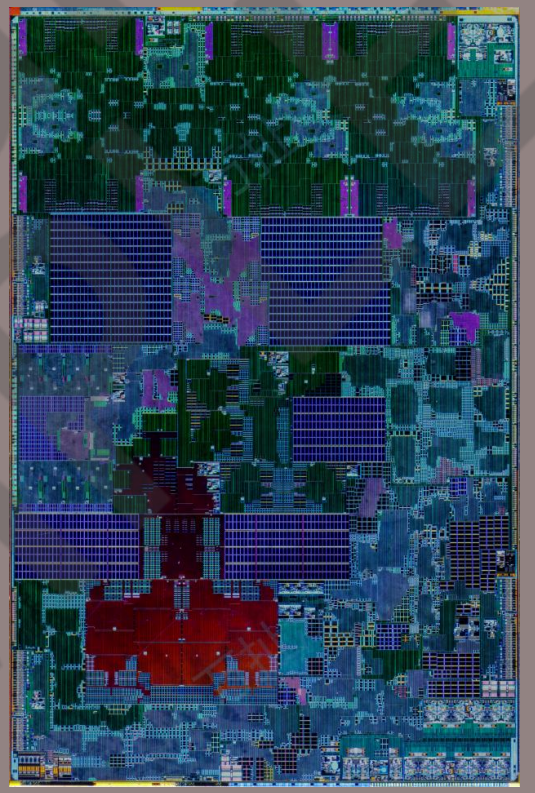
Decaped

A19 Pro

Chip analyze

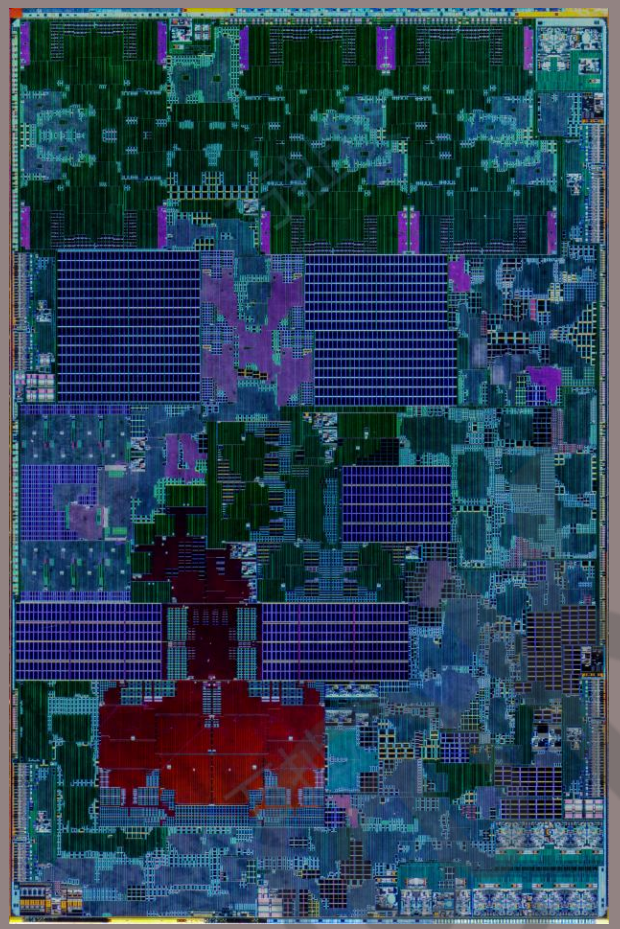
Package Frontside

Decaped



Die shot pics

Chip analyze



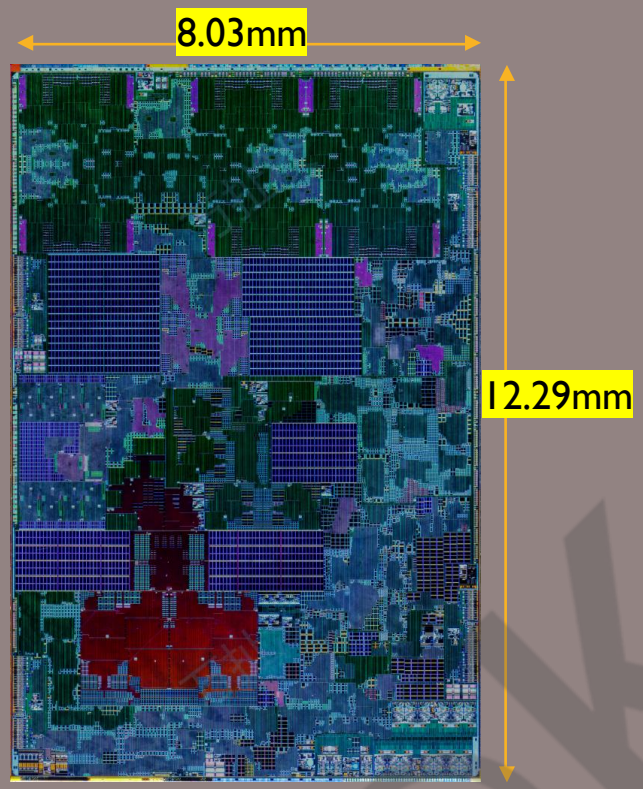
Die shot pics

Die size: 98.69mm2
Die Thickness: 230um

Die Mark : TM UA28

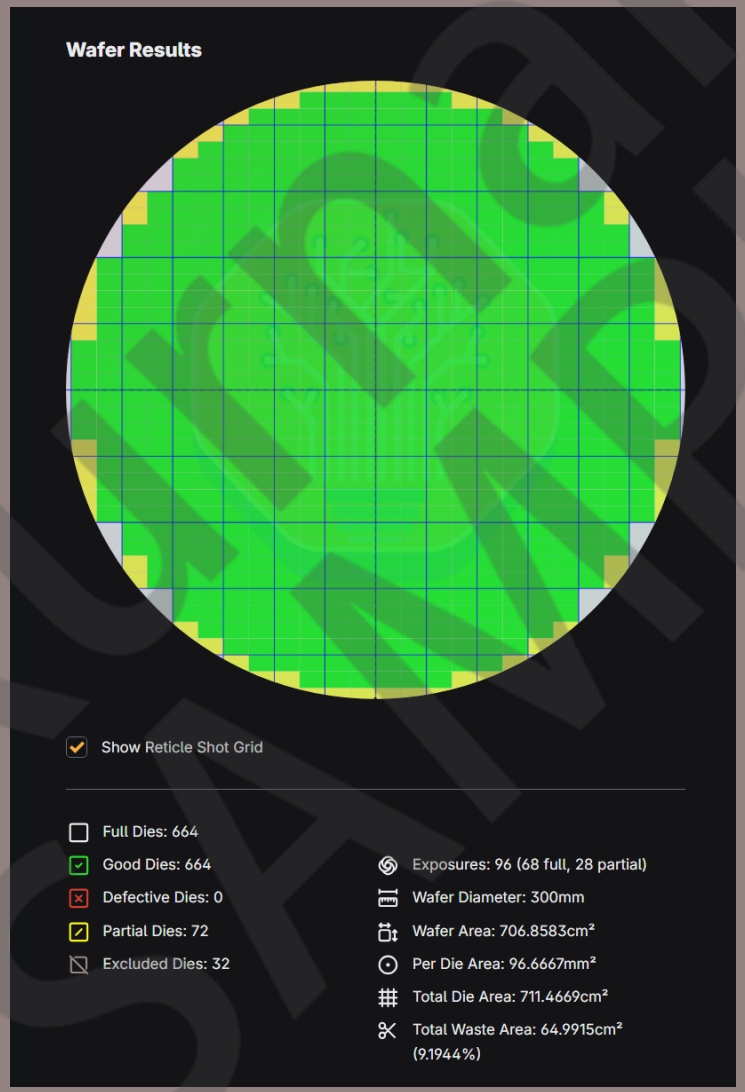
TSMC Tap Out Mark
Tap Out in year 2025

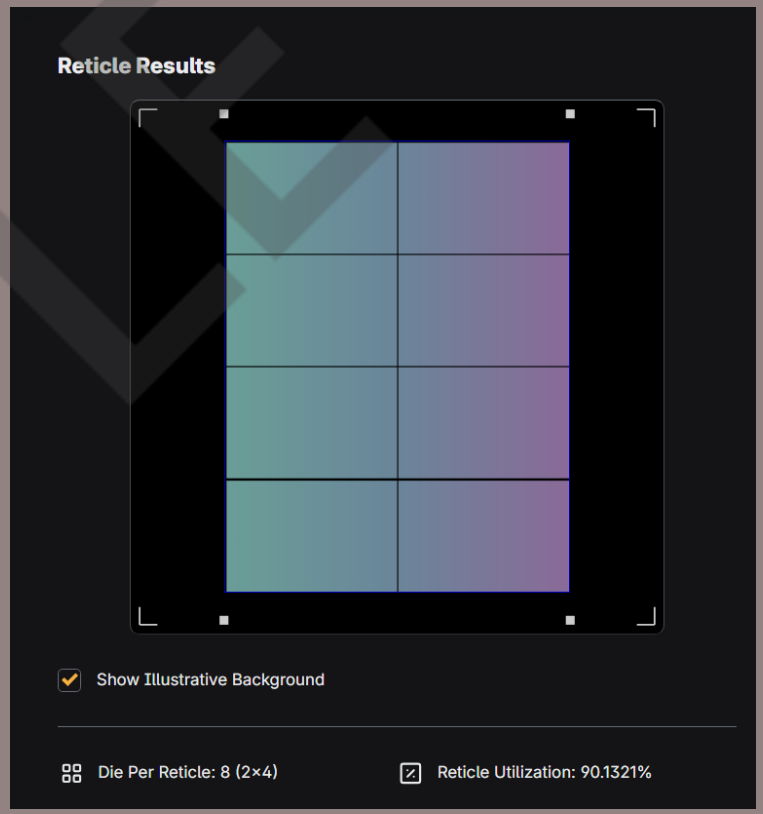
Chip analyze- Die Per Wafer/Mask



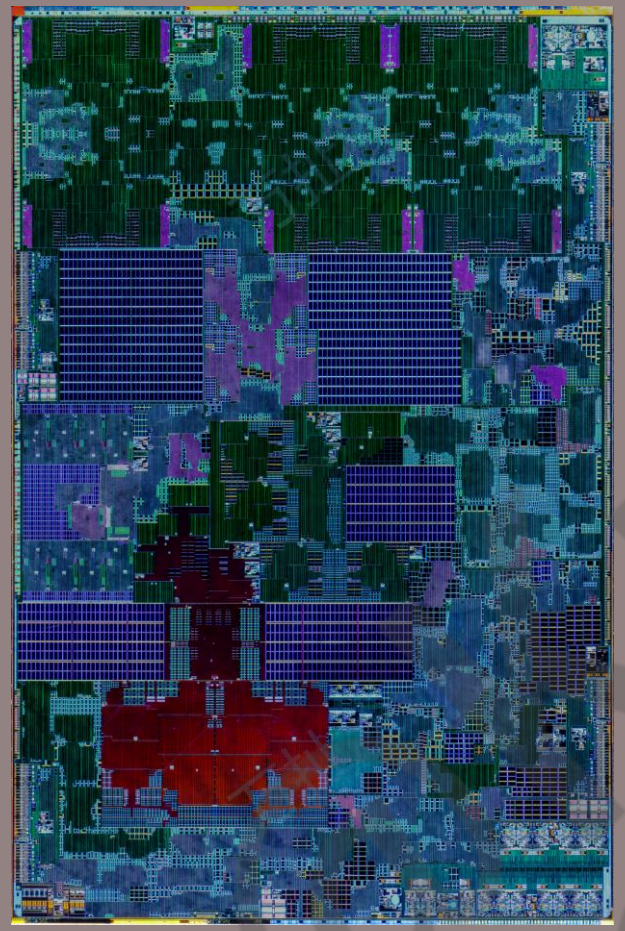
Die shot pics

Die size: 98.69mm2
Die Per Wafer: 664
Die Per Mask: 8:1



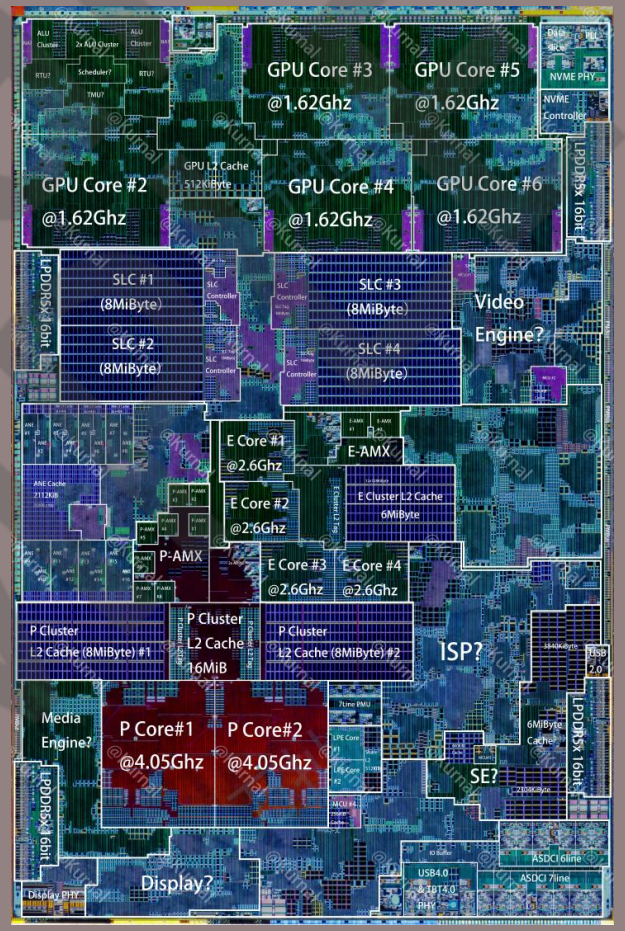


Chip analyze



Die Shot

Layout



Die Shot

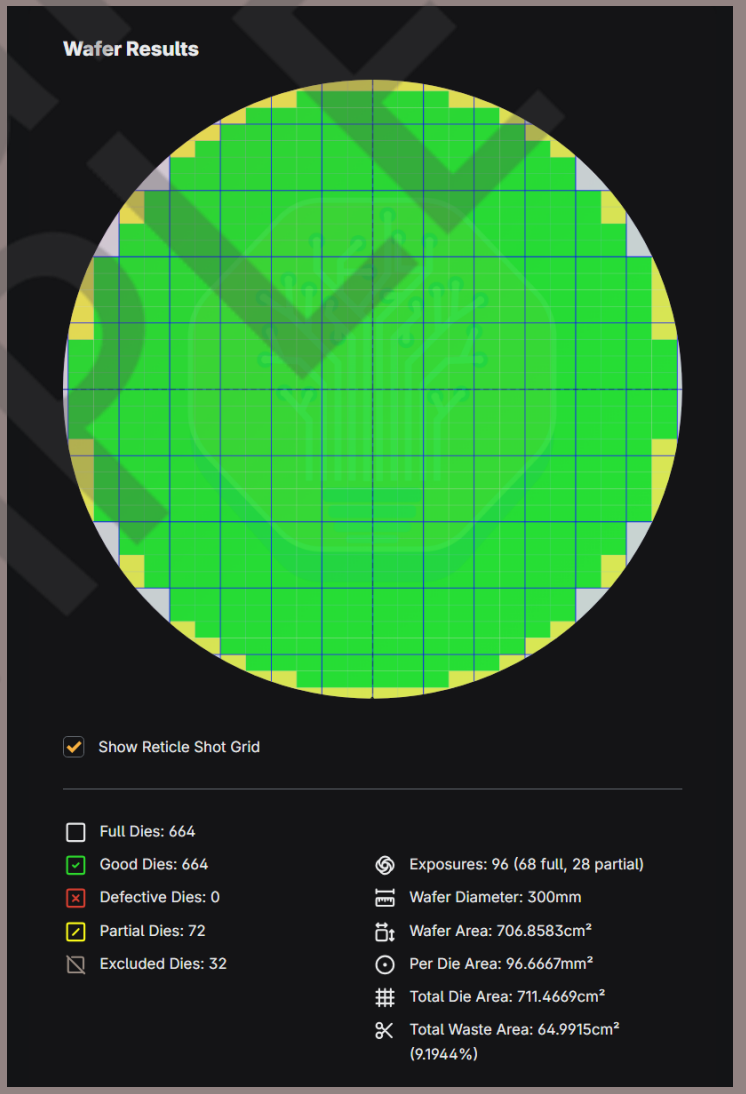
Price and Yield

Apple A19 Pro

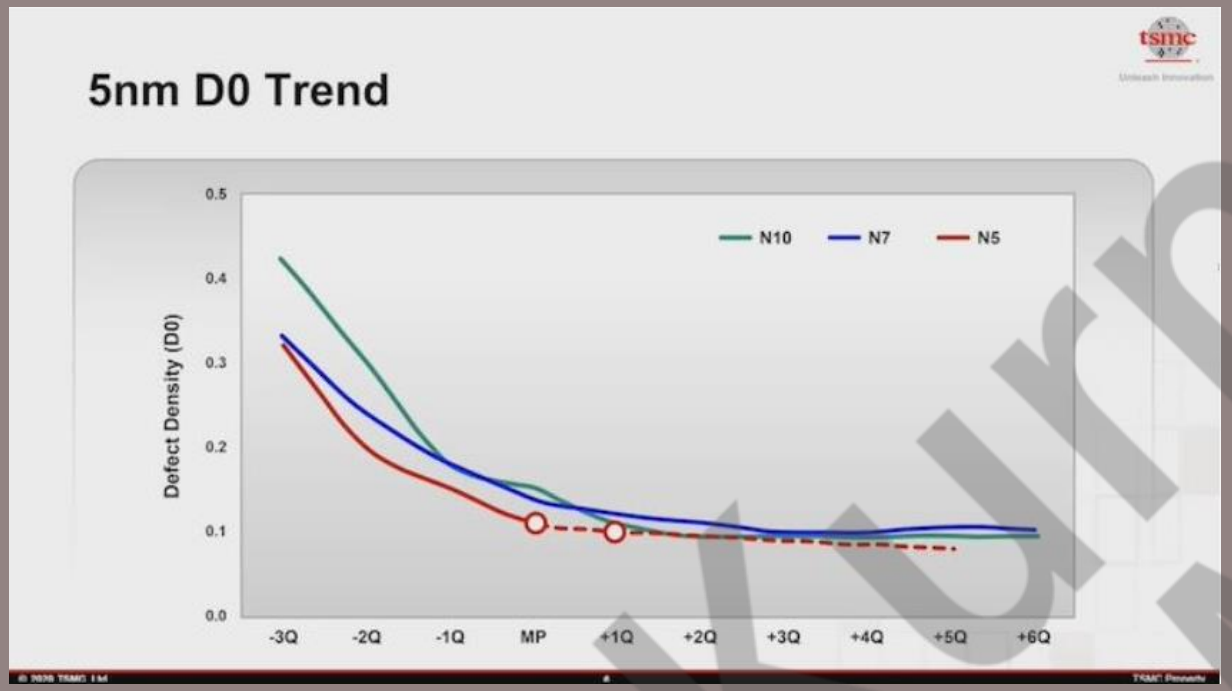
Price and Yield

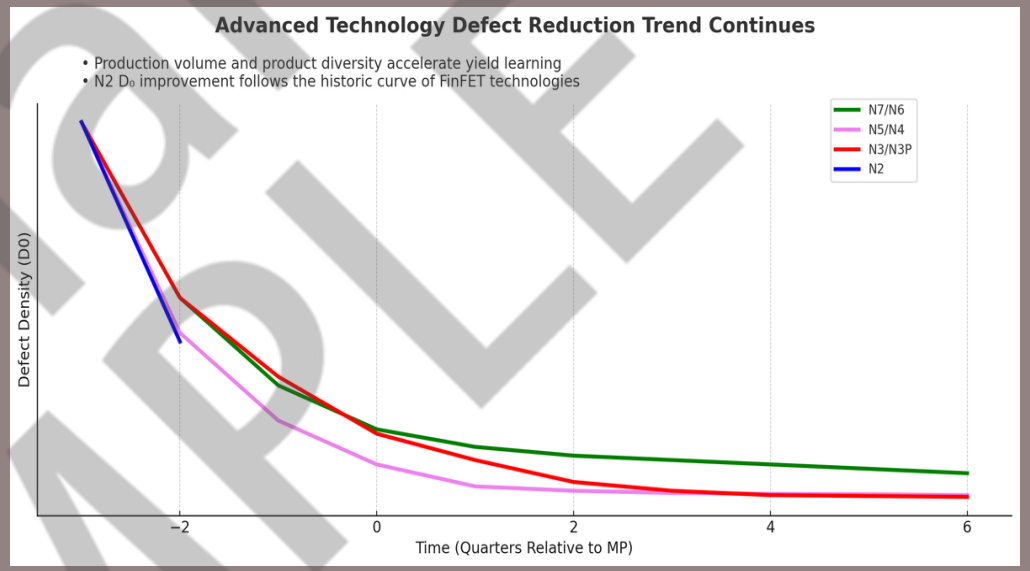
How to know the product price?
We need to know the yield
In this analyze data,we just compute Manufacturing yield
No Package yield

We need to know the D0(used Murphy's) and Wafer Price
Then we can know the Price/die and yield



Price and Yield





In those photo shows that
When the process enters mass production
We can roughly estimate D0=0.1

Estimate Price and yield we can use Level data

High Yield: D0=0.06
Middle Yield: D0=0.1
Low Yield: D0=0.15
Ultra Low Yield: D0=0.2

Table 1 – TSMC Wafer Prices by Node ($)						
	2020	2021	2022	2023	2024	2025
2nm	$0	$0	$0	$0	$0	$24,570
3nm	$0	$0	$0	$19,865	$19,150	$18,445
5nm	$13,495	$14,105	$14,105	$13,400	$12,730	$12,095
7nm	$10,720	$10,775	$10,775	$10,235	$9,725	$9,240
Source: The Information Network (www.theinformationnet.com)						

Image credit: The Information Network via SeekingAlpha

N7 Price in 2024/2025 was nearly 18000$/Wafer

Each A19 Pro Price
25.93$ to 36.97$

A19Pro in 3 Price of 4 Yield

Price	High yield	Middle yield	Low yield	Ultra low yield
16000$	25.93	26.936	28.22	29.58
18000$	29.17	30.30	31.75	33.27
20000$	32.41	33.67	35.27	36.97

Yield data

Yield	High yield	Middle yield	Low yield	Ultra low yield
A19pro	94.39%	90.856%	86.65%	82.67%

Good Die per Wafer data

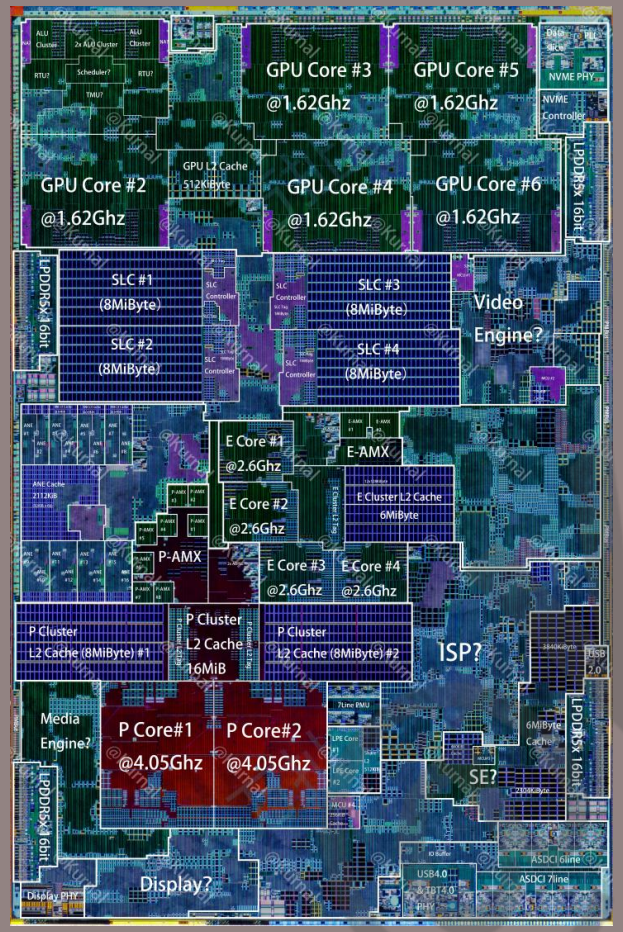
GDPW	High yield	Middle yield	Low yield	Ultra low yield
A19Pro	617	594	567	541

High Yield: D0=0.06
Middle Yield: D0=0.1
Low Yield: D0=0.15
Ultra Low Yield: D0=0.2

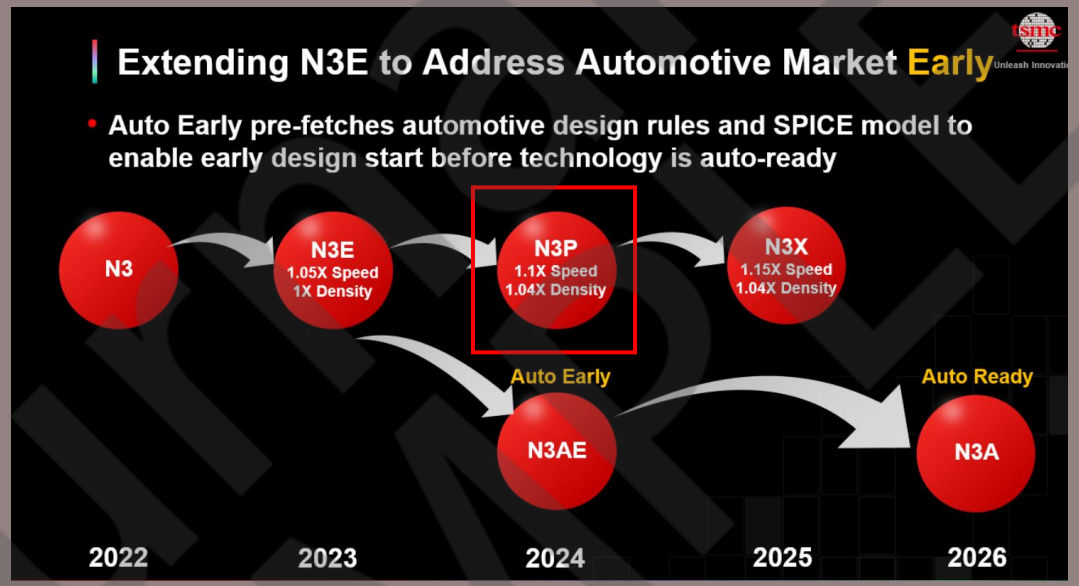
Transister number

Apple A19 Pro

Transister number



Die Shot

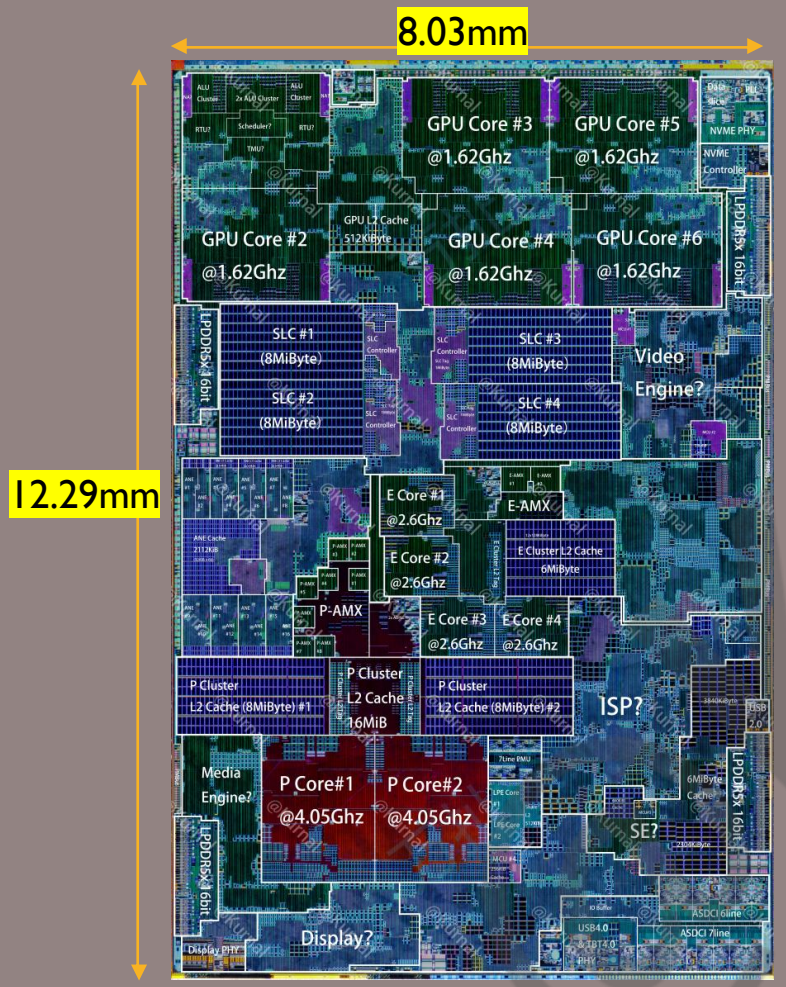


Chip Technology: TSMC N3P (3nm 3rd)

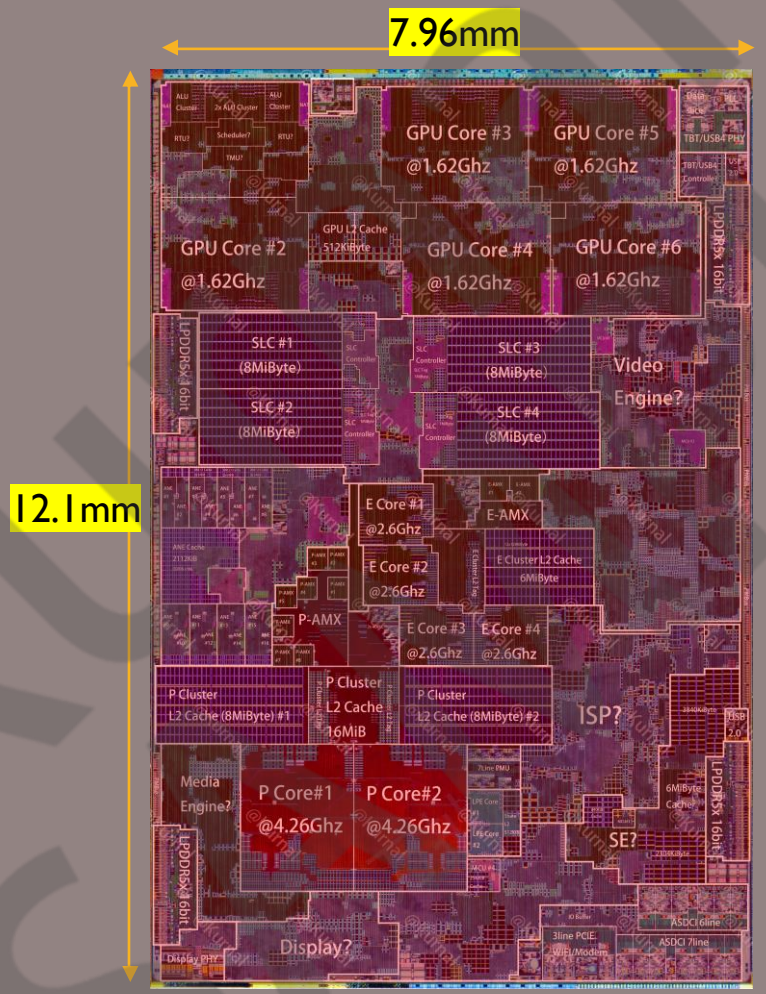
Transister Number: non-data

N3 FINFLEX™

Transister number



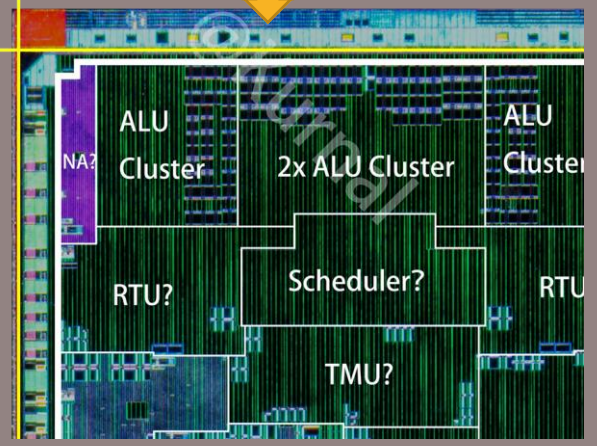
Die Shot



Chip size: 98.69mm2

Chip size in used: 96.316mm2

Score groove



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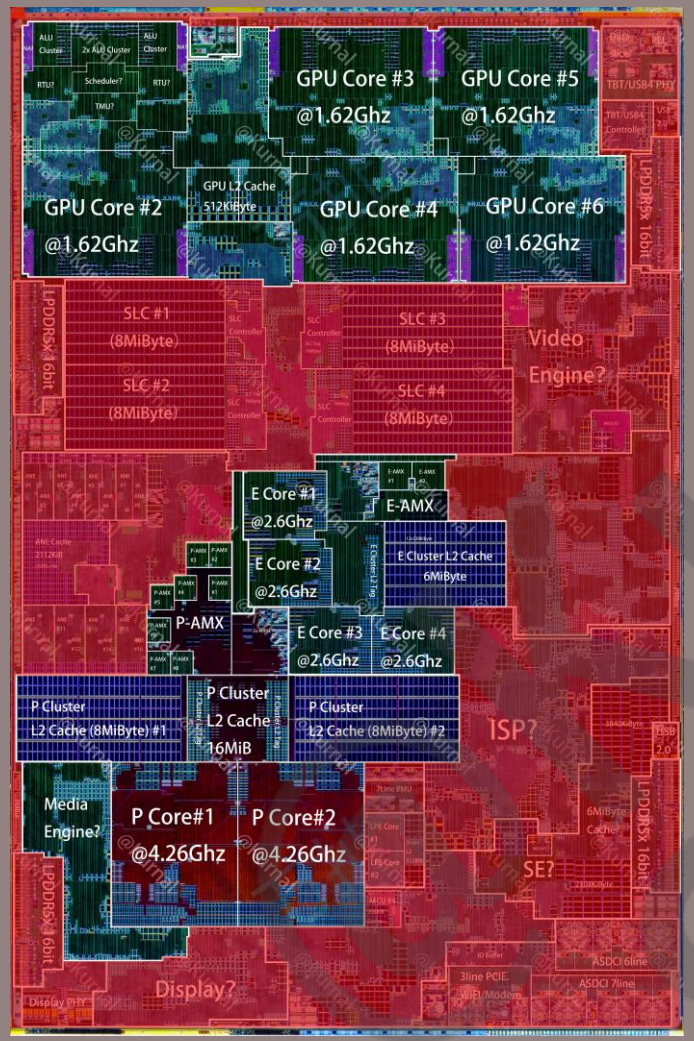
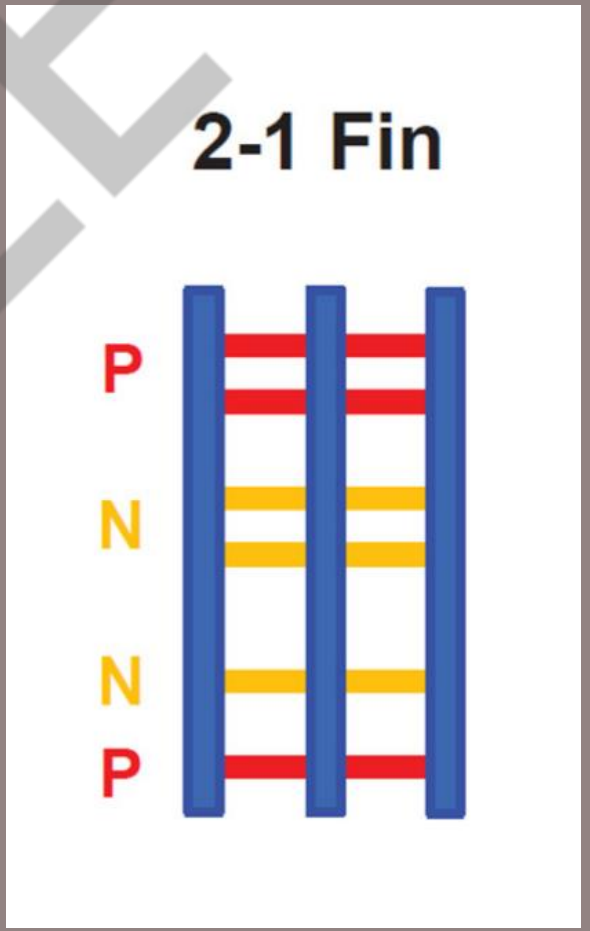


Used UHD lib

Cell H	143nm
Gate Pitch	48nm
Logic Density:	214.7Mtr/mm2
Area:	49.761mm2
Tr number:	10683.69Mtr



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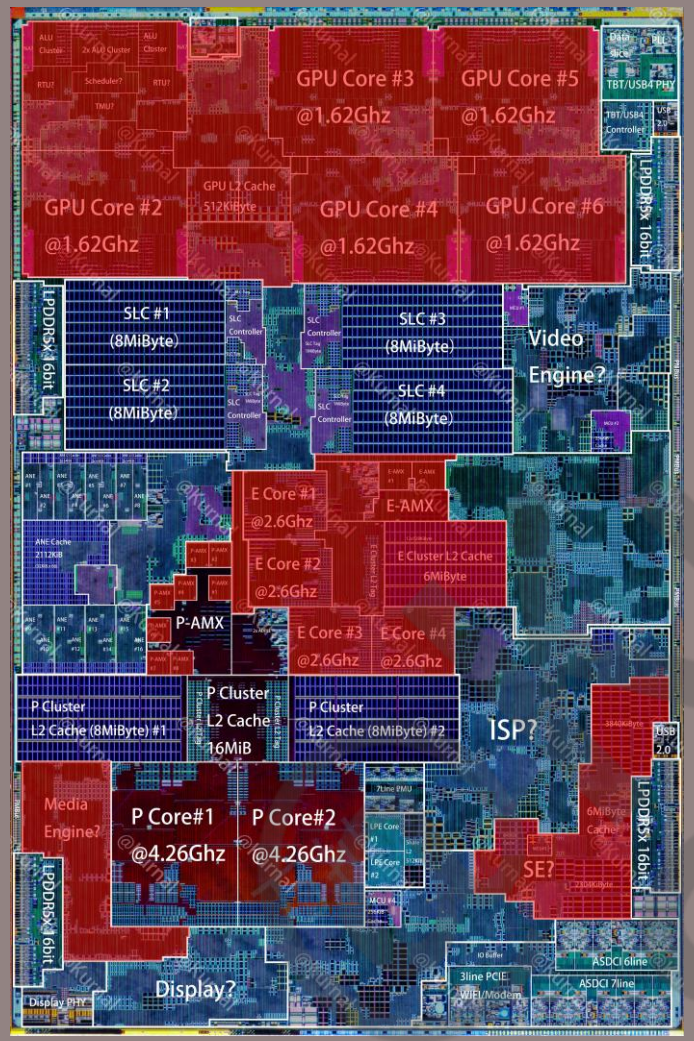
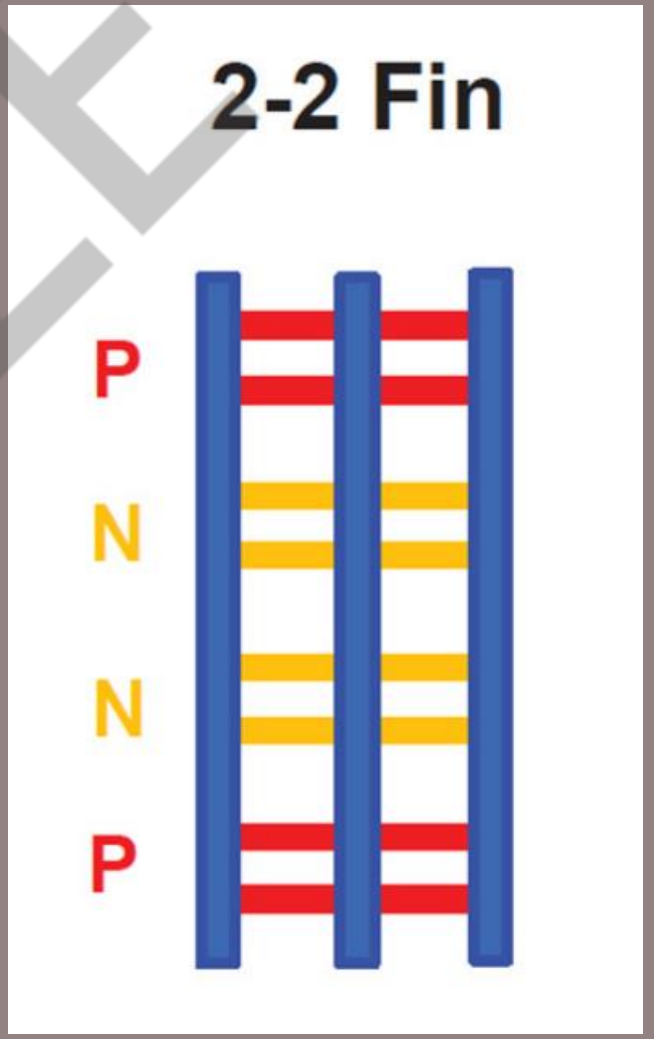
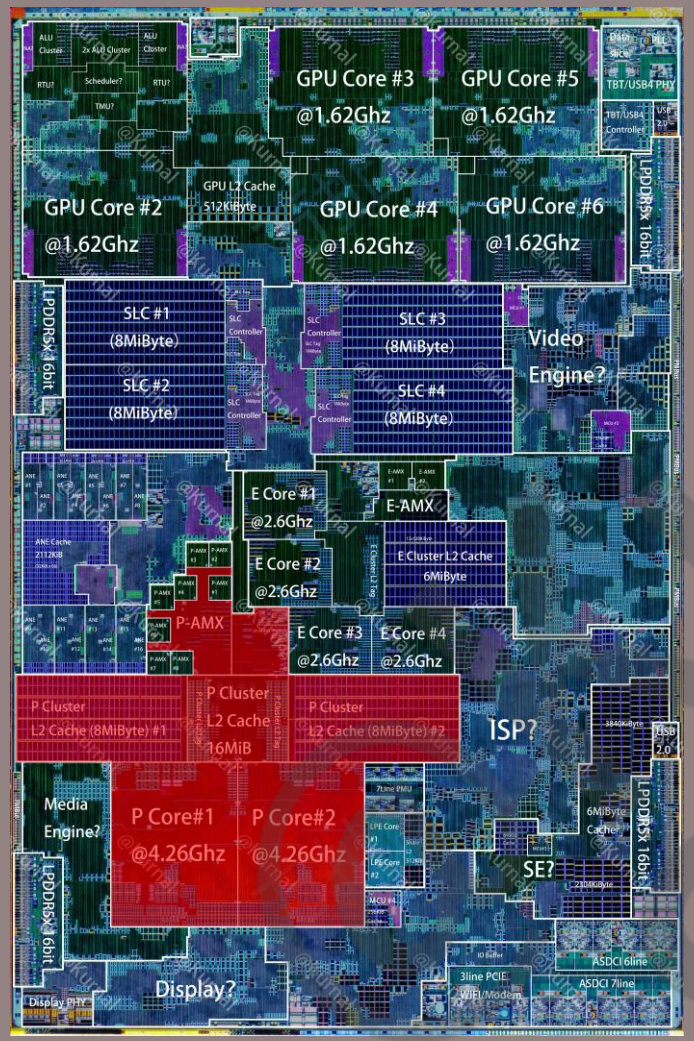


Used HD lib

Cell H	169nm
Gate Pitch	48nm
Logic Density:	181.67Mtr/mm2
Area:	33.846mm2
Tr number:	6148.8Mtr

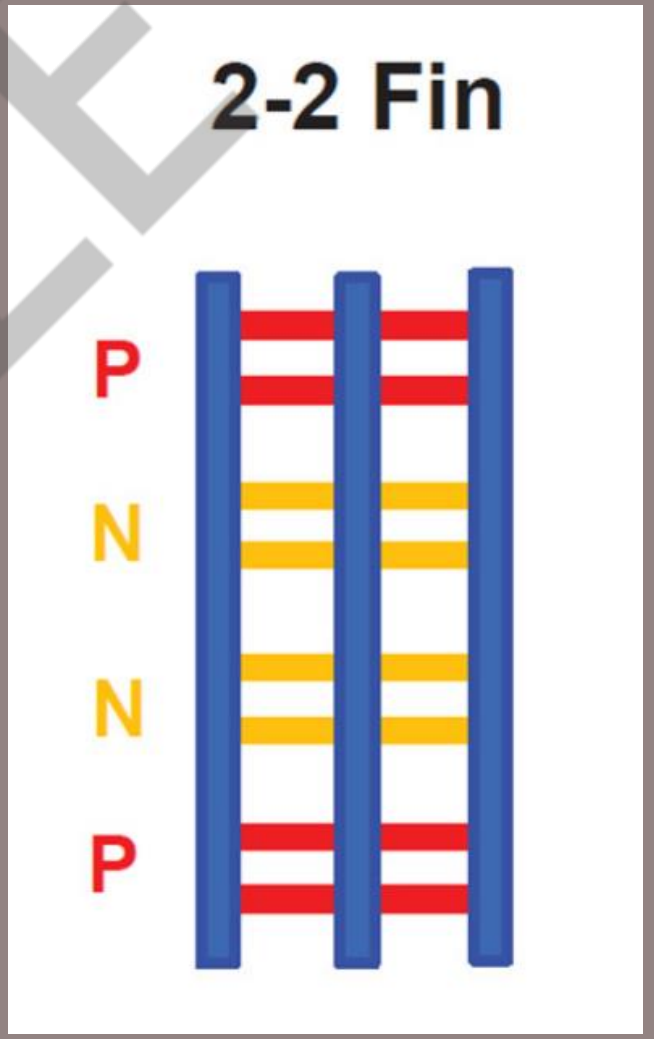


Transister number



Used HP lib

Cell H	169nm
Gate Pitch	54nm
Logic Density:	161.48Mtr/mm2
Area:	12.709mm2
Tr number:	2052.25Mtr



Transister number

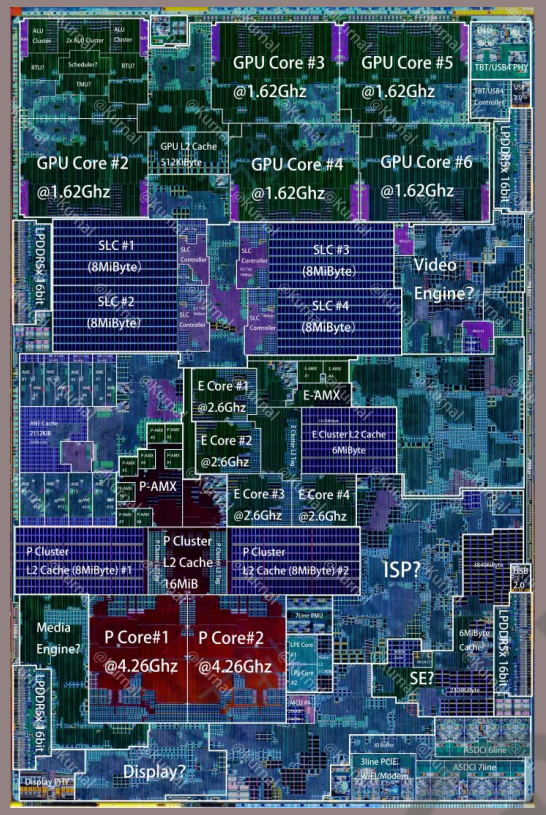
Used UHD lib		Used HD lib		Used HP lib	
Cell H	143nm	Cell H	169nm	Cell H	169nm
Gate Pitch	48nm	Gate Pitch	48nm	Gate Pitch	54nm
Logic Density:	214.7Mtr/mm2	Logic Density:	181.67Mtr/mm2	Logic Density:	161.48Mtr/mm2
Area:	49.761mm2	Area:	33.846mm2	Area:	12.709mm2
Tr number:	10683.69Mtr	Tr number:	6148.8Mtr	Tr number:	2052.25Mtr

A19Pro Transisters number=18,884.74Millions=18.88Billions

On chip analyze-CPU

Apple A19 Pro

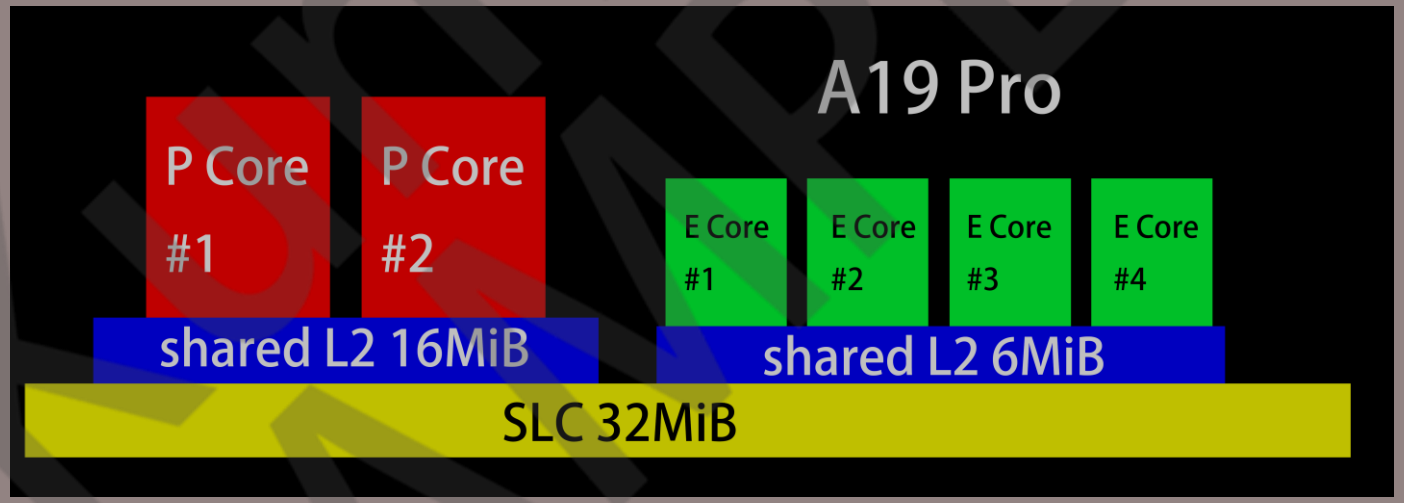
On chip analyze-CPU



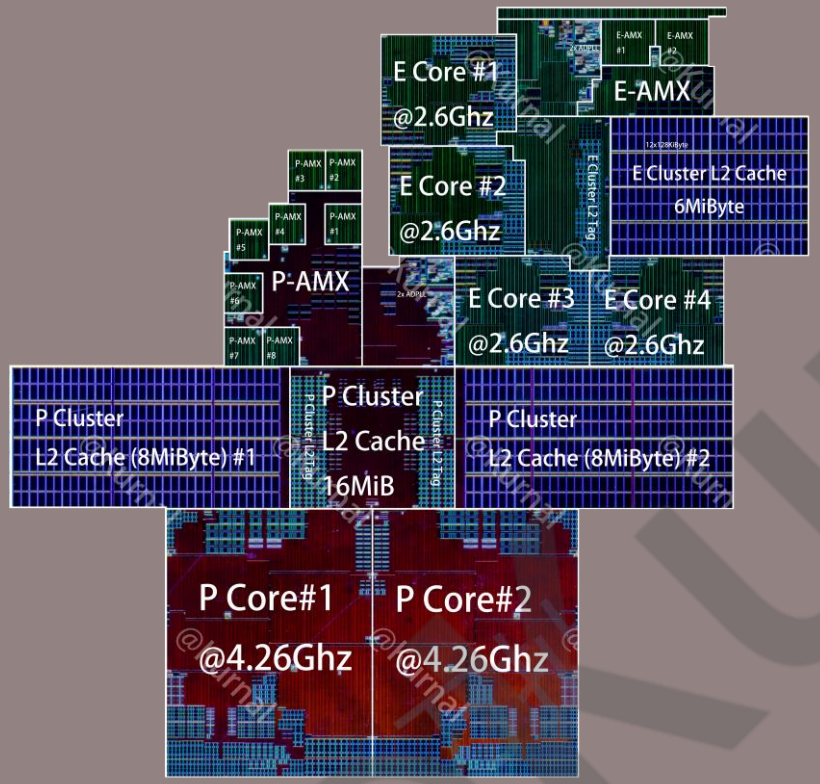
2x P Core @4.26Ghz Shared L2 16MiB

4x E Core @2.6Ghz Shared L2 6MiB

SLC 32MiB



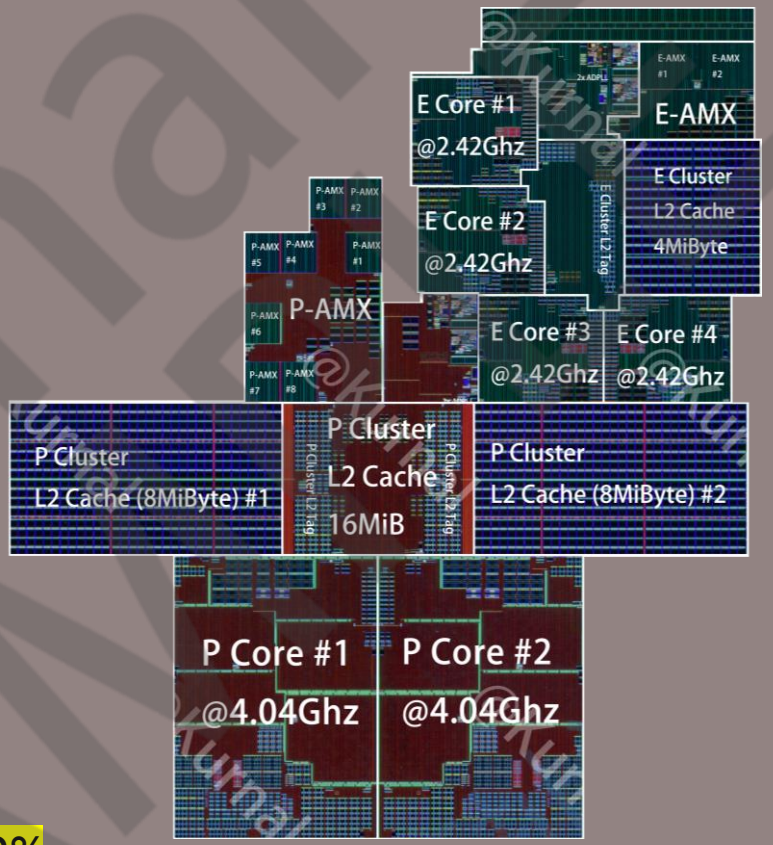
On chip analyze-CPU-Cluster



A19Pro CPU-all Cluster

Small than 4.62%

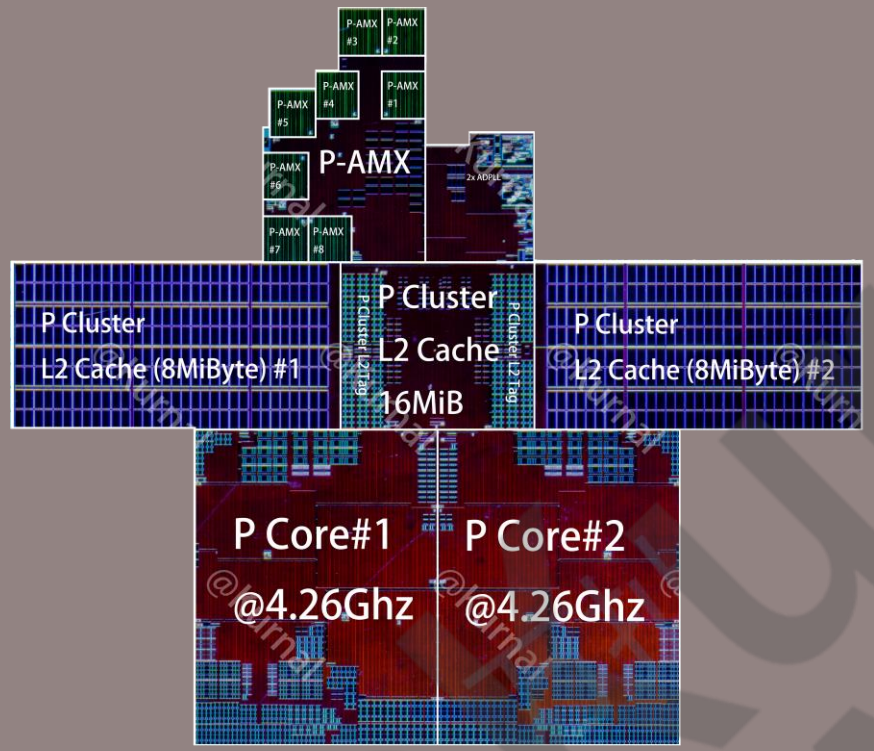
CPU Cluster size: 19.923mm2



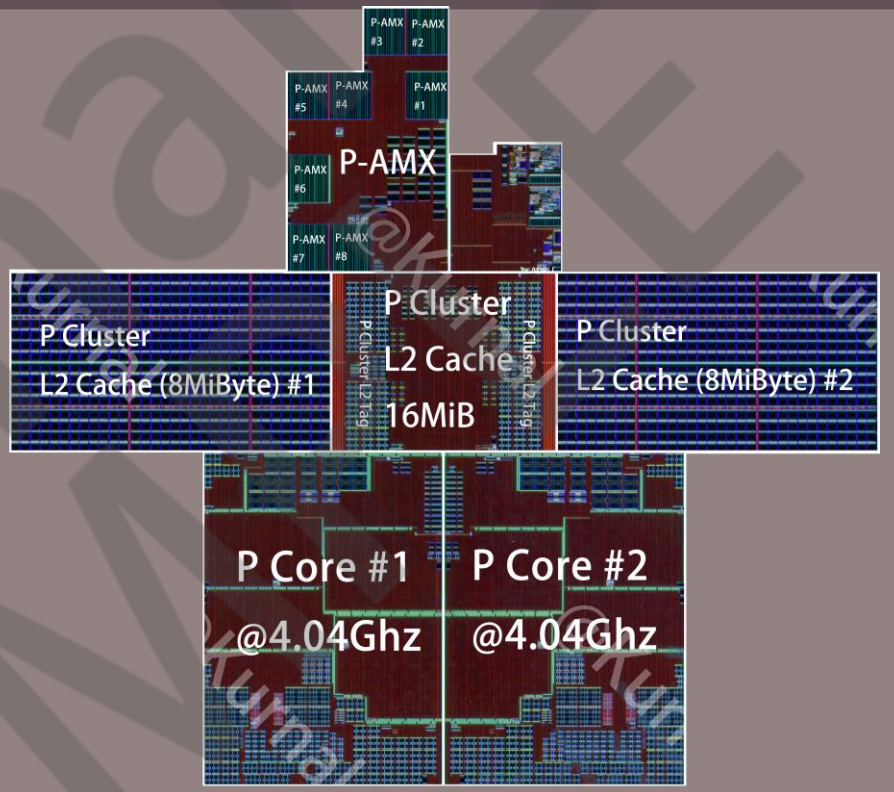
A18Pro CPU-all Cluster

CPU Cluster size: 20.889mm2

On chip analyze-CPU-PCluster



A19Pro CPU-P Cluster



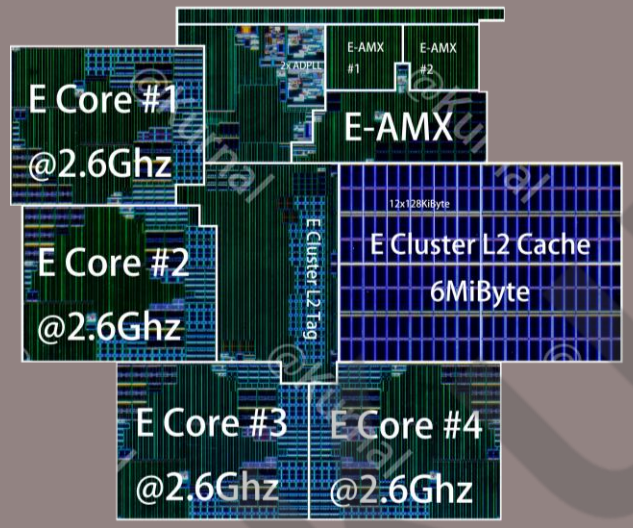
A18Pro CPU-P Cluster

Small than 6.76%

CPU Cluster size: 13.349mm2

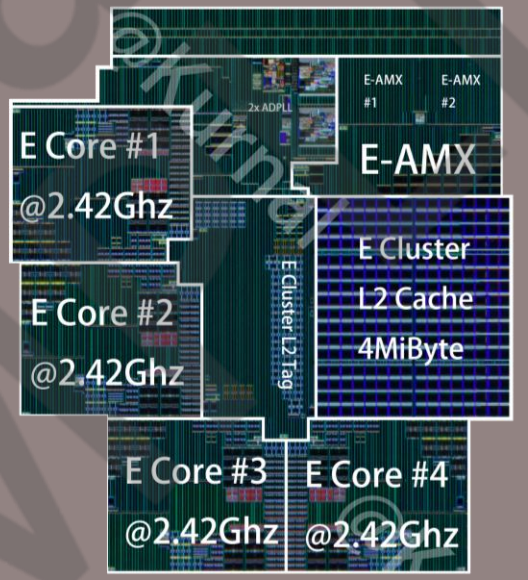
CPU Cluster size: 14.317mm2

On chip analyze-CPU-ECluster



A19Pro CPU-E Cluster

CPU Cluster size: 6.574mm2



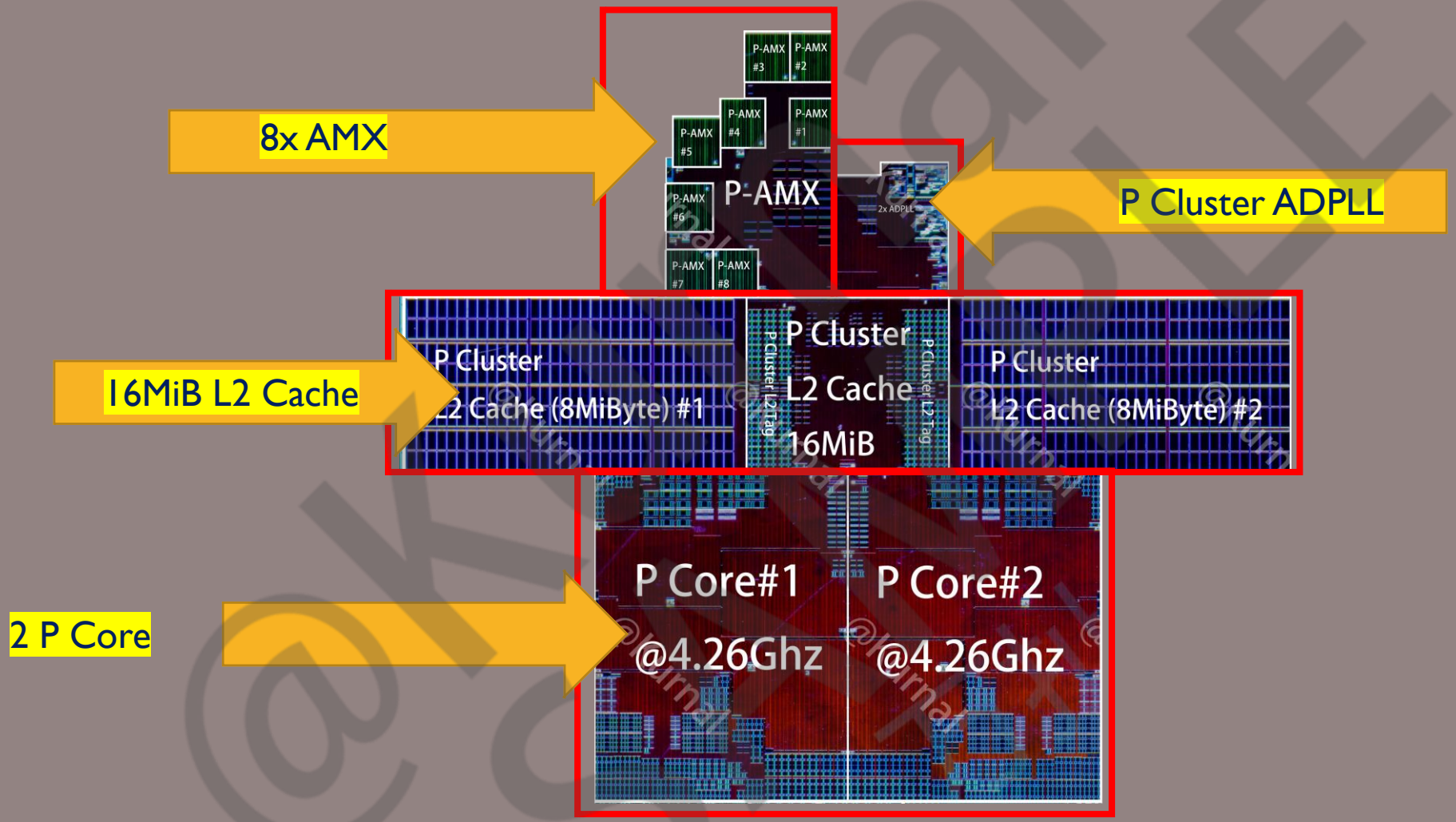
A18Pro CPU-E Cluster

CPU Cluster size: 6.572mm2

On chip analyze-CPU

P Cluster

On chip analyze-CPU-P cluster



On chip analyze-CPU-P Core

New P Core
@4.26Ghz

Higher than 5%

A18Pro P Core
@4.04Ghz

P Core @A19pro

P Core @A18pro

Compared to the A18 Pro
the A19 Pro's Performance Core (P-Core)
has increased by over 5% (to 4.26GHz)

while the core size
has shrunk by approximately 2.27%.

Smaller than 2.27%

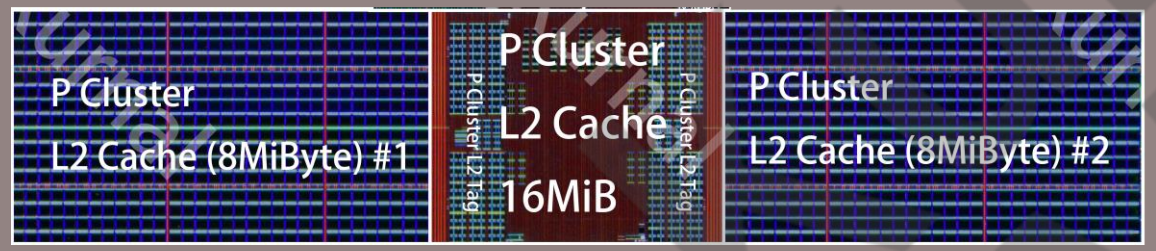
Core size:3.259mm2

Core size:3.335mm2

P-L2 Cache @A19pro

A19Pro P L2 16MiB
5.487mm2

Smaller 9.6%

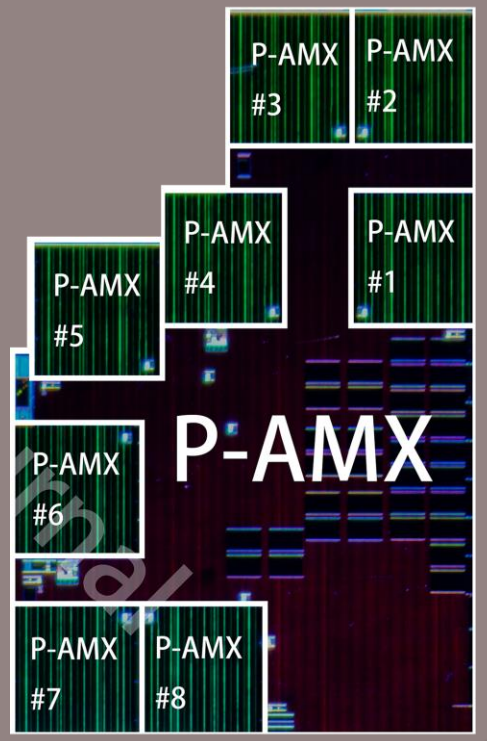


P-L2 Cache @A18pro

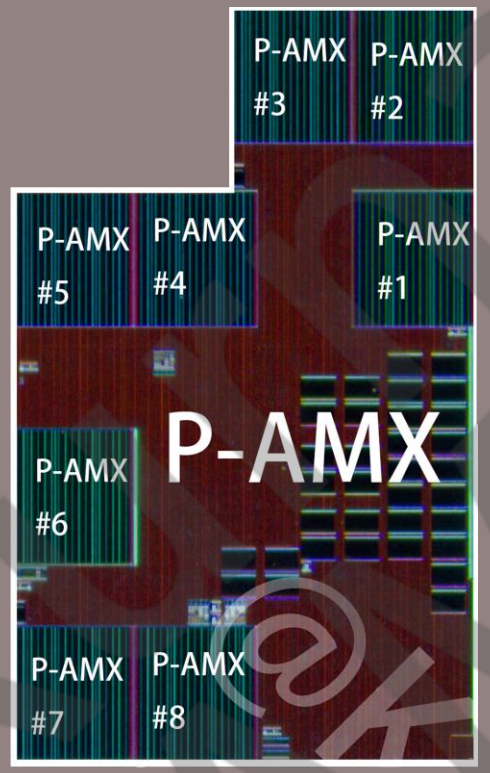
A18Pro P L2 16MiB
6.07mm2

While maintaining the 16MiB capacity,
the A19 Pro's L2 cache area is roughly 9.6% smaller than the A18 Pro's,
showcasing the benefits of physical scaling from advanced process nodes.

On chip analyze-CPU-P AMX



P-AMX @A19pro



P-AMX @A18pro

Similar layout to A18 Pro (Likely same IP)

The P-Core AMX unit in the A19 Pro shows a very similar layout to the A18 Pro, suggesting they share the same IP design.

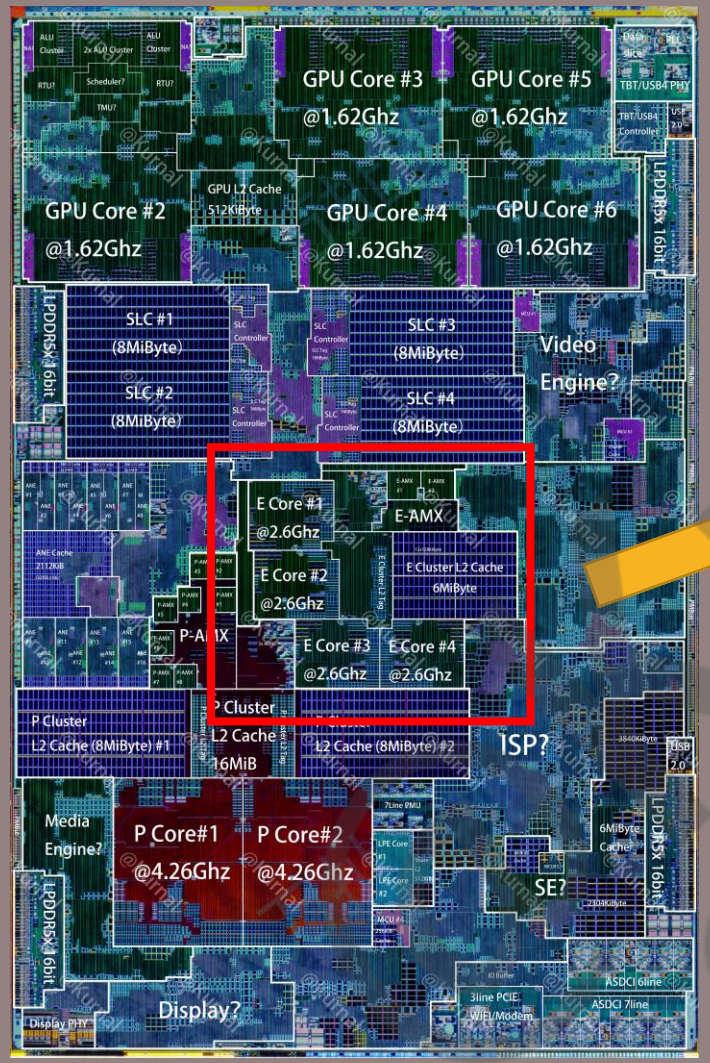
P-AMX @A19pro

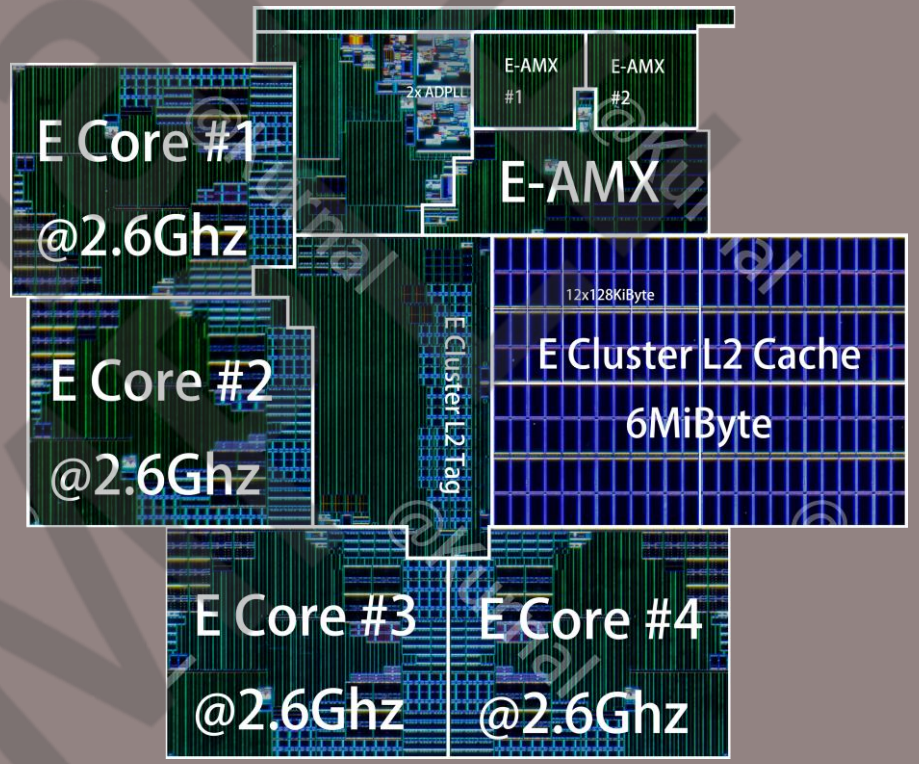
P-AMX size: 0.08mm2

On chip analyze-CPU

E Cluster

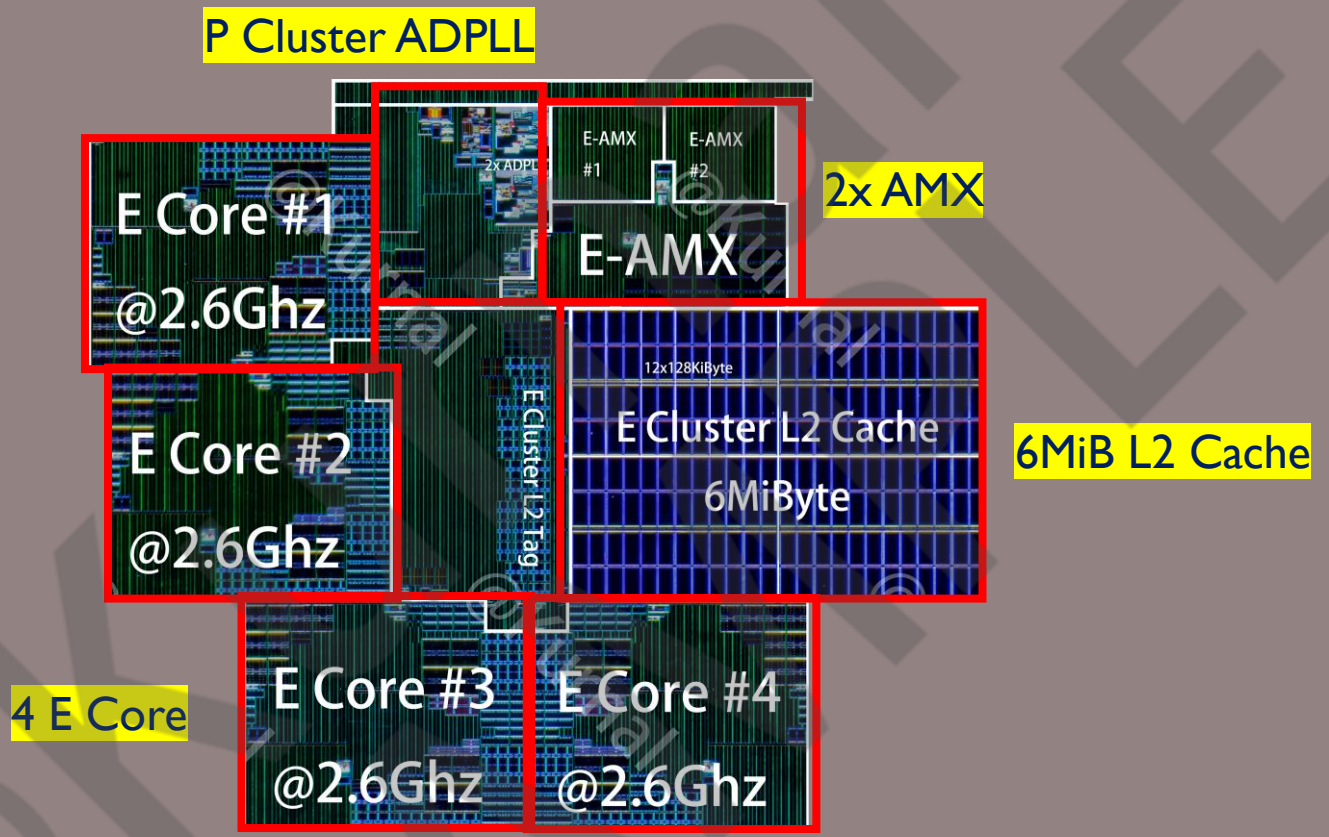
On chip analyze-CPU-E





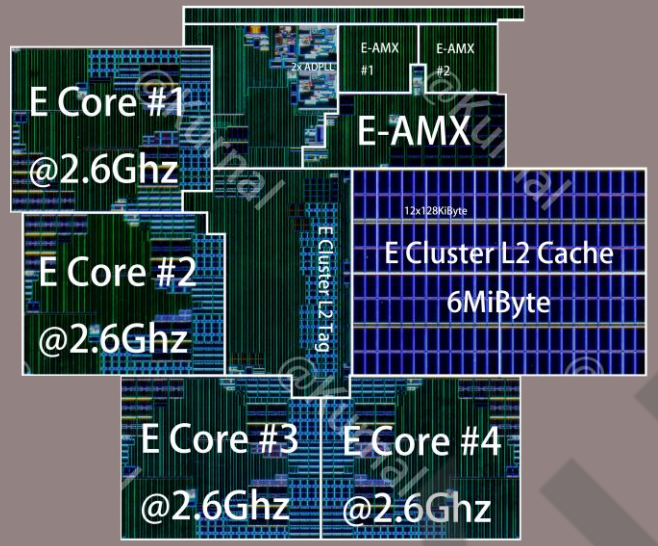
A19Pro CPU-E Cluster

CPU Cluster size: 6.574mm2



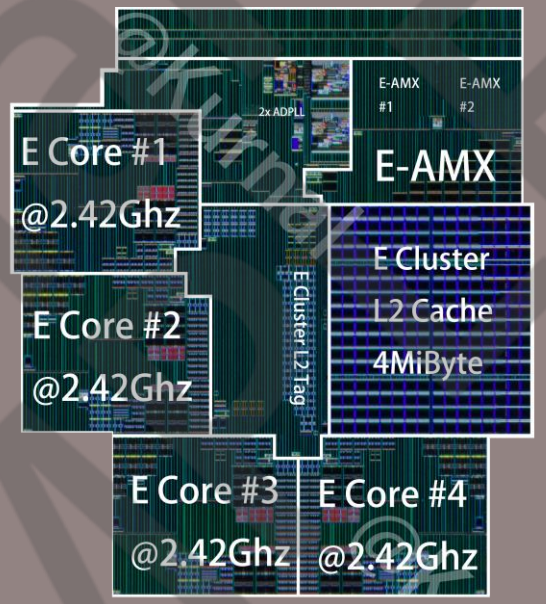
A19Pro CPU-E Cluster

On chip analyze-CPU-E



E Core @A19pro

E-Cluster Area: 6.574mm²



E Core @A18pro

E-Cluster Area: 6.572mm²

Design: Global 2-2 HD Library

Comparison: Nearly unchanged vs previous generation

On chip analyze-CPU-E

E Core @A19pro

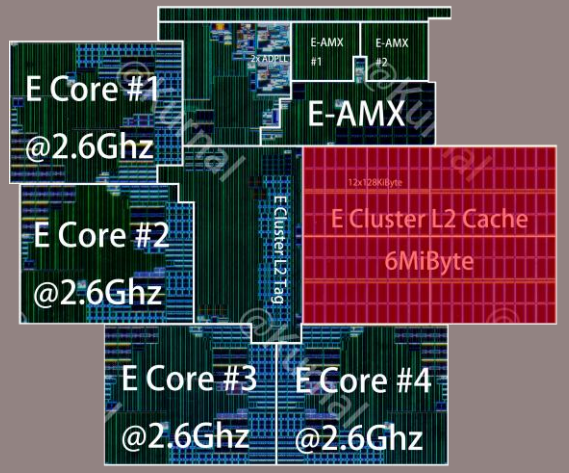
Core Area: 0.786mm² (+8.8%)

E Core @A18pro

Core Area: 0.722mm²

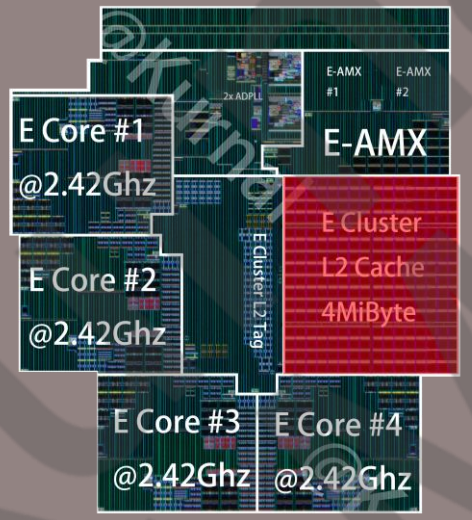
A19 Pro's E-Core single-core area is 0.786mm².
This is an 8.8% increase from the 0.722mm² of the A18 Pro.

A19Pro E Core



L2 Area: 1.489mm² (+32%)

A18Pro E Core



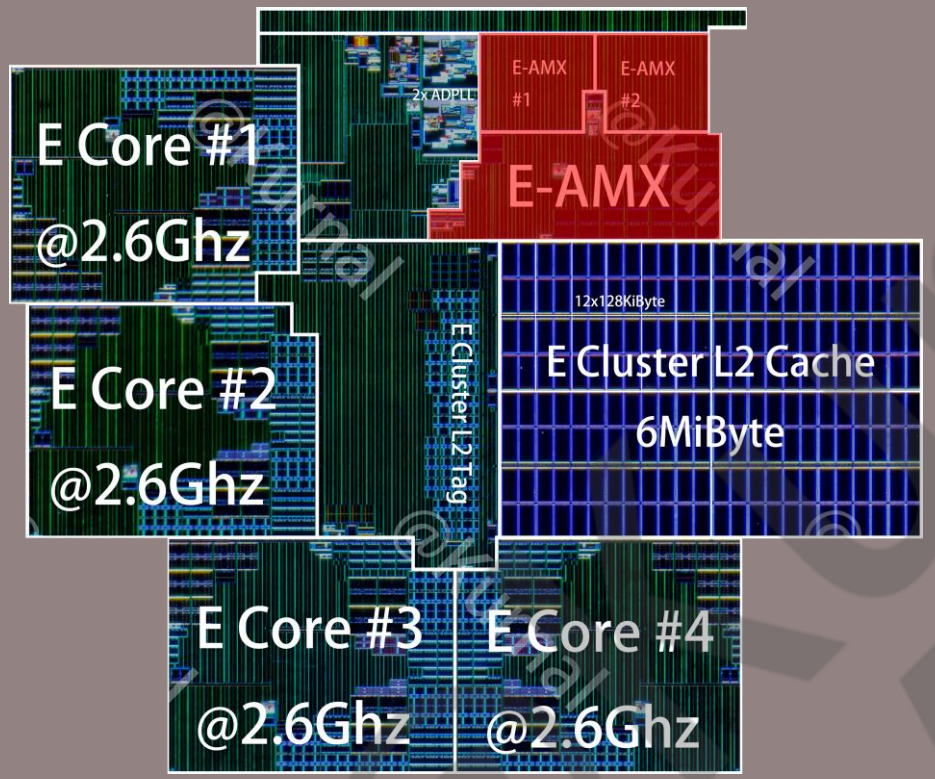
L2 Area: 1.128mm²

E-Core L2 Cache: +2MiB (1.5x)

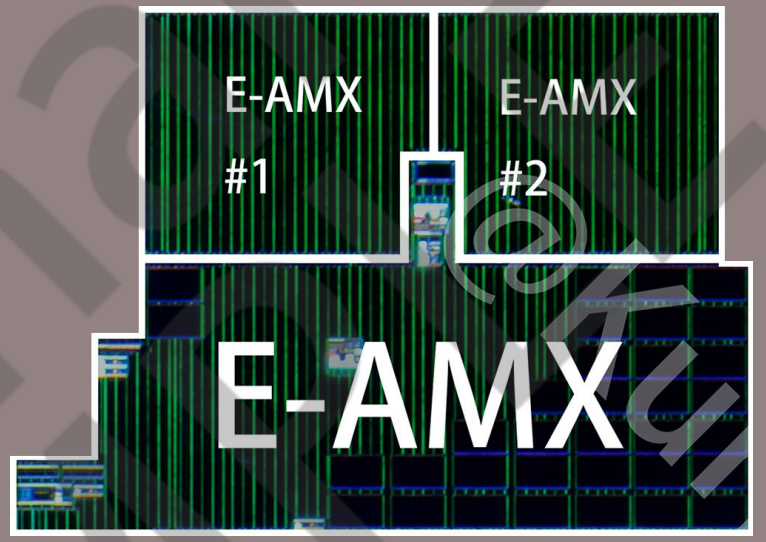
L2 Area: 1.489mm² (+32%)

A19 Pro's E-Core cluster L2 cache increased by 2MiB (1.5x).
The L2 area grew 32% to 1.489mm², an increase of 0.361mm² over the previous generation.

On chip analyze-CPU-E-AMX



E Core @A19pro

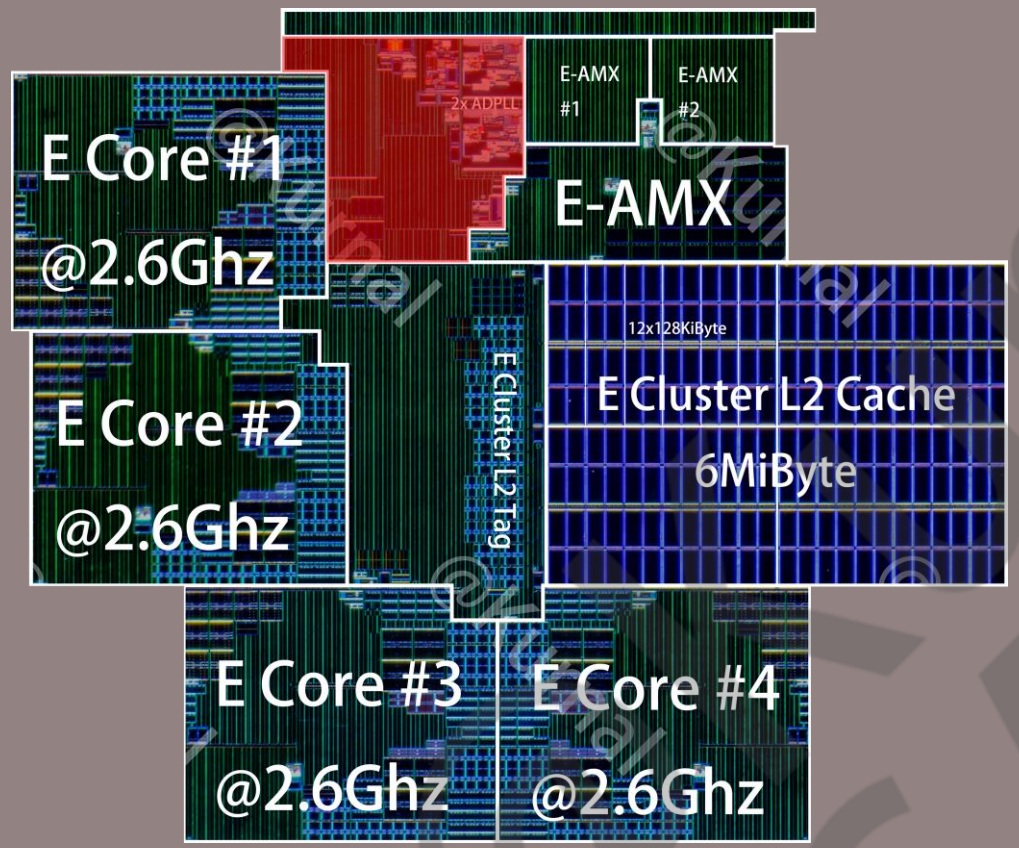


AMX size: 0.127mm2 x2

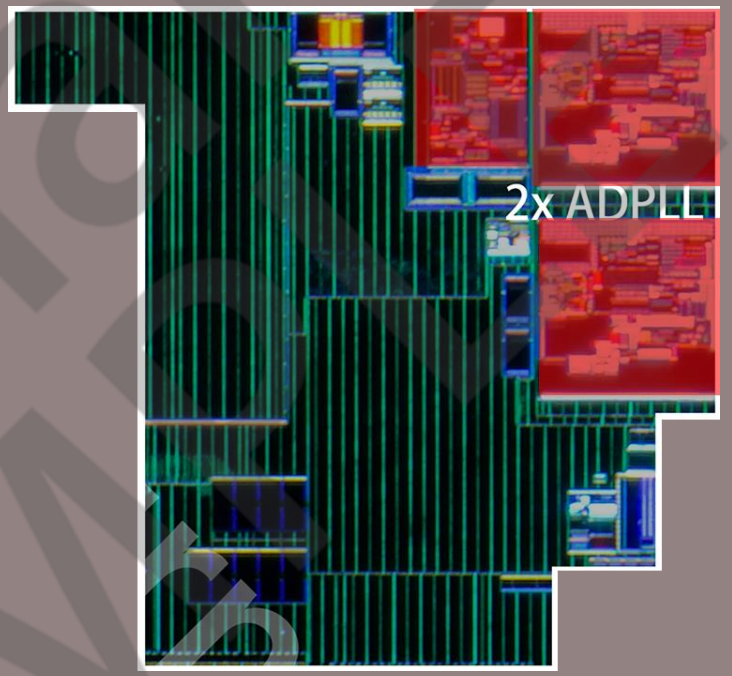
E-Cluster AMX: 2 Units (Unchanged)

Apple equipped the E-cluster with two units, consistent with the previous A18 Pro.

On chip analyze-CPU-E ADPLL



E Core @A19pro



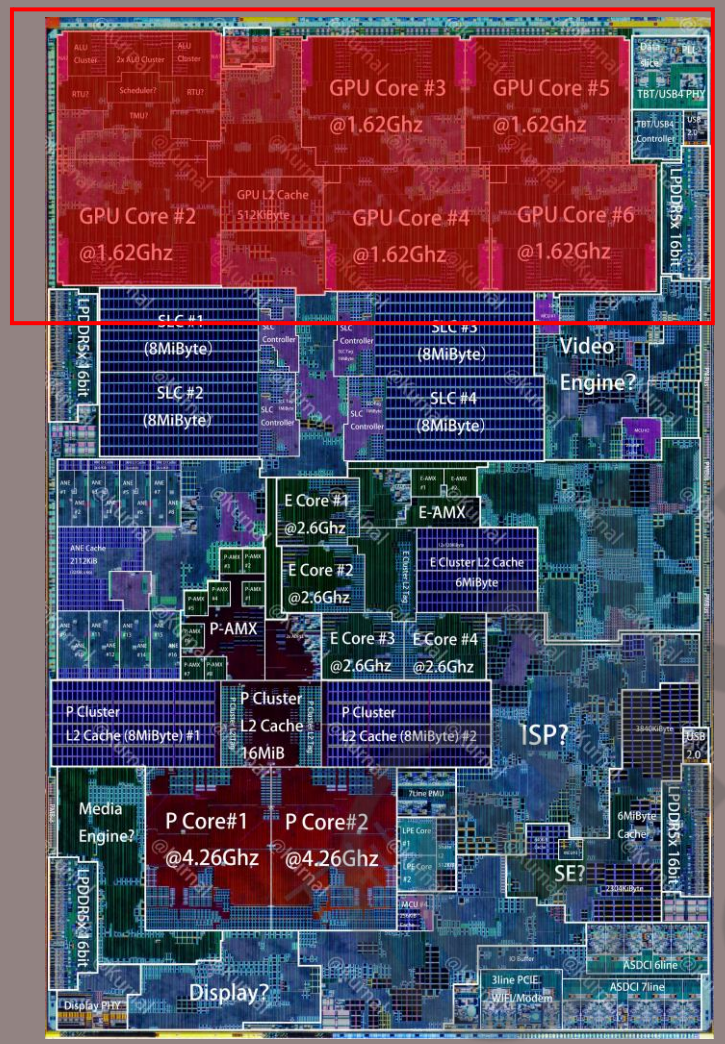
PMU Design: 2+1 (2 Main + 1 Aux/Clock)
Main PMU Size: 0.38mm² (Unchanged)

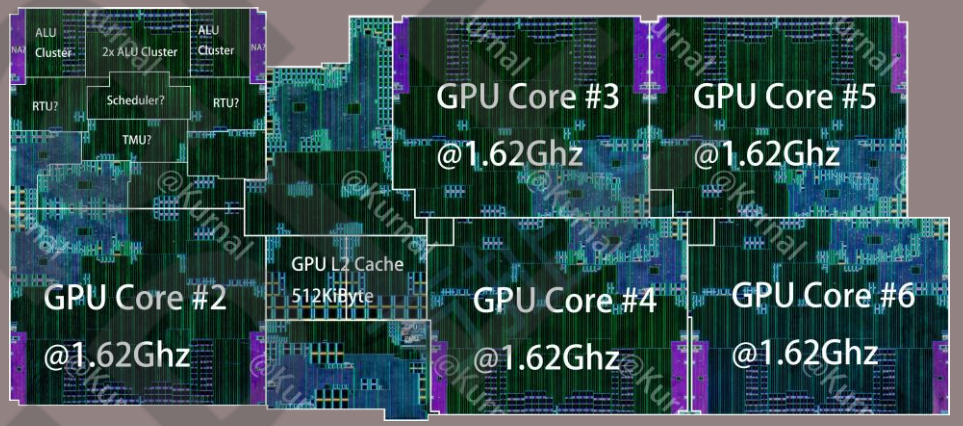
E-cluster keeps a 2+1 PMU design: 2 main units and 1 aux/clock unit.
Main unit size stays at 0.38mm².

On chip analyze-GPU

Apple A19 Pro

On chip analyze-GPU

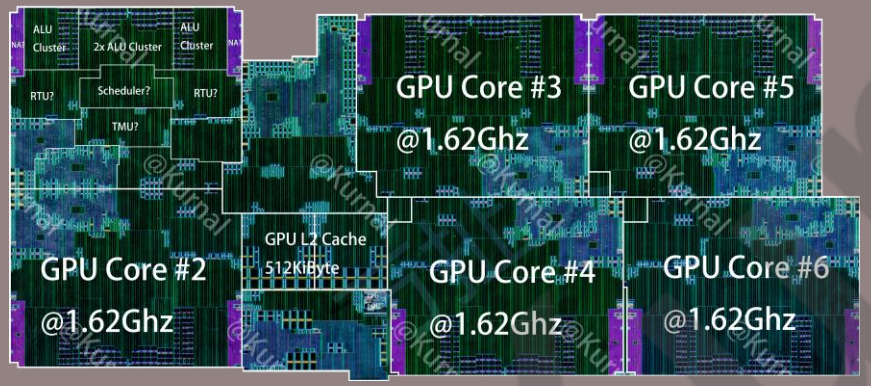




The A19 Pro continues to use the same 6-core GPU architecture as the previous generation.

A19Pro GPU

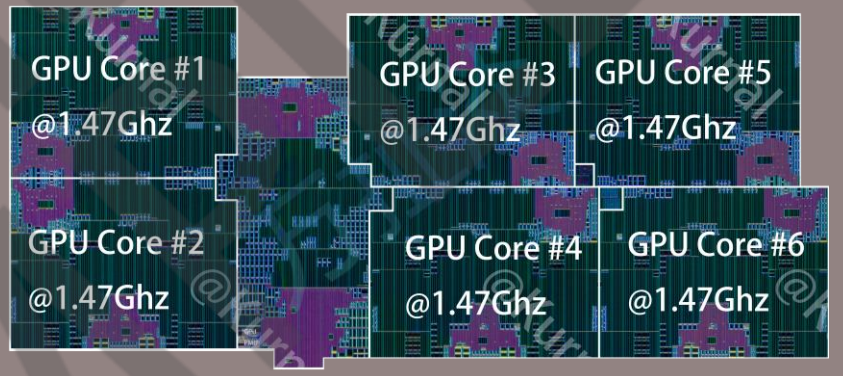
@1.62Ghz



21.215mm2

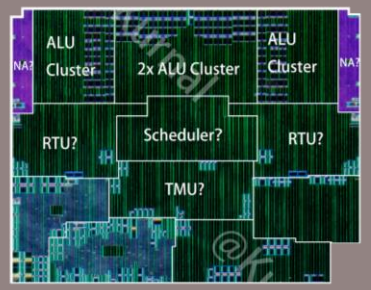
A18Pro GPU

@1.47Ghz



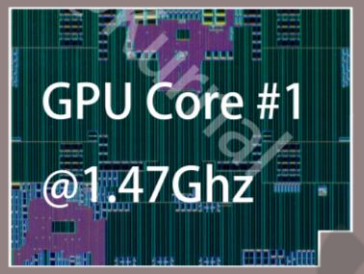
19.197mm2

The clock speed increased from 1.47GHz in the A18 Pro to 1.62GHz.
The total GPU area grew from 19.197mm² to 21.215mm².



A19Pro GPU

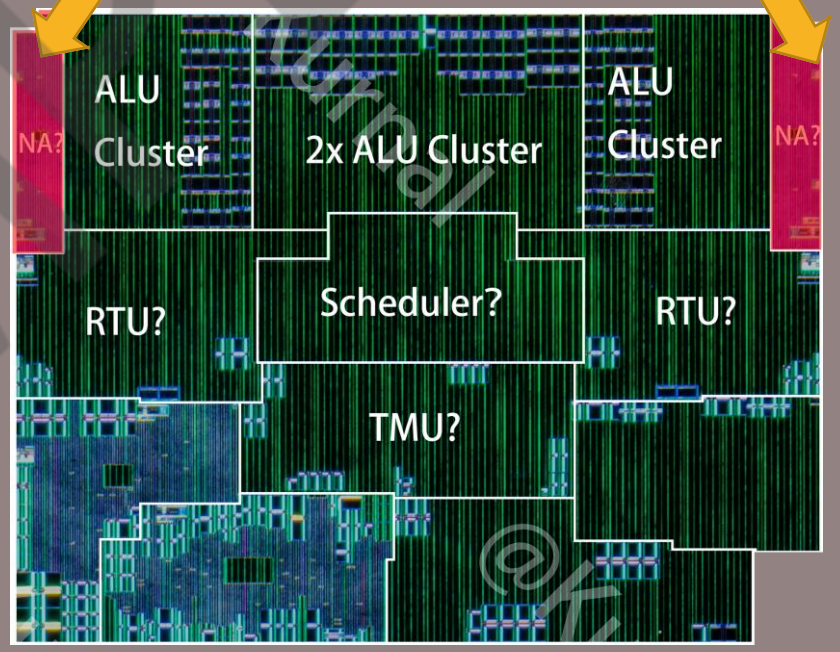
2.766mm2



A18Pro GPU

2.963mm2

Apple GPU NA
0.07mm2 x2

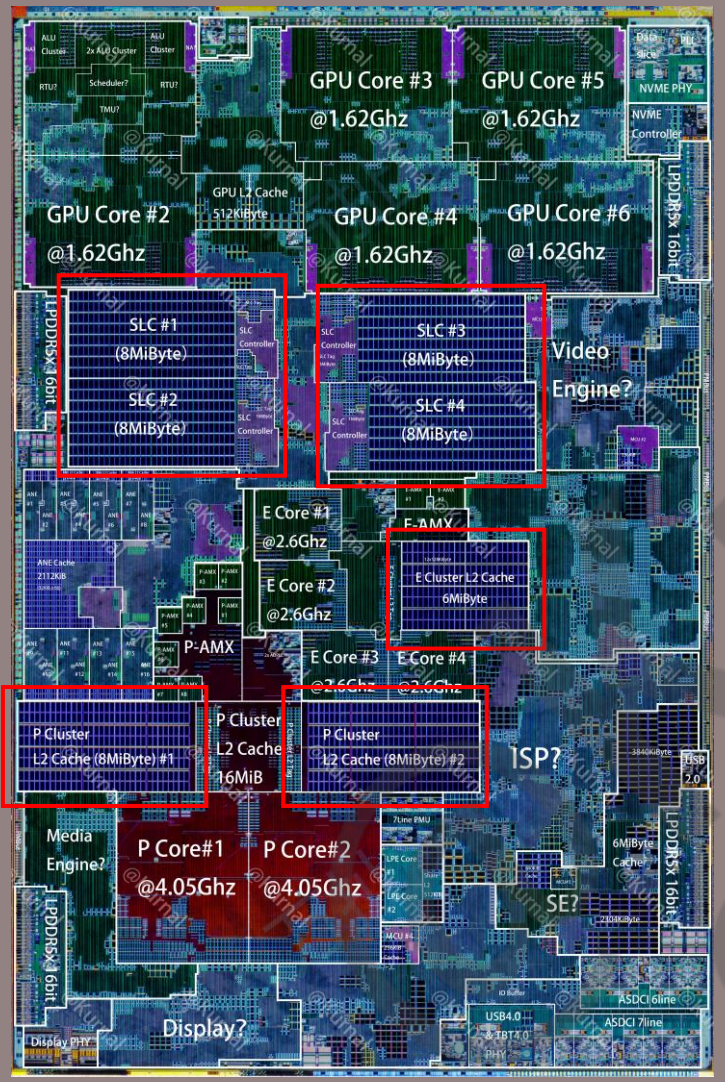


The GPU single-core area of the A19 Pro has increased significantly, growing from 2.766mm² in the A18 Pro to 2.963mm².

SRAM Density

Apple A19 Pro

SRAM Density-SRAM IP #1



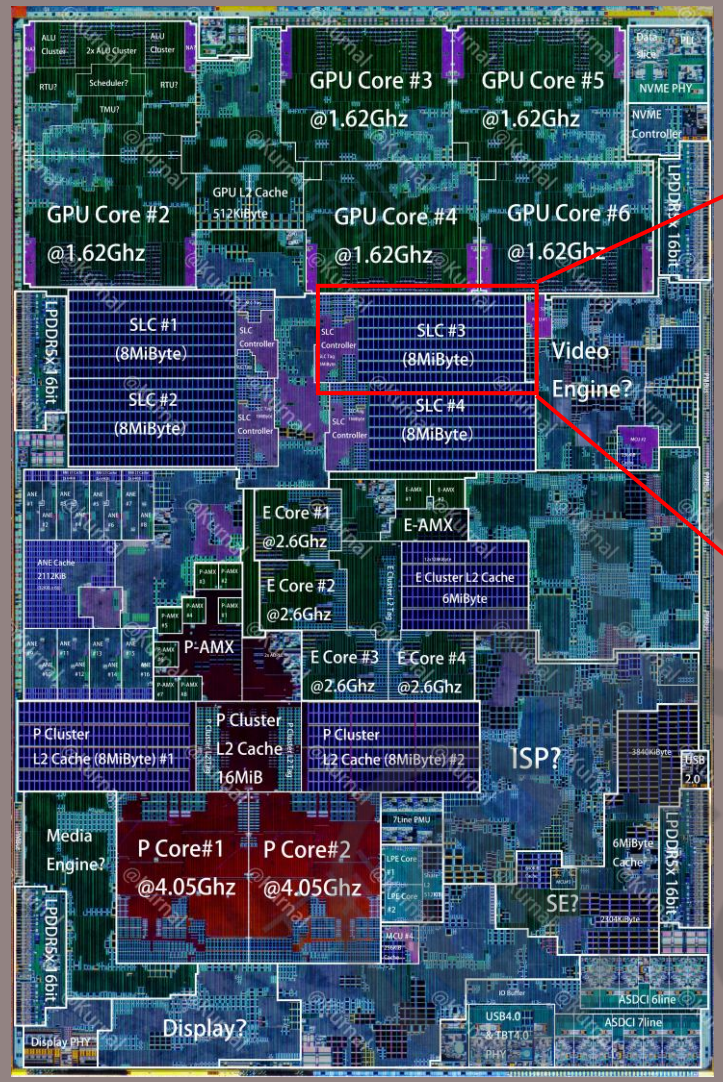
Used SRAM IP #1

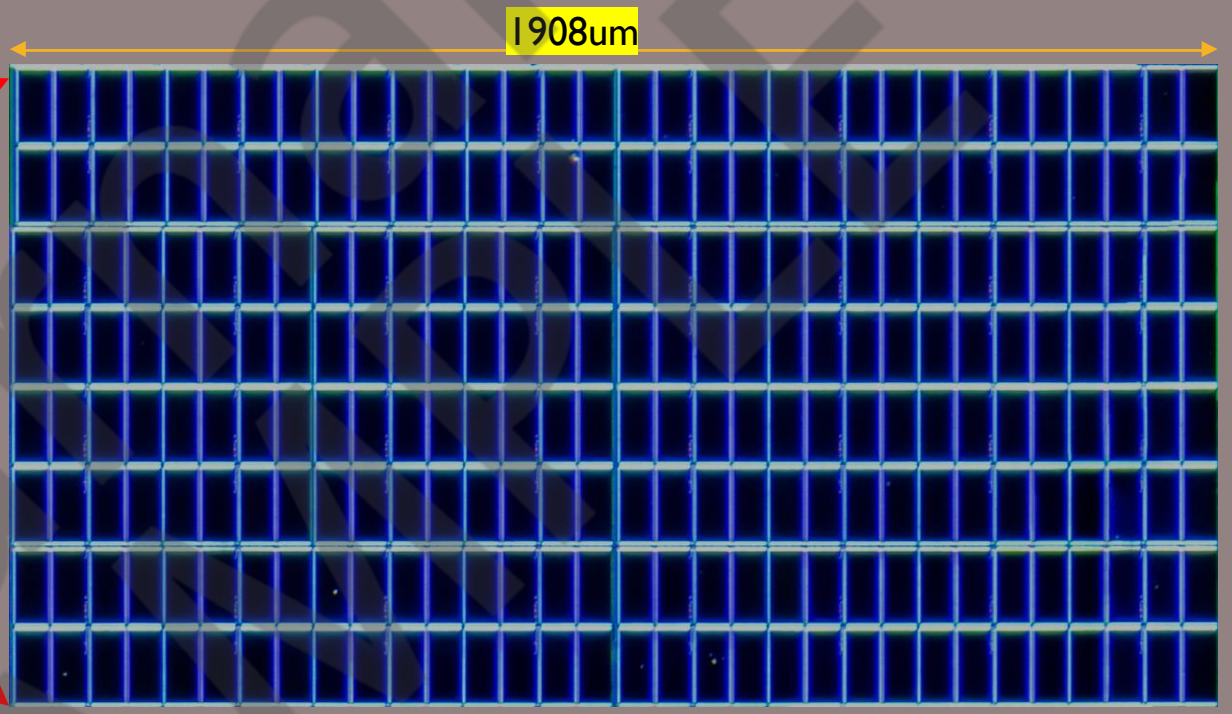
SLC: 32MiByte
P Cluster L2: 16MiByte
E Cluster L2: 6MiByte

Totally 54MiByte

SRAM IP #1

SRAM Density-SRAM IP #1

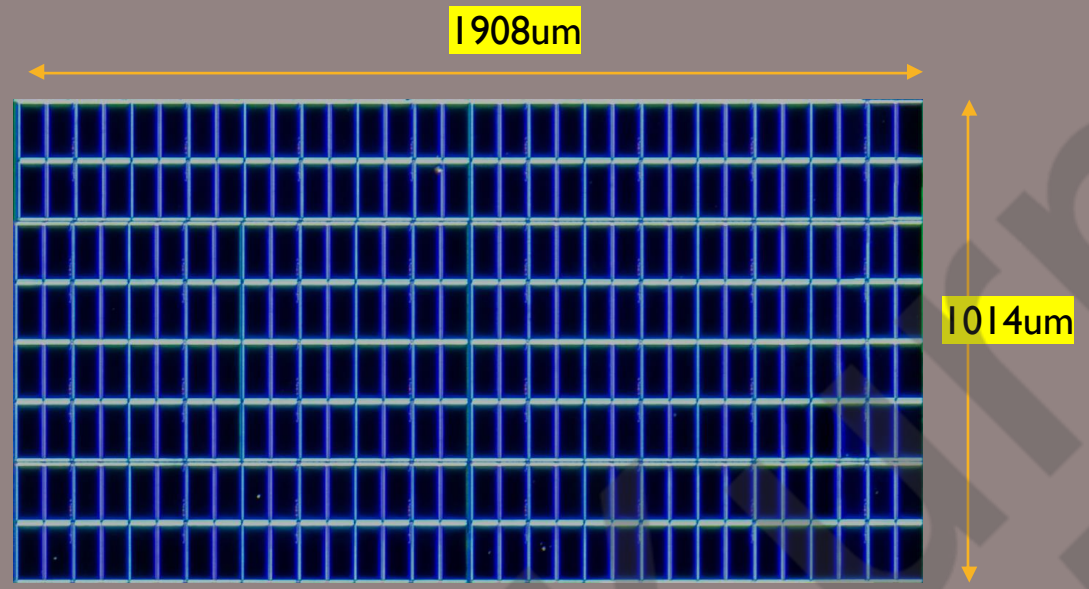




8 MiByte SRAM

SRAM Macro Density: 33.079Mbit/mm2

SRAM Density-SRAM IP #1



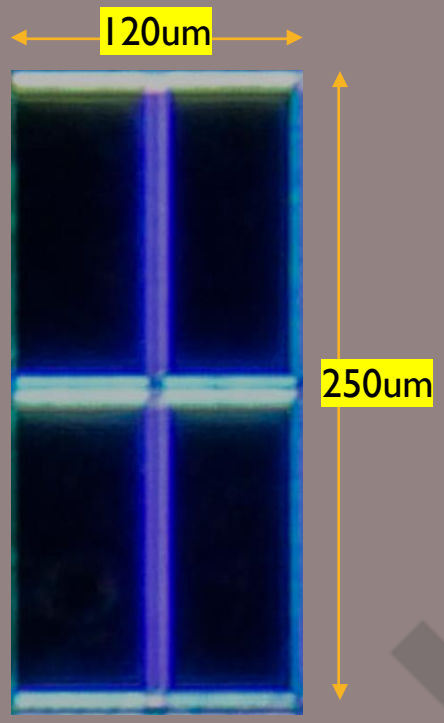
8 MiByte SRAM

SRAM Macro Density: 33.079Mbit/mm2

8 MiByte SRAM have 4 x 16=64 Block SRAM IP #1

128KiByte SRAM IP #1

SRAM Density-SRAM IP #1



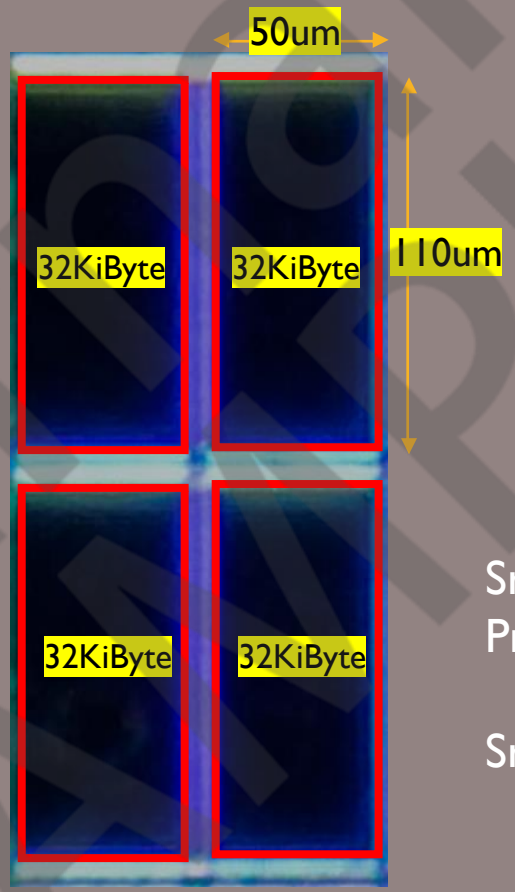
128KiByte SRAM IP #1

Size: 128KiB

0.03mm2/128KiB

4,266.66KiB/mm2

33.33Mibit/mm2

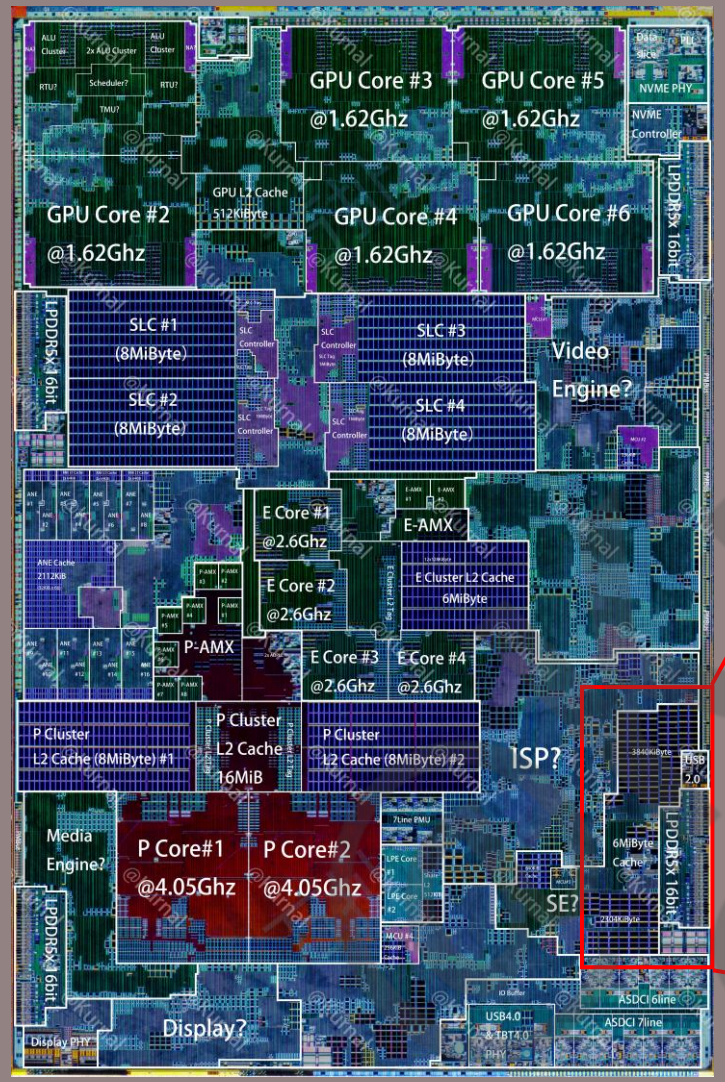


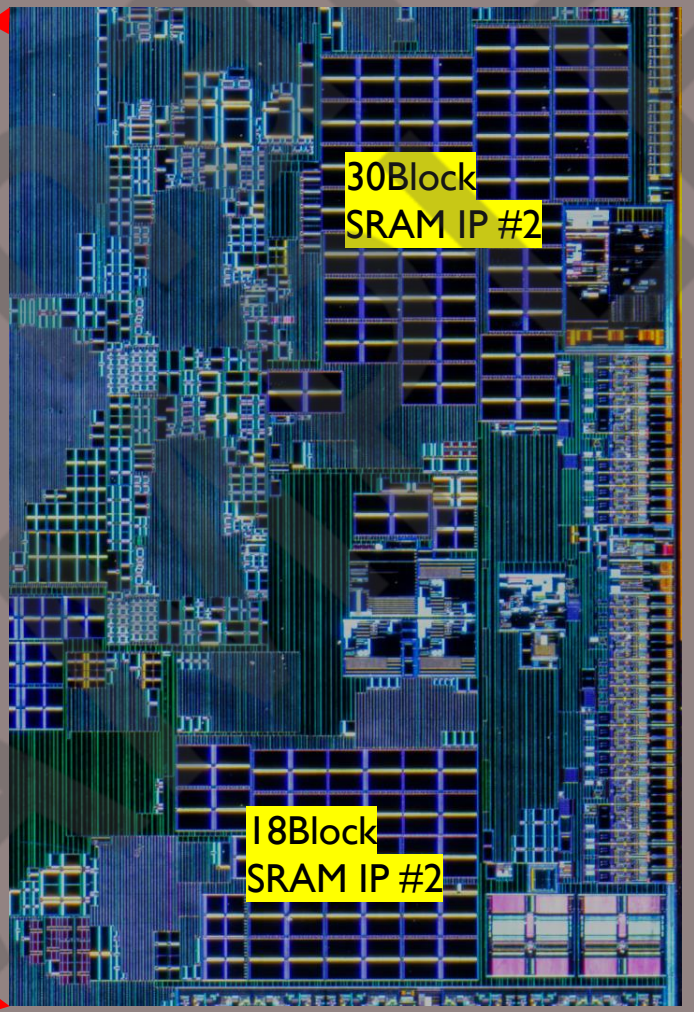
Sram bit cell by used: 22,000um2

Proportion: 73.33%

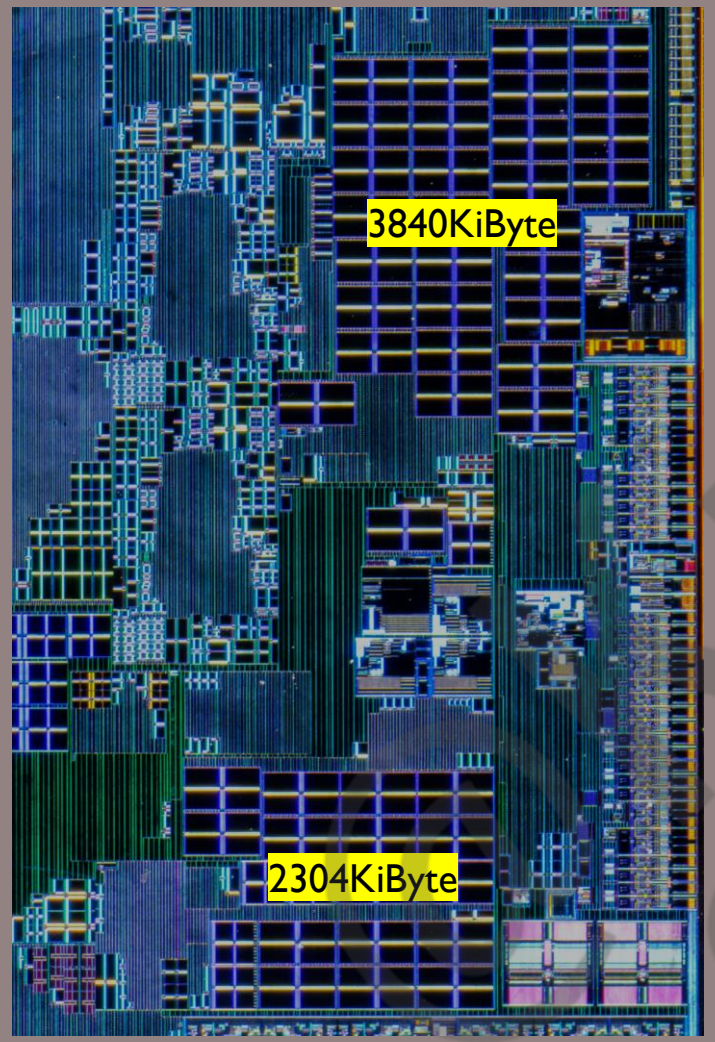
Sram Bit cell Density: 0.02098um2/bit

SRAM Density-SRAM IP #2



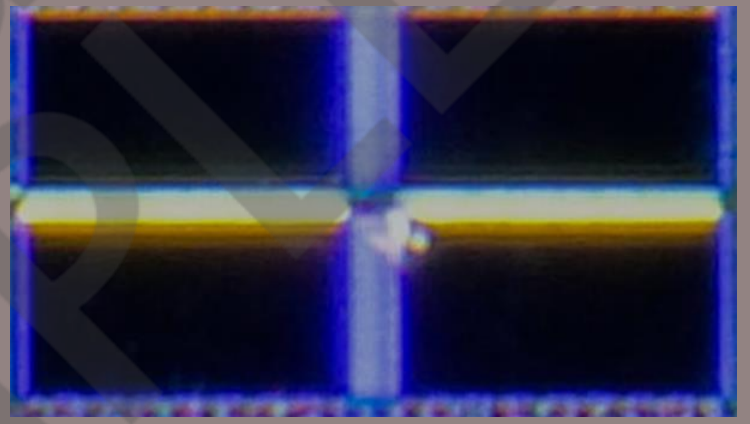


SRAM Density-SRAM IP #2



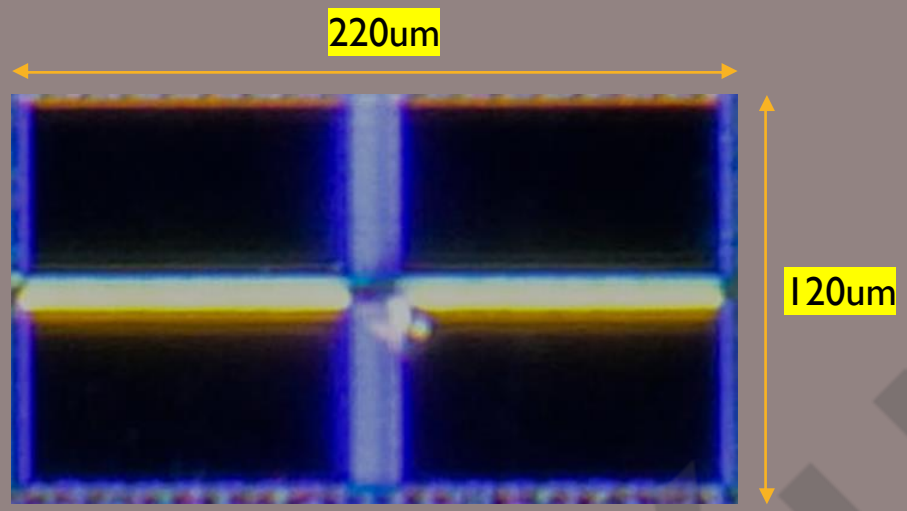
Used SRAM IP #2

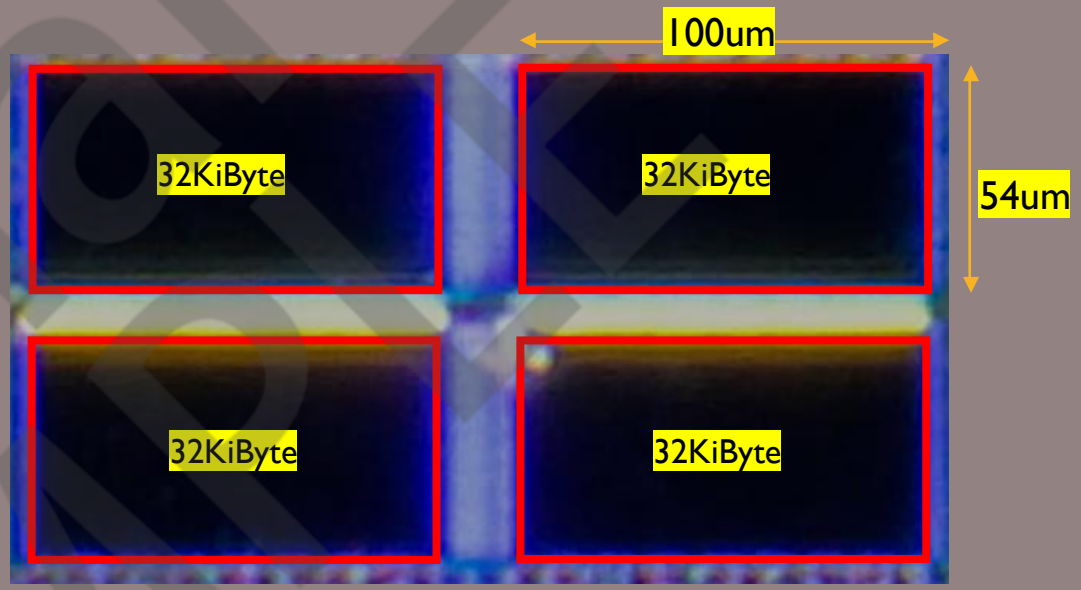
SE: 6MiByte



128KiByte SRAM IP #2

SRAM Density-SRAM IP #2





128KiByte SRAM IP #2

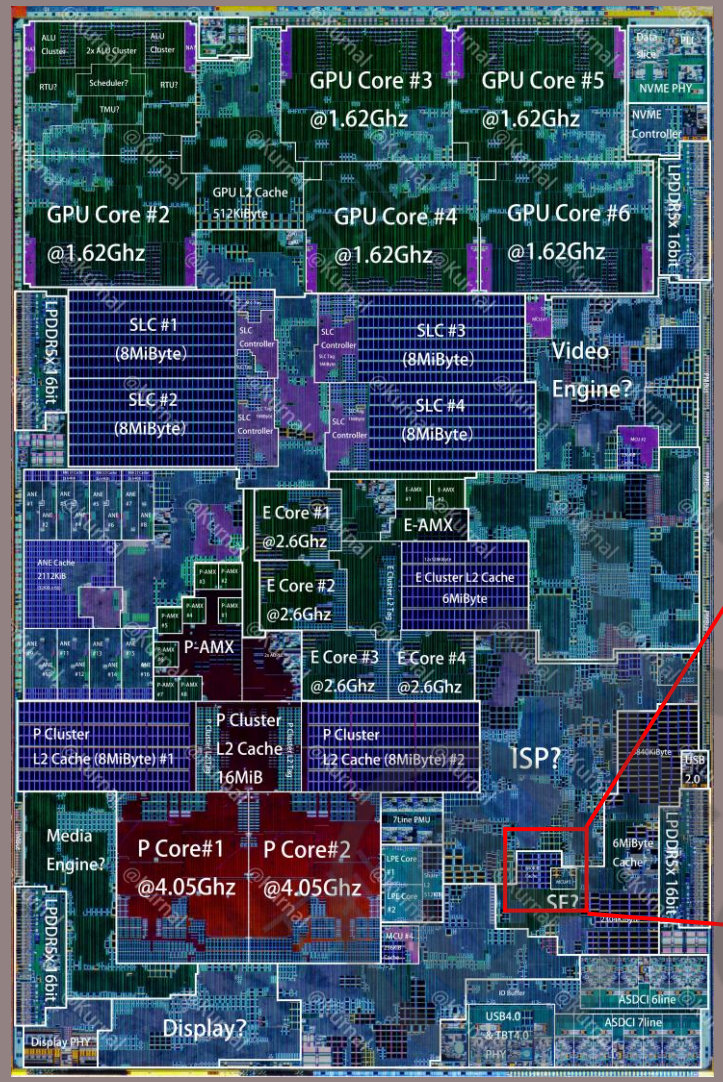
Size: 128KiB

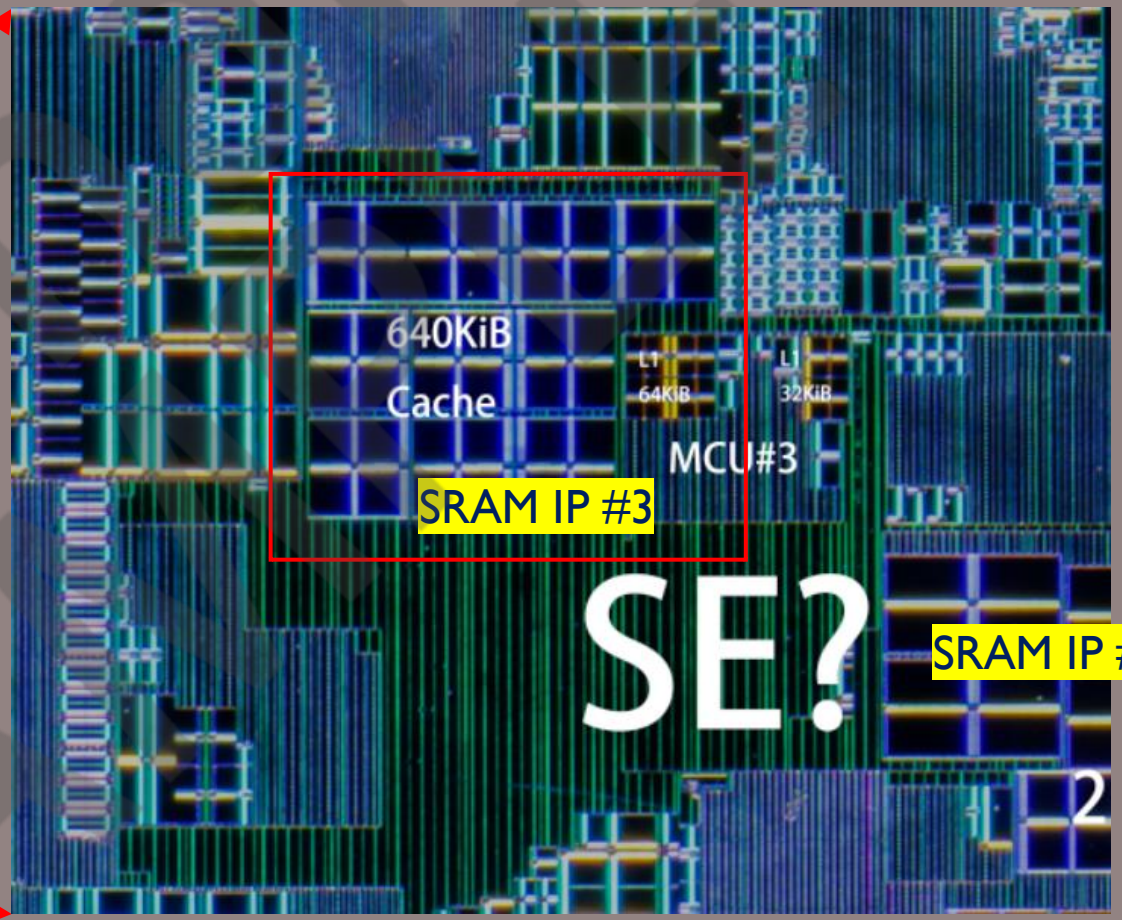
0.0264mm2/128KiB
4,848.48KiB/mm2
37.878Mbit/mm2

Sram bit cell by used: 21600um2
Proportion: 81.818%

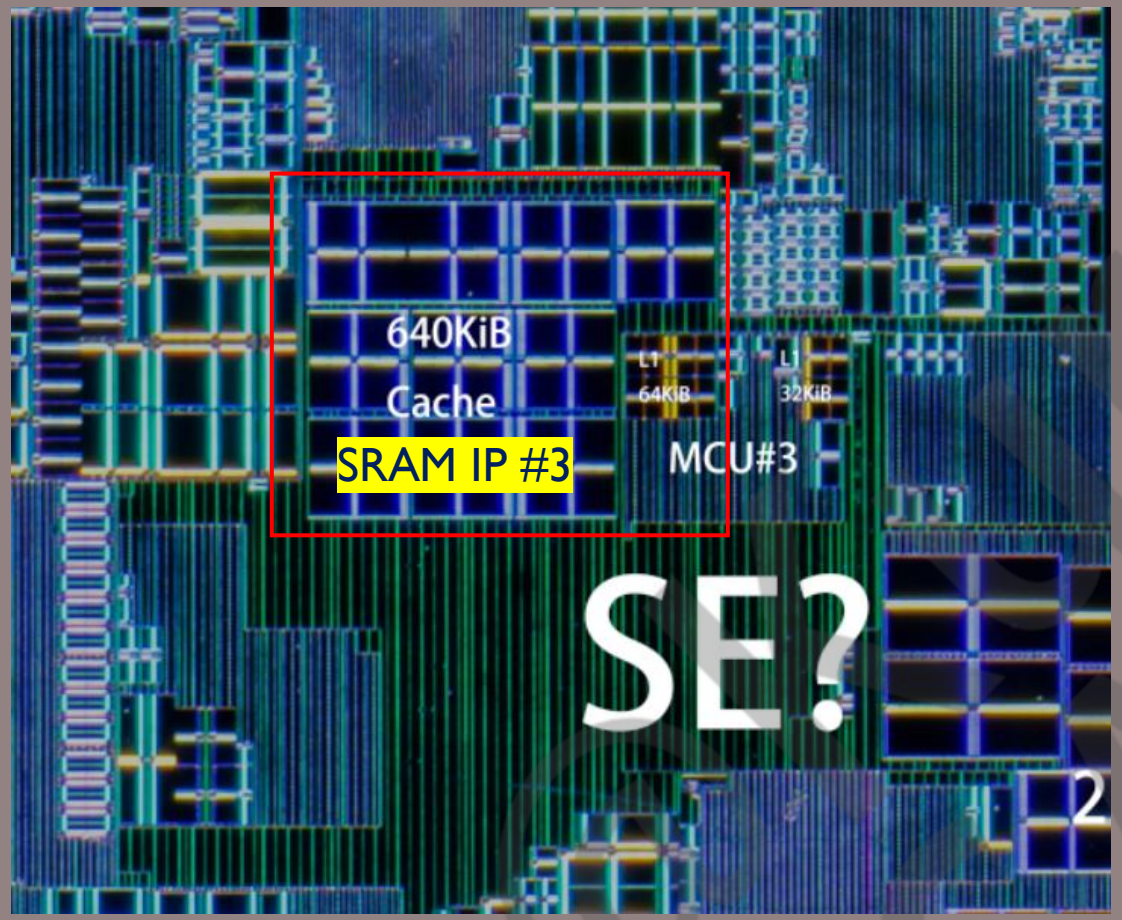
Sram Bit cell Density: 0.020599um2/bit

SRAM Density-SRAM IP #3



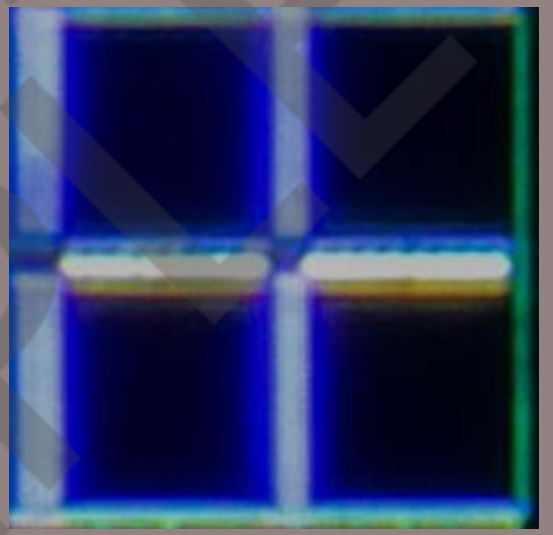


SRAM Density-SRAM IP #3



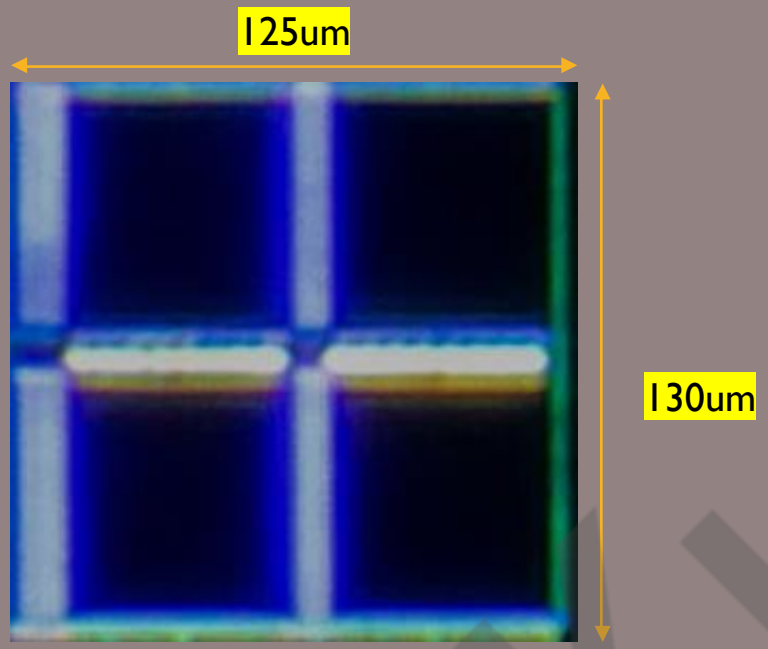
Used SRAM IP #3

Size : 640KiByte



64KiByte SRAM IP #3

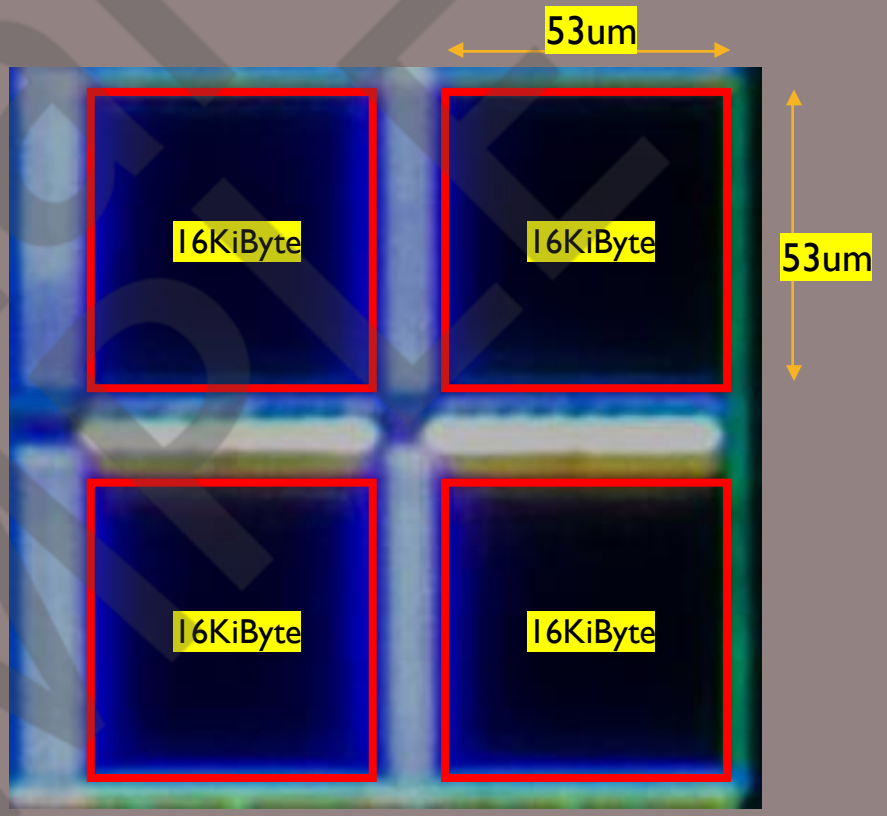
SRAM Density-SRAM IP #3



64KiByte SRAM IP #3

Size: 64KiB

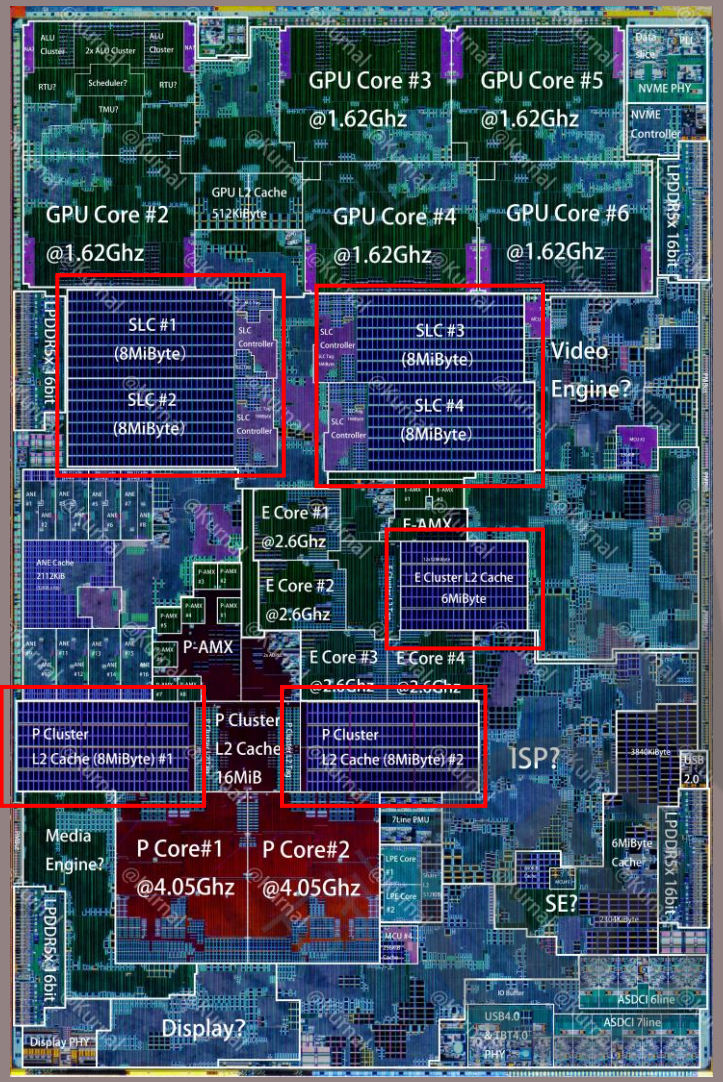
0.01625mm2/64KiB
3,938.46KiB/mm2
30.769Mbit/mm2



Sram bit cell by used: 11,236um2
Proportion: 69.144%

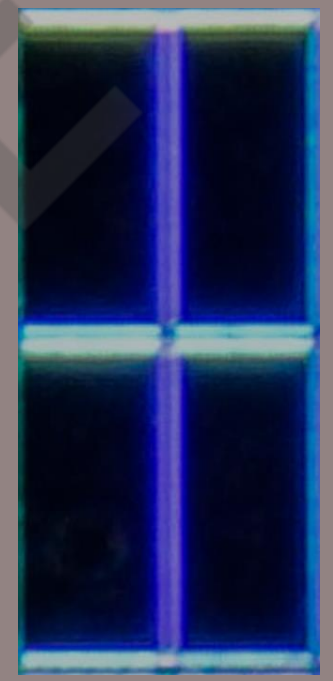
Sram Bit cell Density: 0.02143um2/bit

SRAM Density-END



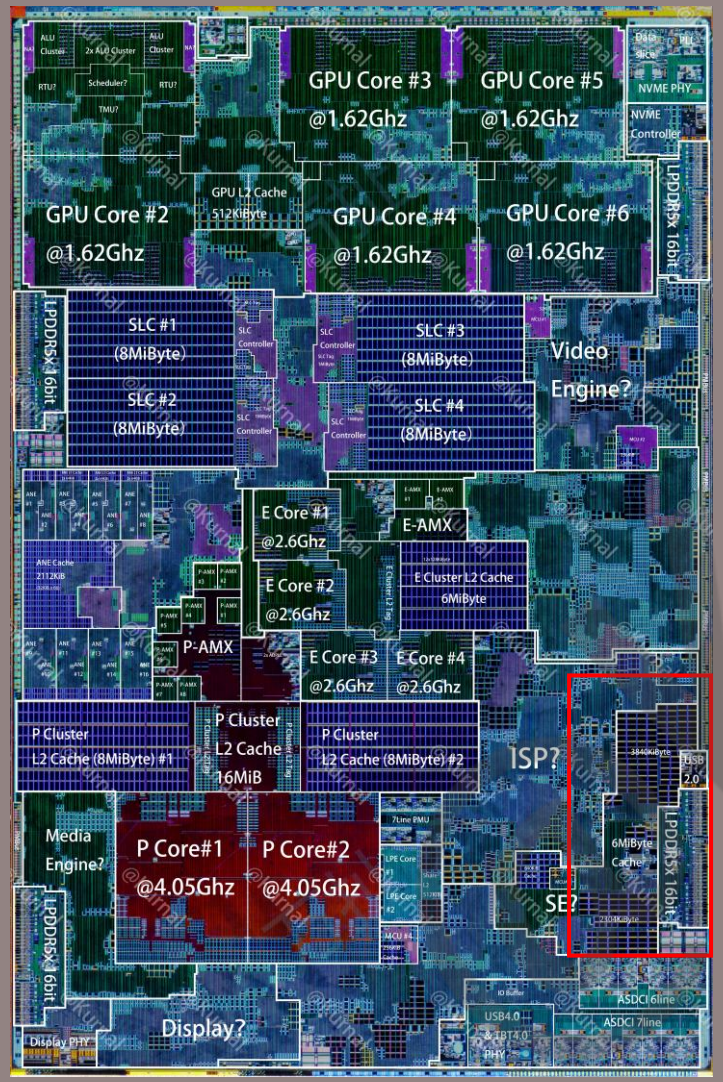
SRAM Block size: 128KiB
Block area: 0.03mm2
Macro Density: 33.33Mibit/mm2

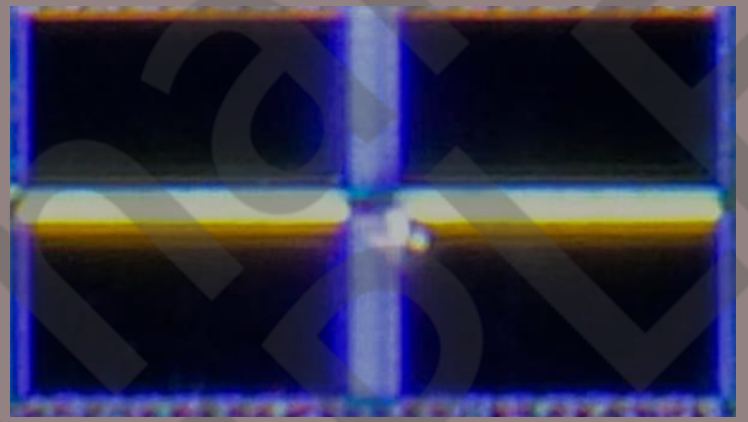
Sram bit cell Proportion: 73.33%
SRAM Bit Cell Density: 0.02098um2/bit



SRAM IP #1

SRAM Density-END

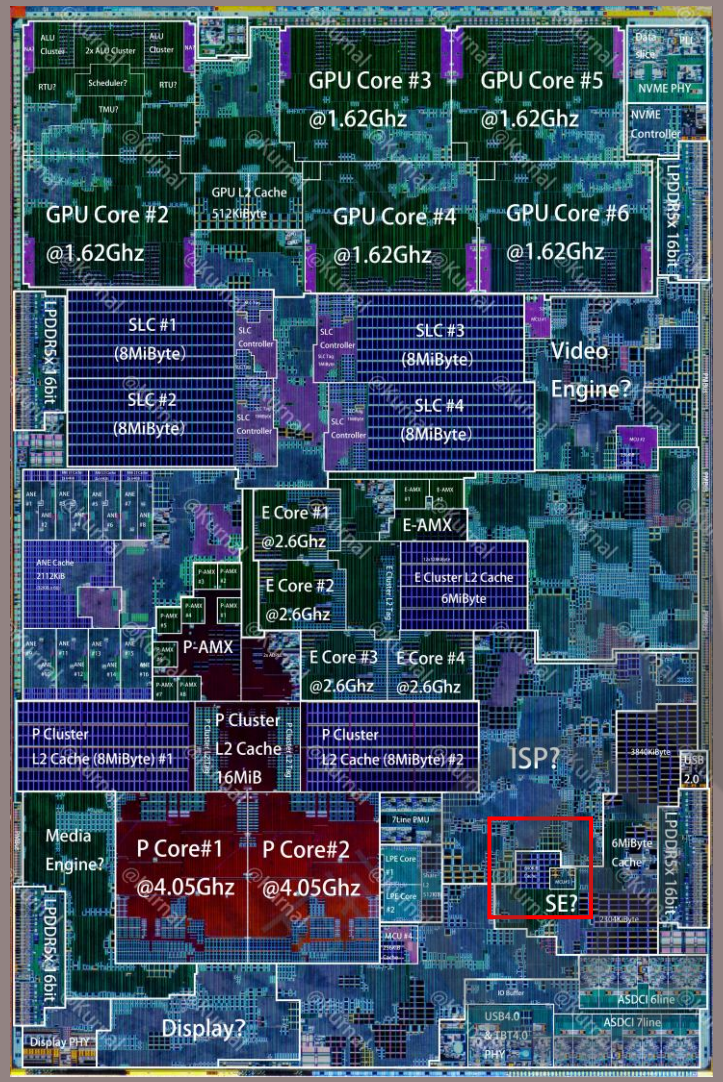


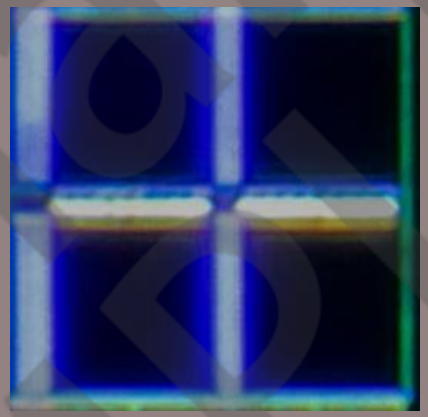


SRAM IP #2

SRAM Block size :	128KiB
Block area :	0.0264mm2
Macro Density :	37.878Mibit/mm2
Sram bit cell Proportion:	81.818%
SRAM Bit Cell Density:	0.020599um2/bit

SRAM Density-END





SRAM IP #3

SRAM Block size: 64KiB
Block area: 0.01625mm2
Macro Density: 30.769Mibit/mm2

Sram bit cell Proportion: 69.144%
SRAM Bit Cell Density: 0.02143um2/bit

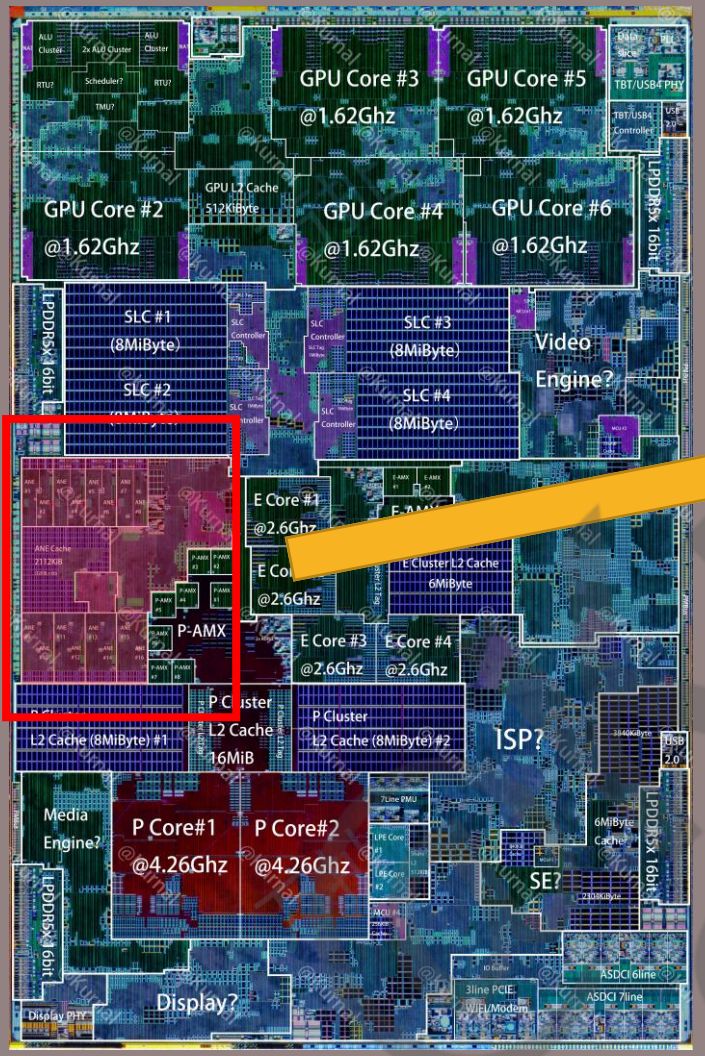
On chip analyze-GPU

A19Pro

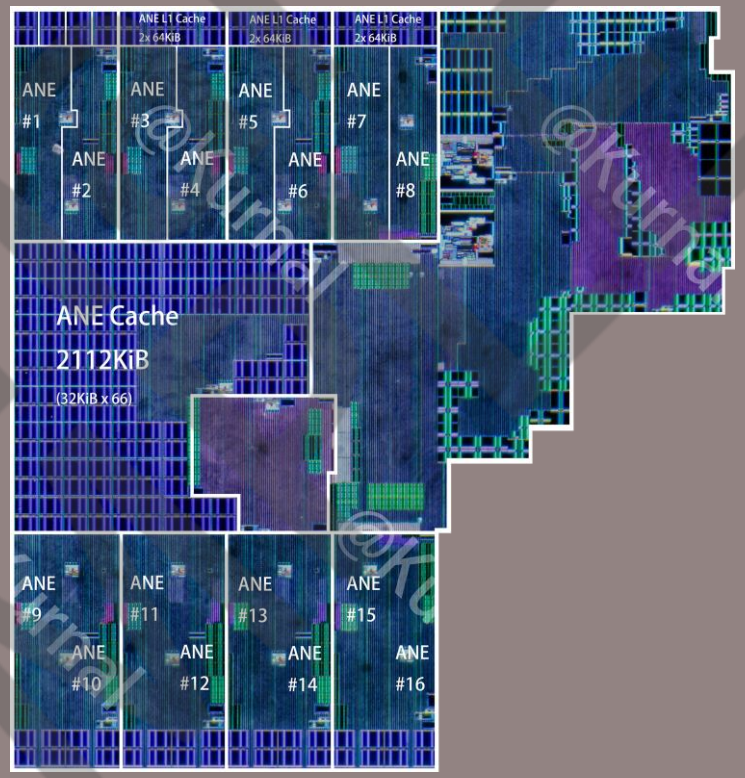
On chip analyze-NPU

A19Pro

On chip analyze-NPU



@A19pro



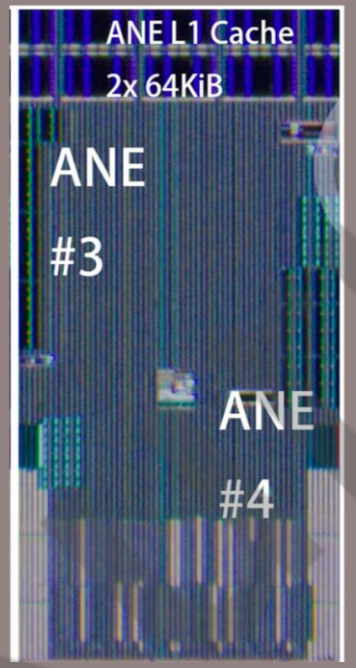
ANE @A19pro

The A19 Pro's NPU (ANE) retains the legacy physical floorplan, situated consistently below the SLC and above the P-Core cluster.

ANE Core @A19pro

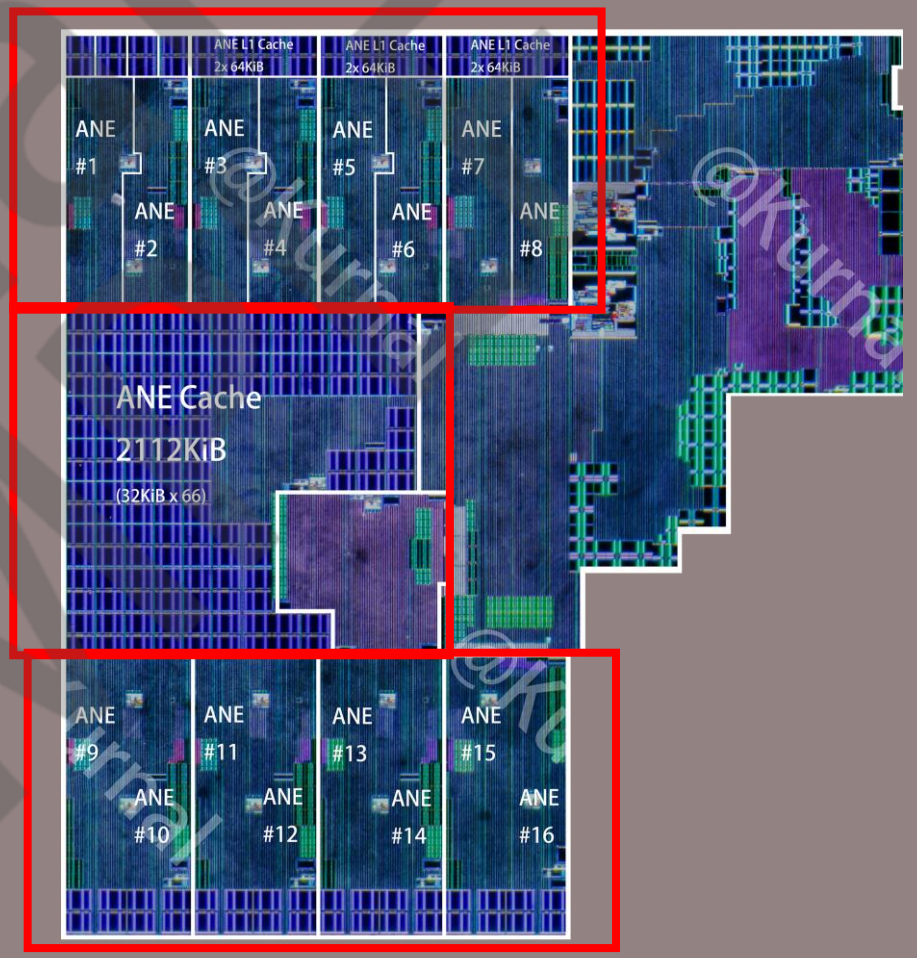
0.15mm2

Core Area: -20%



ANE Core @A18pro

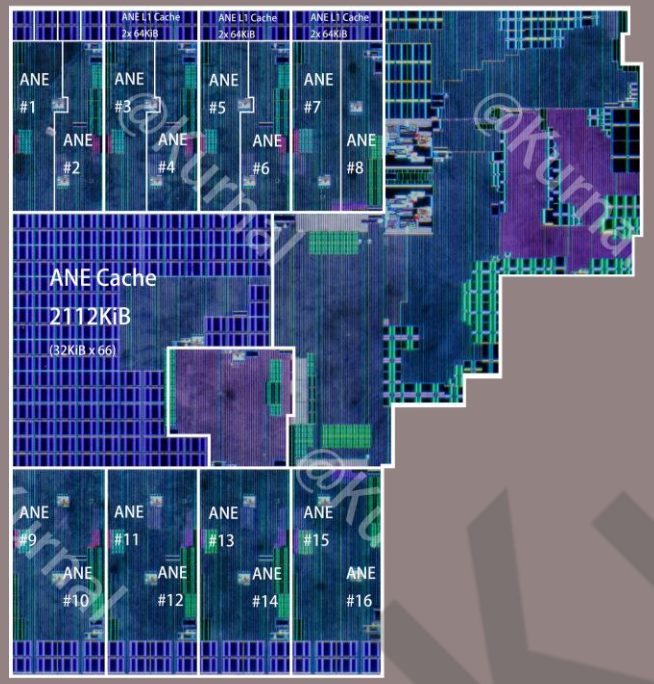
0.1875mm2



ANE @A19pro

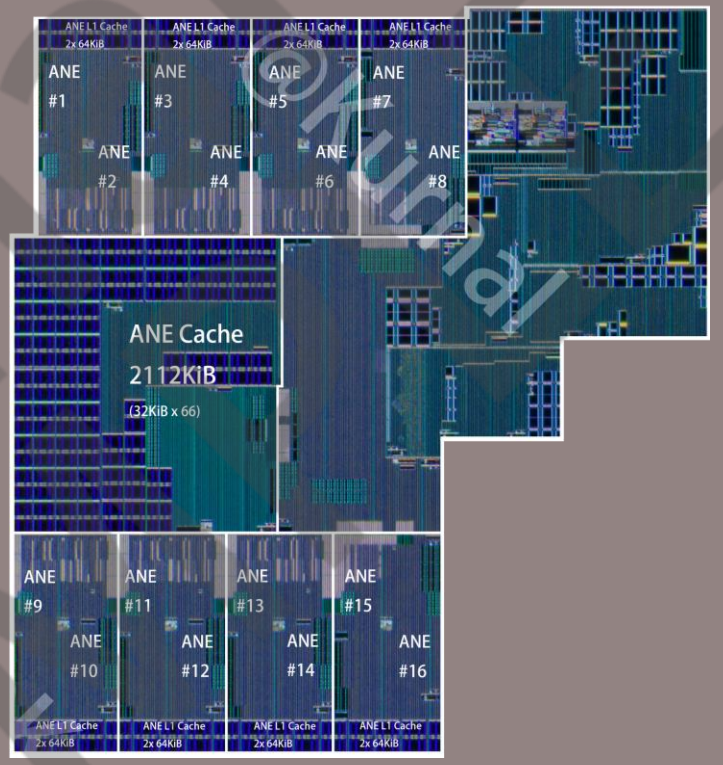
A19 Pro ANE remains 16-core.
It keeps the 2112KiB shared cache and 16KiB L1 cache per core.
Single-core area dropped 20%, from 0.1875mm² to 0.15mm²

On chip analyze-NPU



ANE @A19pro

5.216mm2



ANE @A19pro

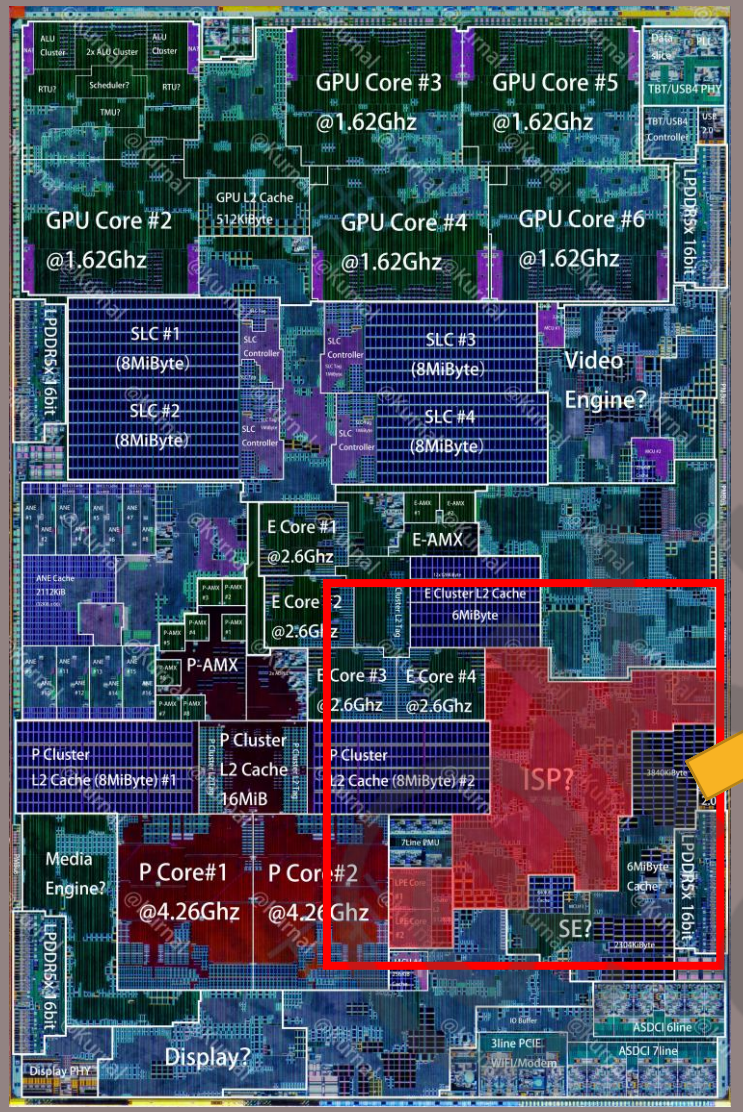
6.9mm2

Total NPU area shrank by 1.274mm² to 5.216mm²

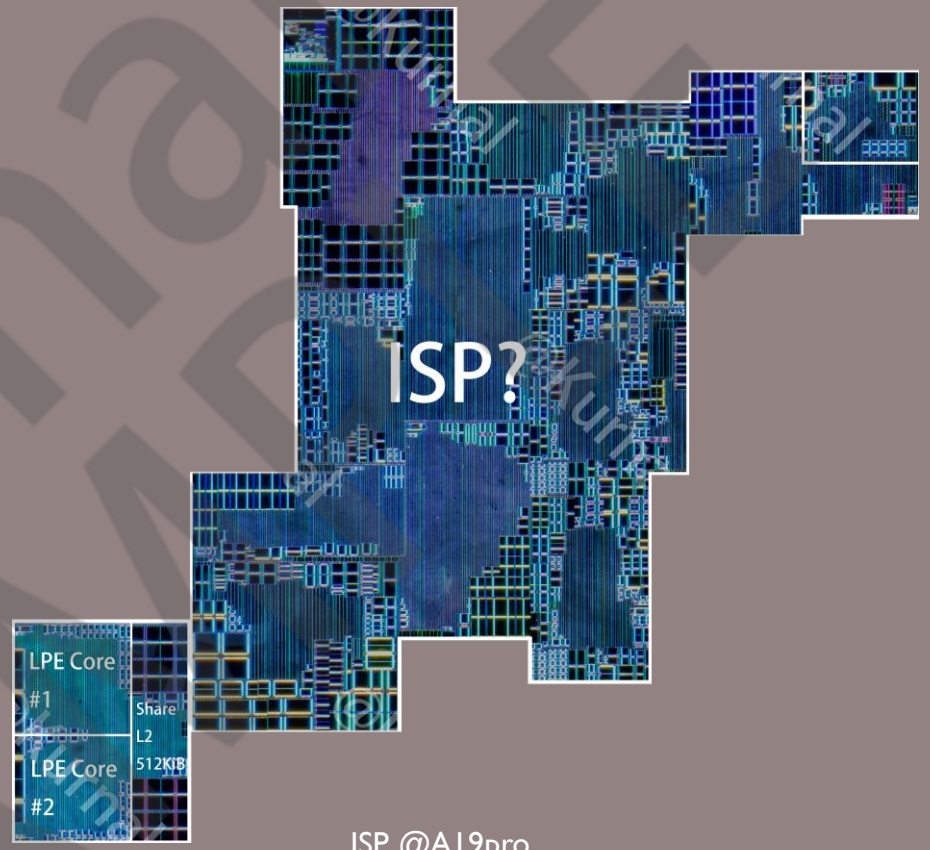
On chip analyze-ISP

A19Pro

On chip analyze-ISP



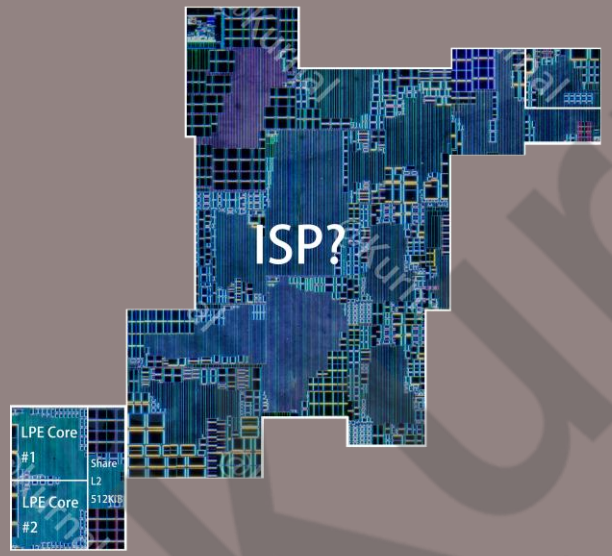
@A19pro



ISP @A19pro

The A19 Pro's ISP unit is located in the upper-right region of the CPU P-Core

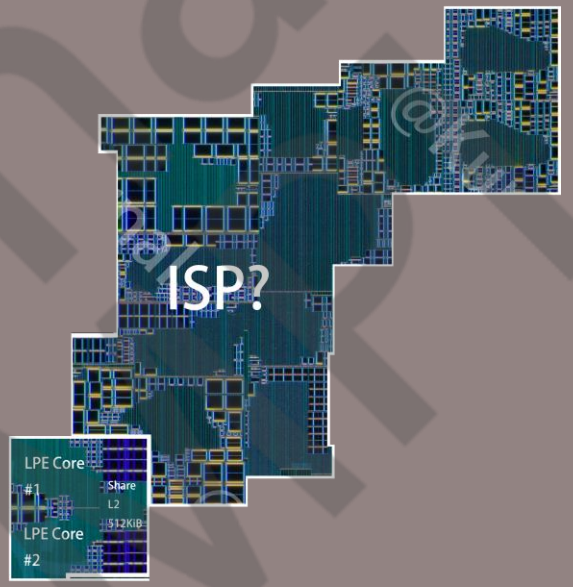
A19Pro ISP



ISP @A19pro

5.491mm2

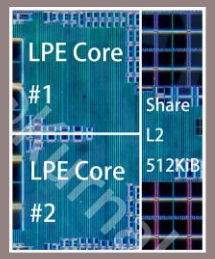
A18Pro ISP



ISP @A18pro

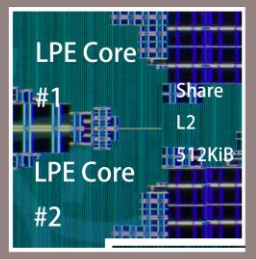
5.586mm2

The ISP area of the A19 Pro has decreased from the A18 Pro's 5.586mm2 to 5.491mm2, a slight reduction of approximately 1.7%



A19Pro ISP Core

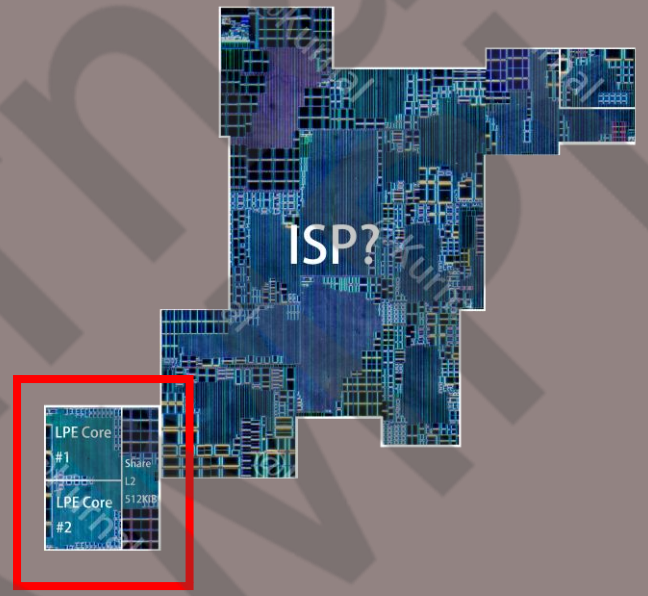
0.63mm2



A18Pro ISP Core

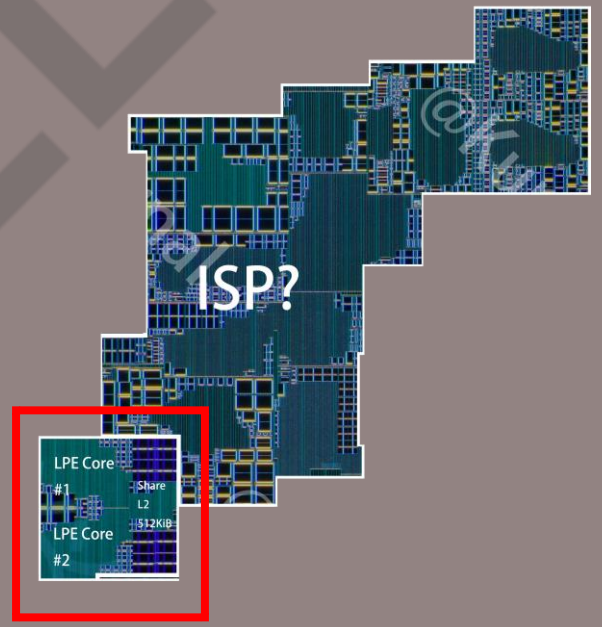
0.756mm2

A19Pro ISP



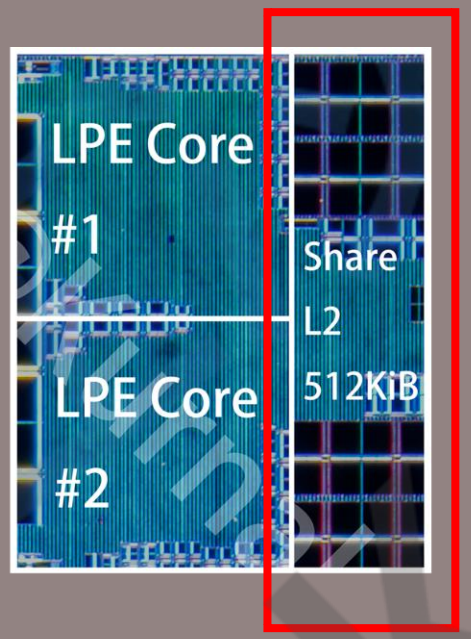
ISP @A19pro

A18Pro ISP

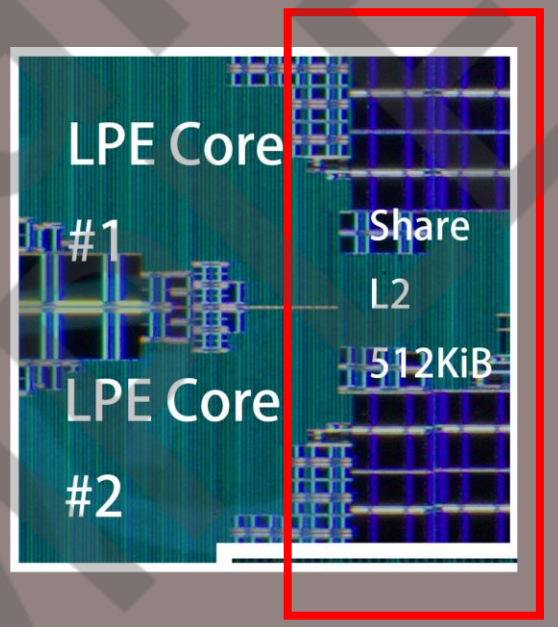


ISP @A18pro

The two ISP CPU cores (LPE cores) situated at the bottom-left of the ISP saw a more significant reduction,
Shrinking from 0.756mm² to 0.63mm² (an approximately 16.7% decrease)



ISP CPU Core @A19pro



ISP CPU Core @A18pro

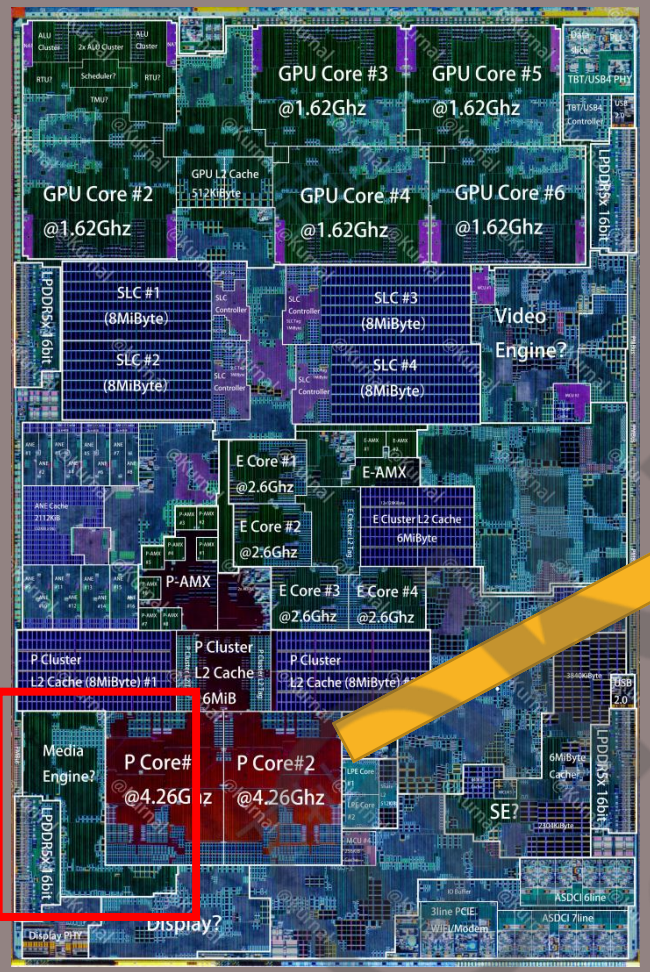
The A19 Pro features dual LPE cores with a total area of 0.63mm2 a slight reduction from the A18 Pro's 0.756mm2.

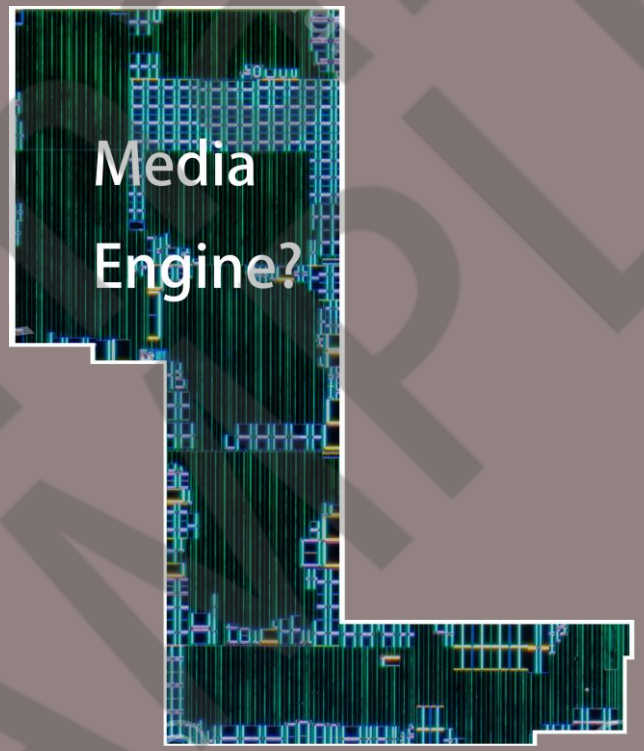
The individual core size has decreased from 0.25mm2 to 0.21mm2, while maintaining a dual-core shared 512KiB L2 cache configuration.

On chip analyze-Media Engine

A19Pro

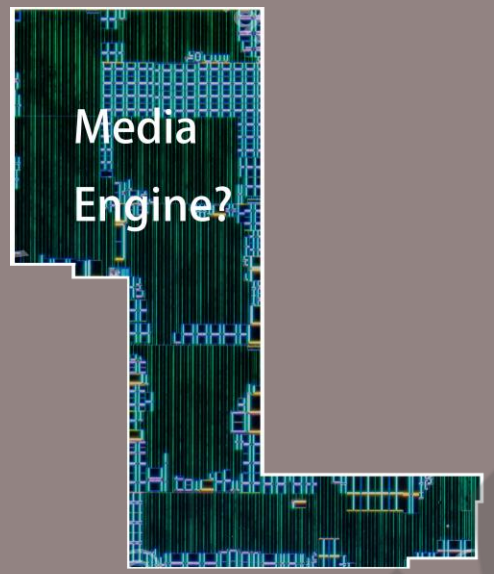
On chip analyze-Media Engine





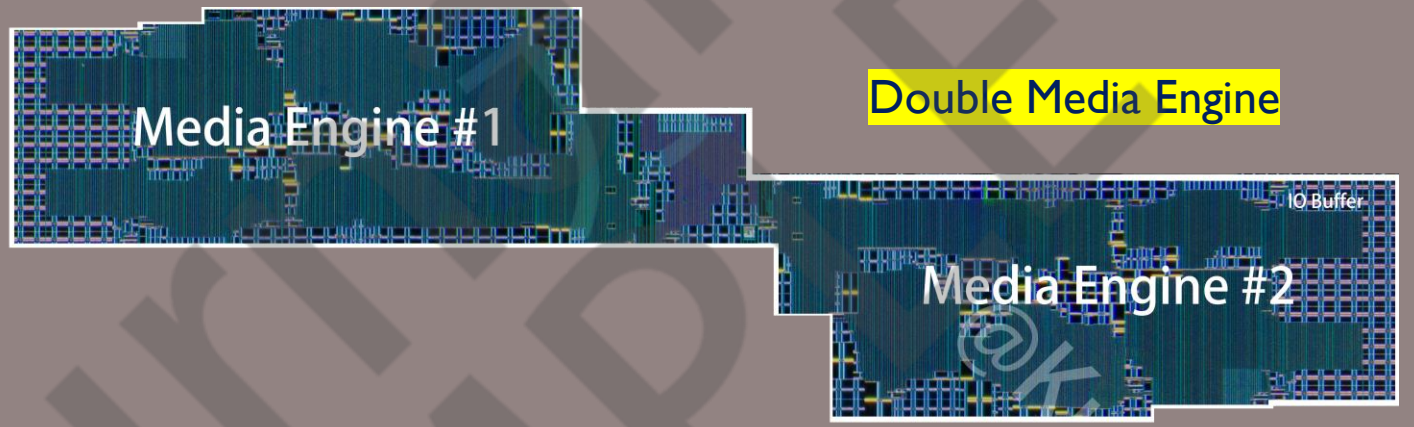
The Media Engine unit is located in the bottom-left region of the chip, adjacent to the P-Core cluster;

On chip analyze-Media Engine



Media Engine @A19pro

2.264mm2



Media Engine @A18pro

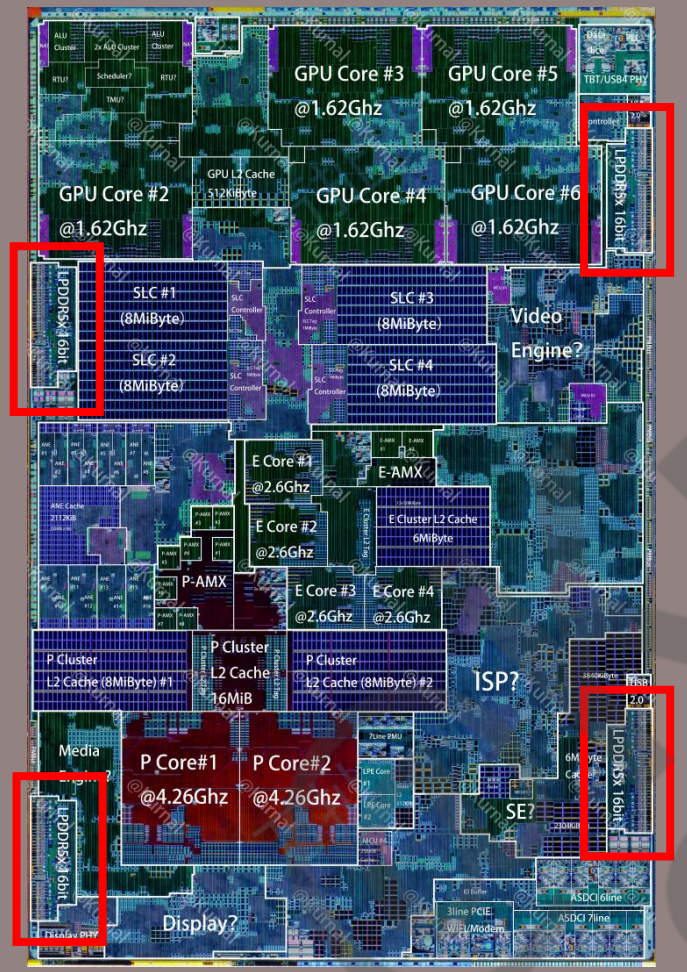
5.3mm2

The A19 Pro Media Engine has been streamlined from the A18 Pro's dual-unit design (totaling 5.3mm2) to a single unit of 2.264mm2, representing an area reduction of approximately 57.3%.

On chip analyze-LPDDR PHY

A19Pro

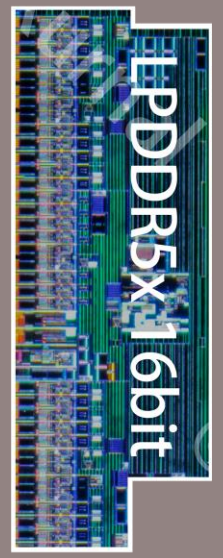
On chip analyze-Media Engine



The A19 Pro continues to utilize a 4 x 16-bit LPDDR5X PHY with each individual PHY occupying an area of just 0.854mm2

A19Pro

LPDDR5X PHY



0.854mm2

A18Pro

LPDDR5X PHY

1.125mm2

The memory controller region also achieves a footprint reduction.

The A19 Pro continues to use LPDDR5X, the area of a single PHY has decreased from 1.125mm2 to 0.854mm2

resulting in a total saving of 1.084mm2 across all four PHYs

4x LPDDR PHY