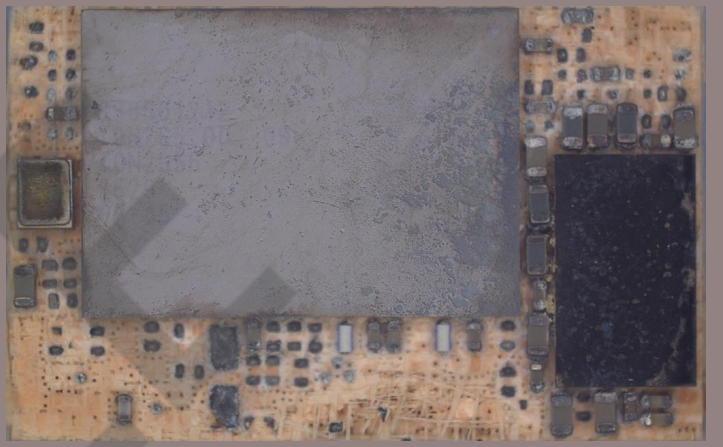
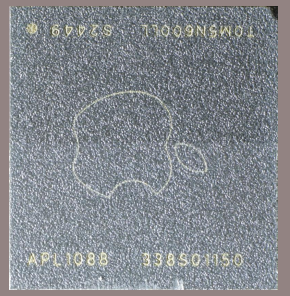
Apple
C1 & N1

Chip analyze

V1





@Kurnal

Version	Date	Updates	Author
V0.1	2025/12/22 16:32	Working	Kurnal
V0.2	2025/12/22 19:26	Finish C1	Kurnal
V1	2025/12/26 23:27	Finish N1	Kurnal

About Authors

This Report is made From @Kurnal

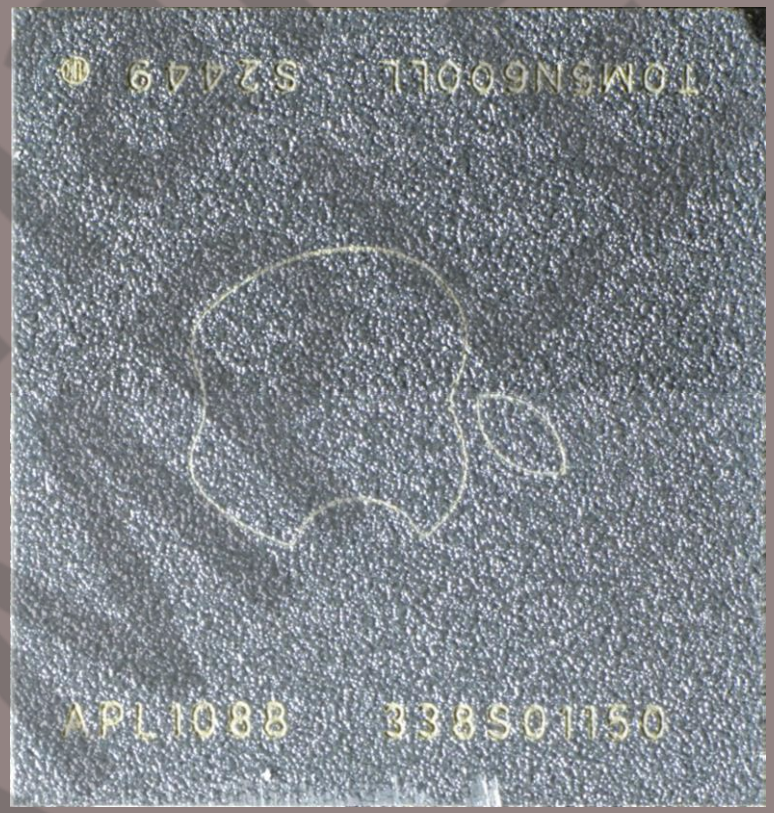
BiliBili: @Kurnal
X: @Kurnalsalts
WeChat: KurnalWeChat

C1 Analyze

Package

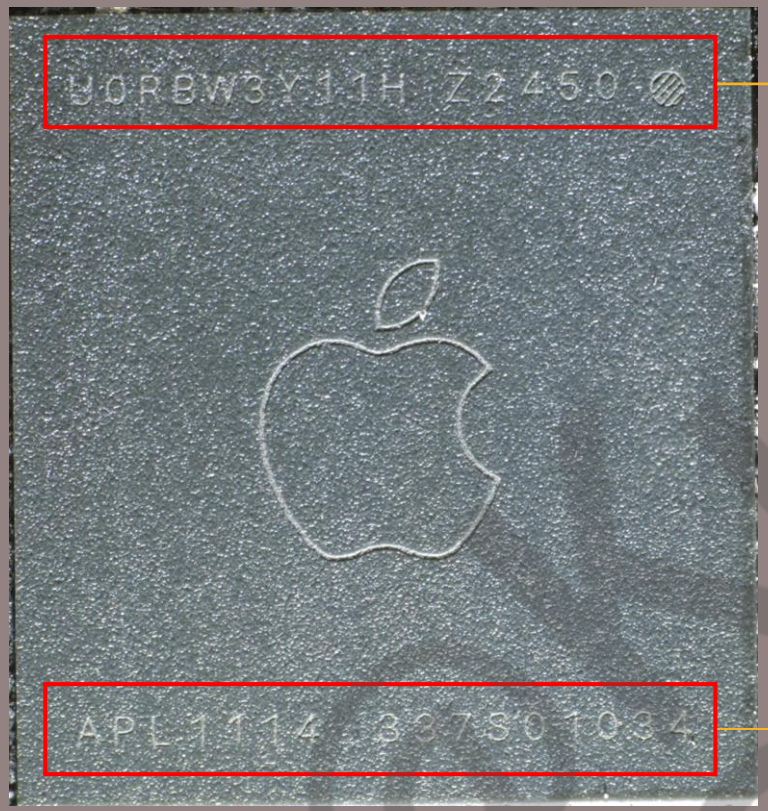
Apple C1-Package analyze

APL1114 Frontside



APL1088 Frontside

Apple C1-Package analyze-Top Mark

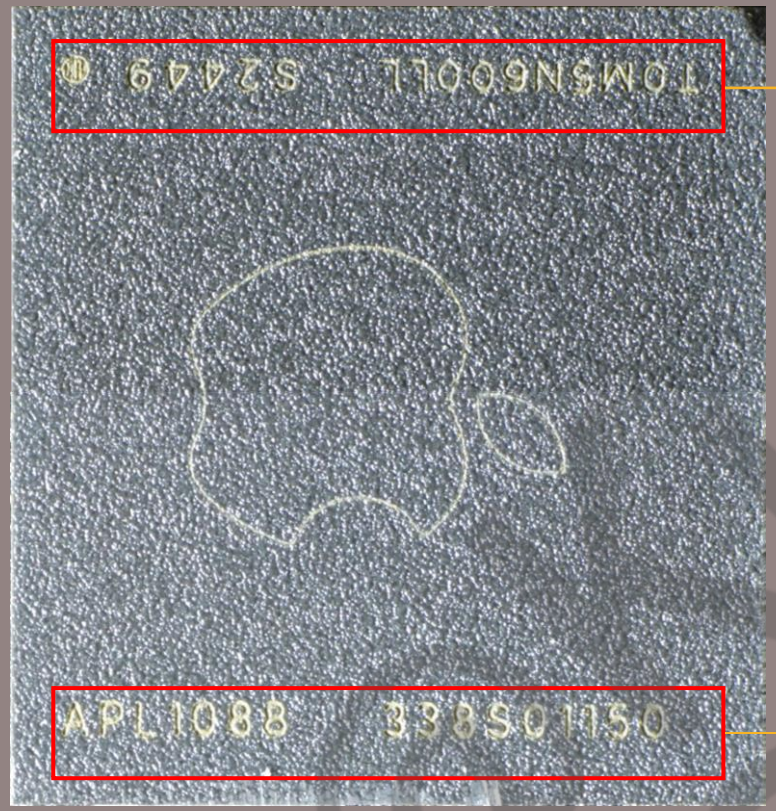


APL1114 Frontside

Product name: APL 1114

Made/Package data: Year 2024 Week 50

Apple C1-Package analyze-Top Mark



APL1088 Frontside

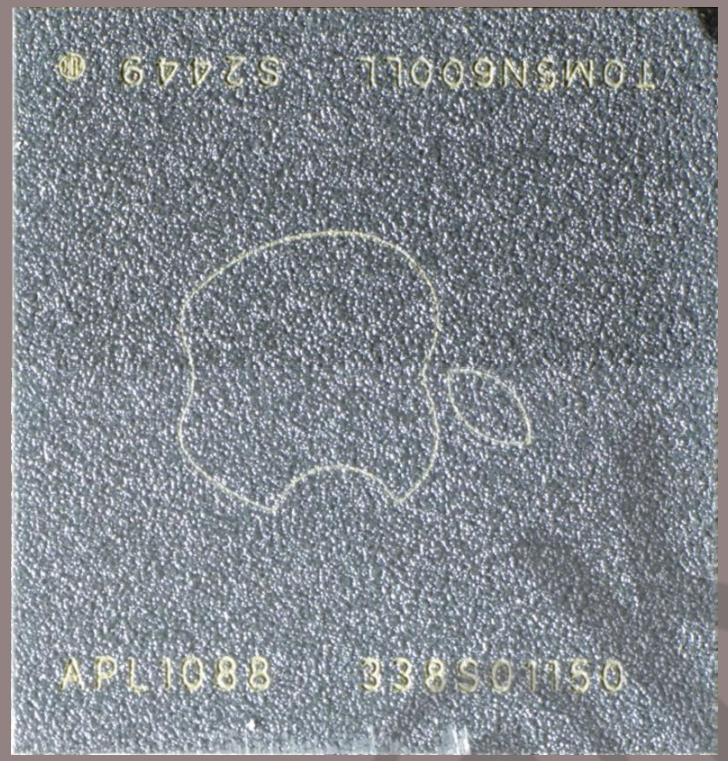
Product name: APL 1088

Made/Package data: Year 2024 Week 49

C1 Analyze

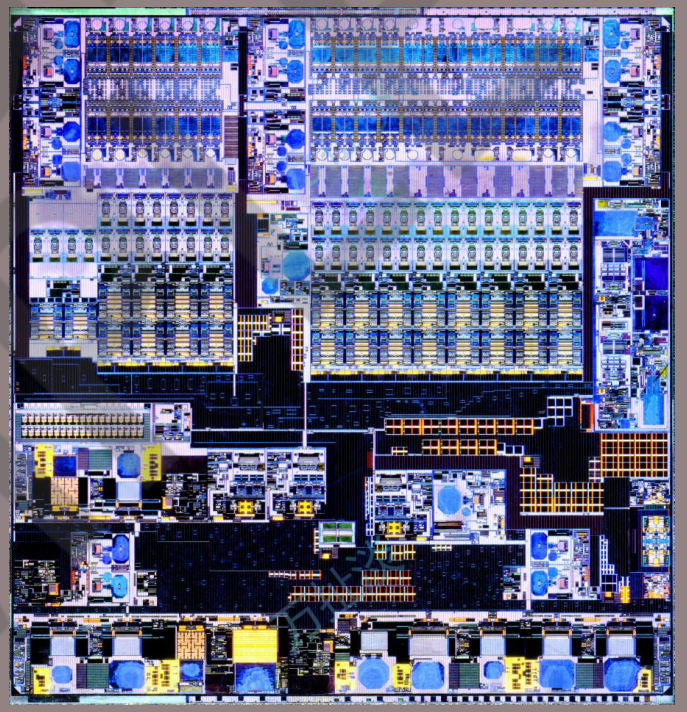
Decap

Apple C1-Decap-APL1088



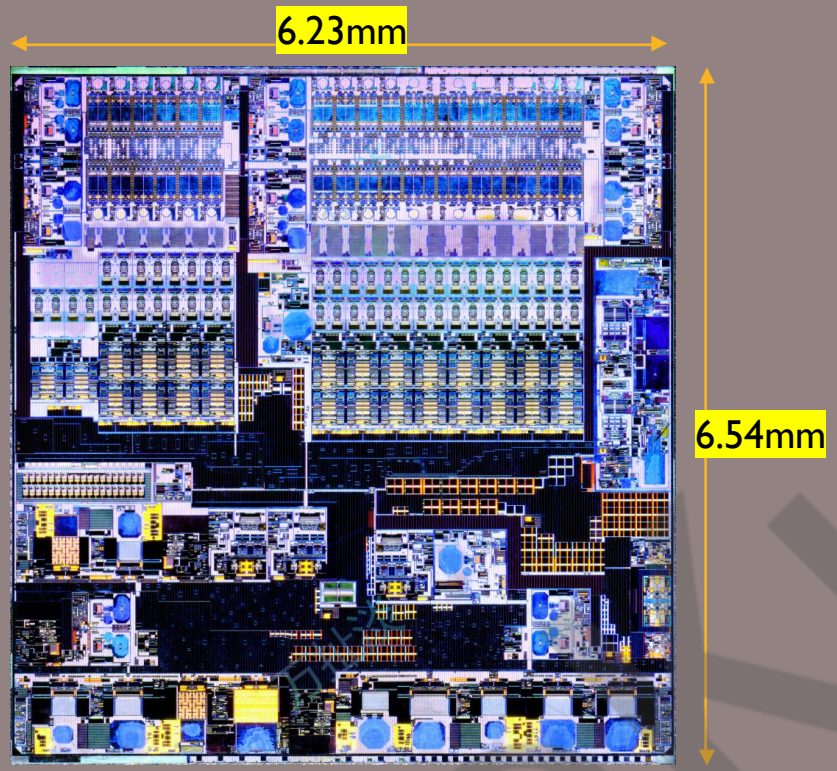
APL1088 Frontside

Decaped



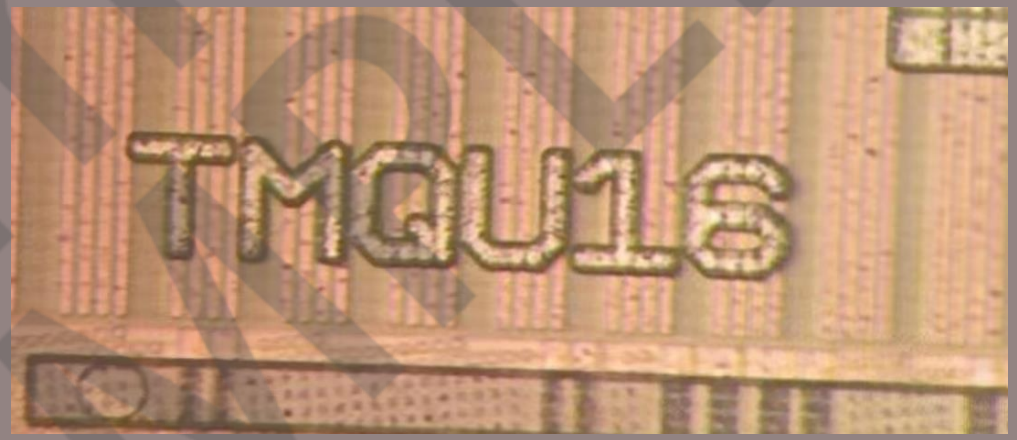
APL1088 Dieshot

Apple C1-Decap-APL1088



APL1088 Dieshot

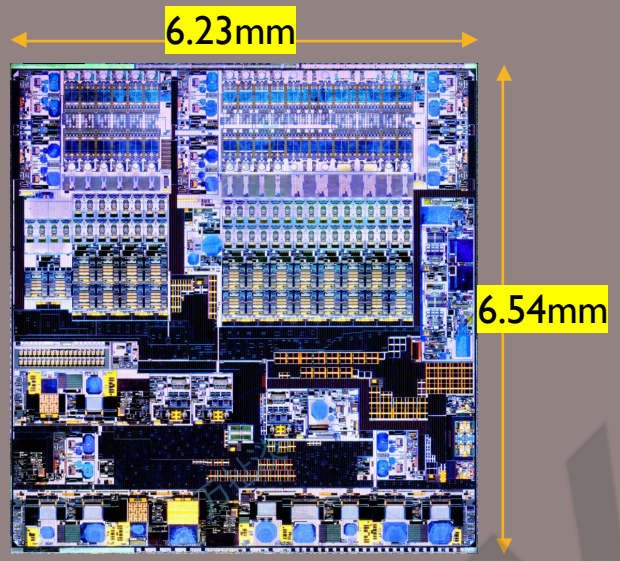
Die size: 40.7442mm2
Die Thickness: 130um
with out seal ring: 6.19mm x 6.38mm



Die Mark : TM QU16

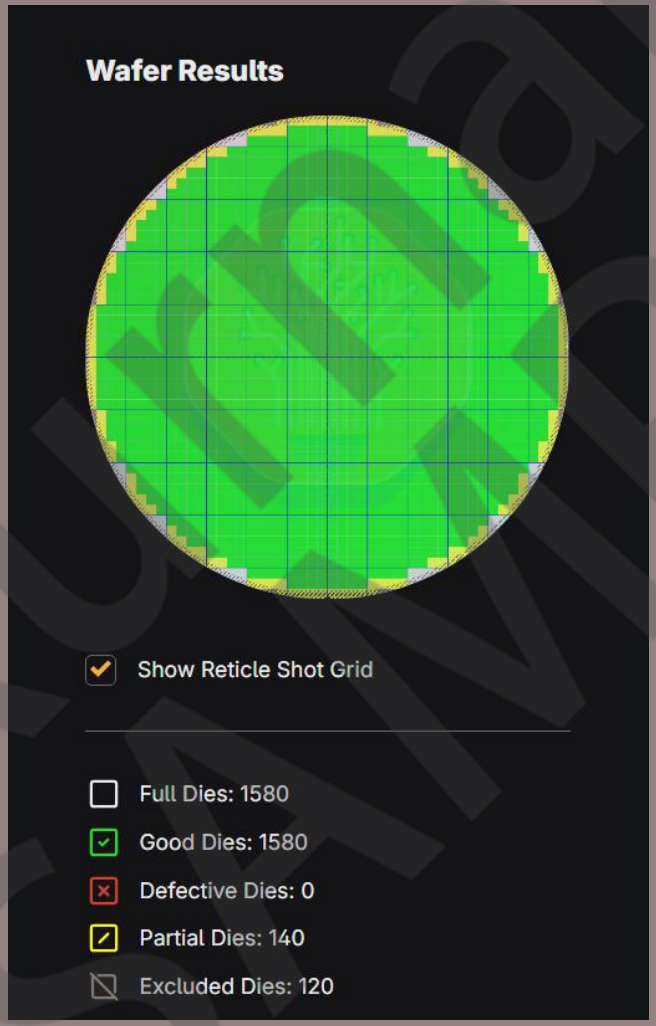
TSMC Tap Out Mark
Tap Out in year 2022/2023

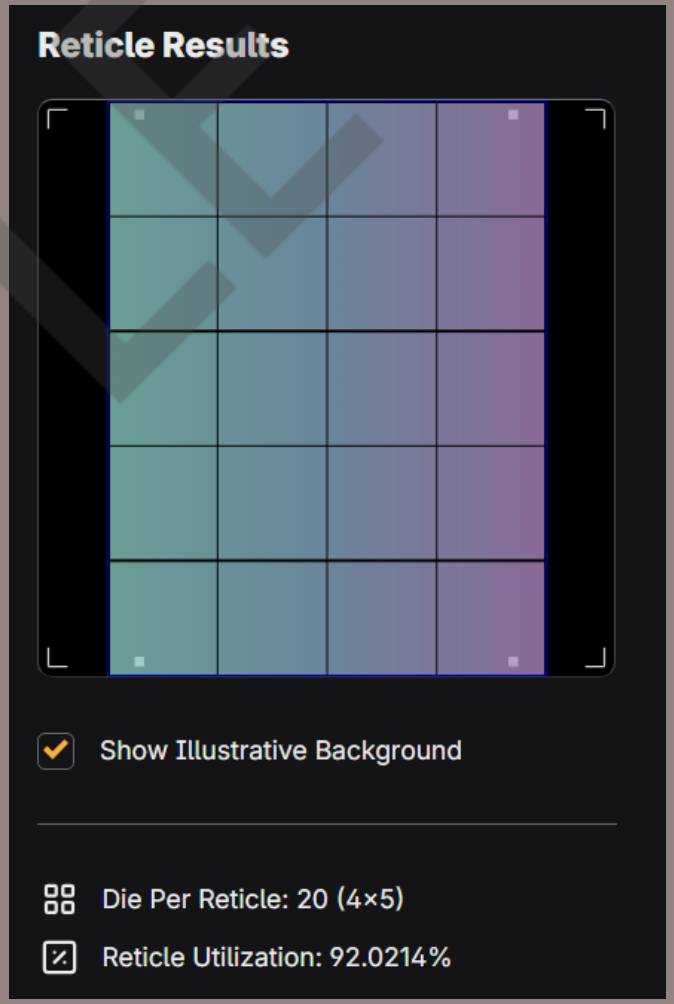
Apple C1-Decap-APL1088



APL1088 Dieshot

Die size: 40.7442mm2
Die Per Wafer: 1580
Die Per Mask: 20:1

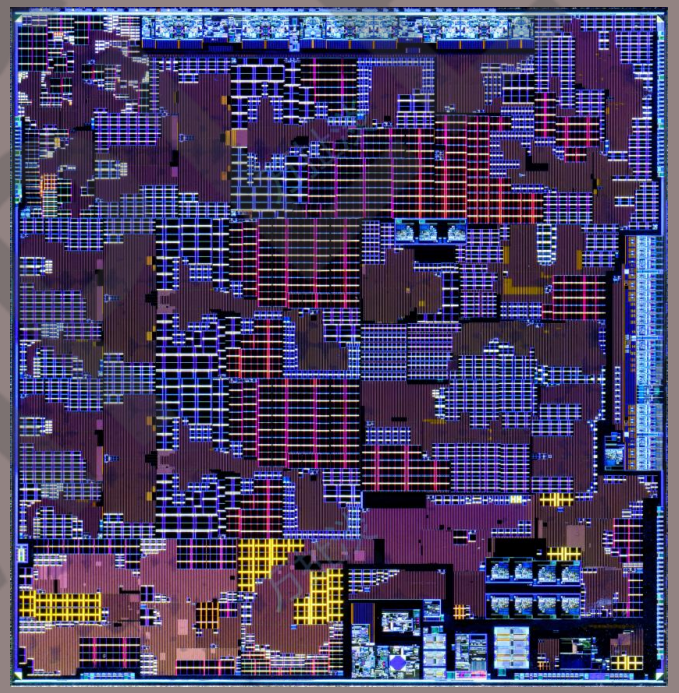




Apple C1-Decap-APL1114

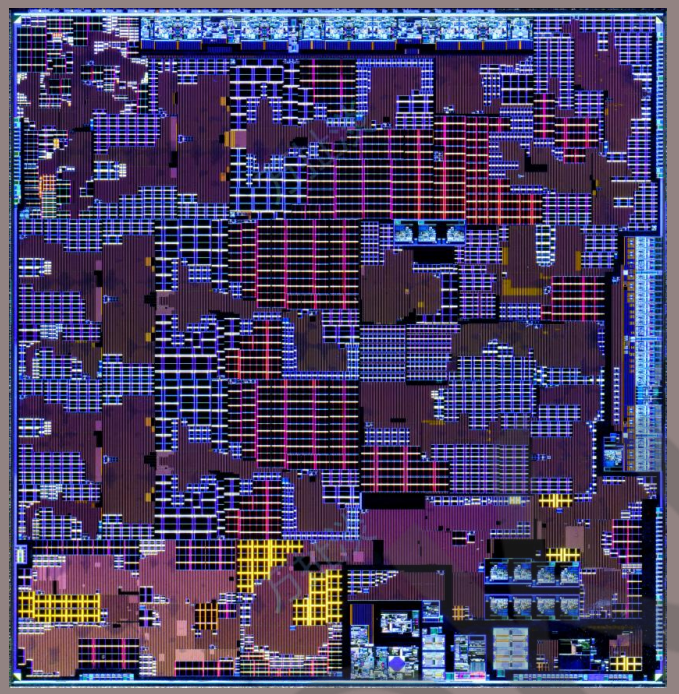
APL1114 Frontside

Decaped



APL1114 Dieshot

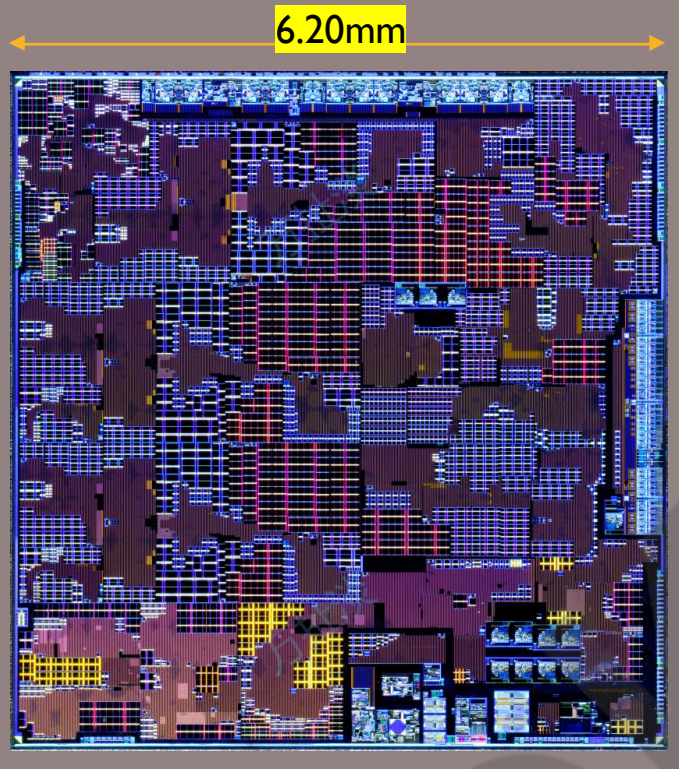
Apple C1-Decap-APL1114



APL1114 Dieshot

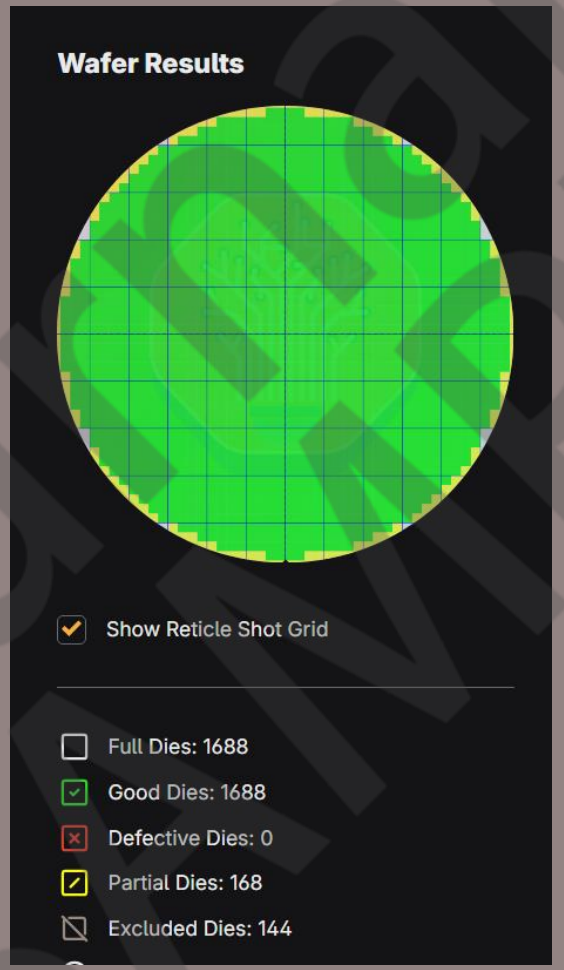
Die size:	39.80mm2
Die Thickness:	100um
with out seal ring:	6.14mm x 6.32mm
Die Mark :	Not Found

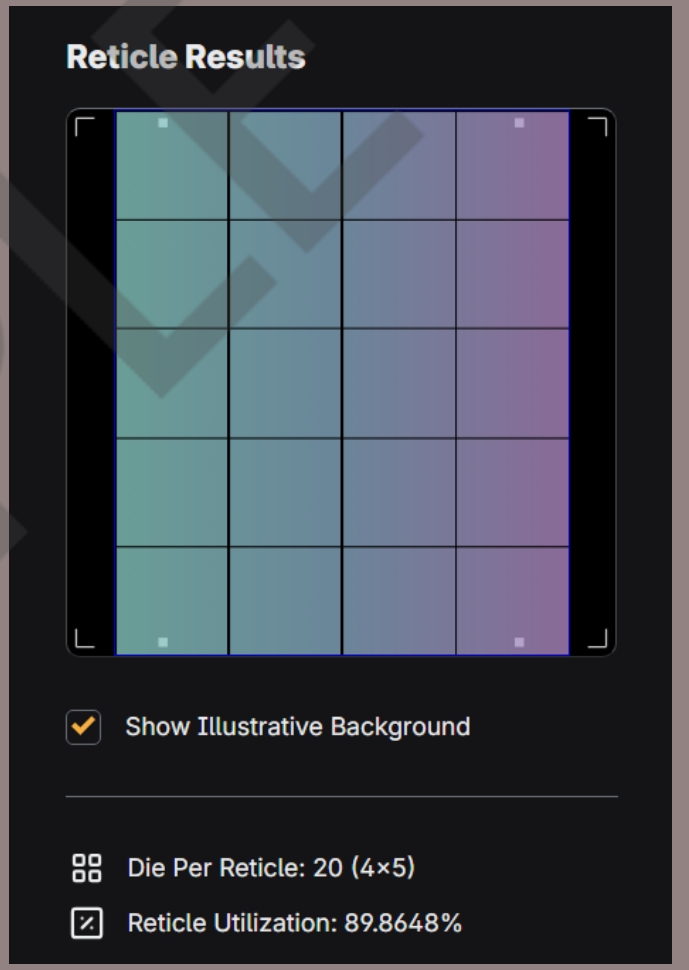
Apple C1-Decap-APL1114



APL1114 Dieshot

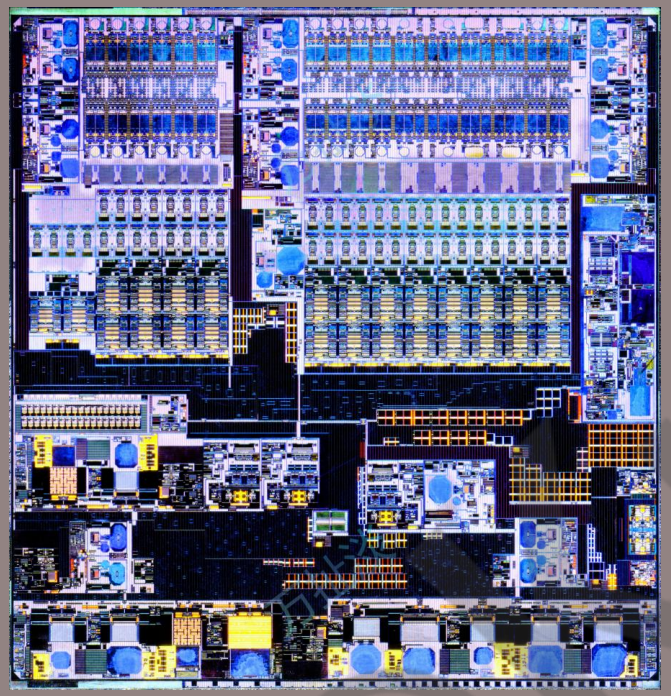
Die size: 39.8mm2
Die Per Wafer: 1688
Die Per Mask: 20:1





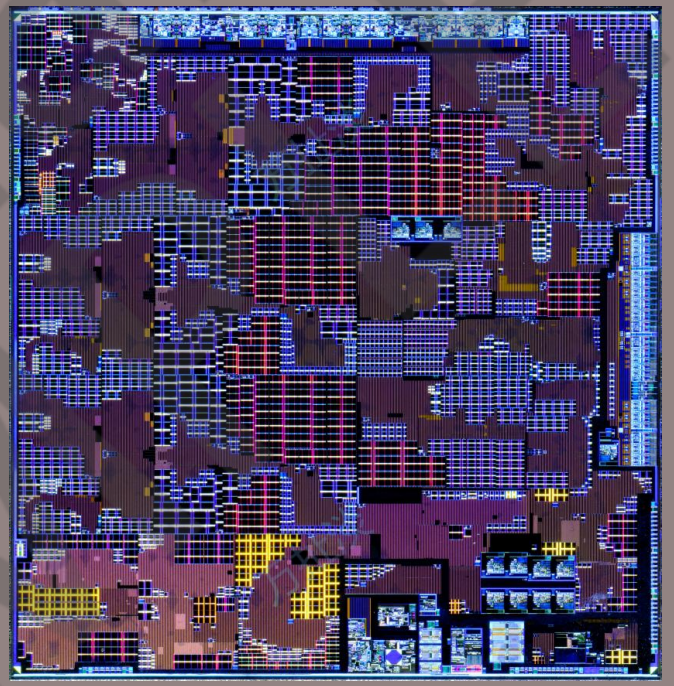
Apple C1-Decap

APL1088 Frontside



C1 RF Chip

APL1114 Frontside

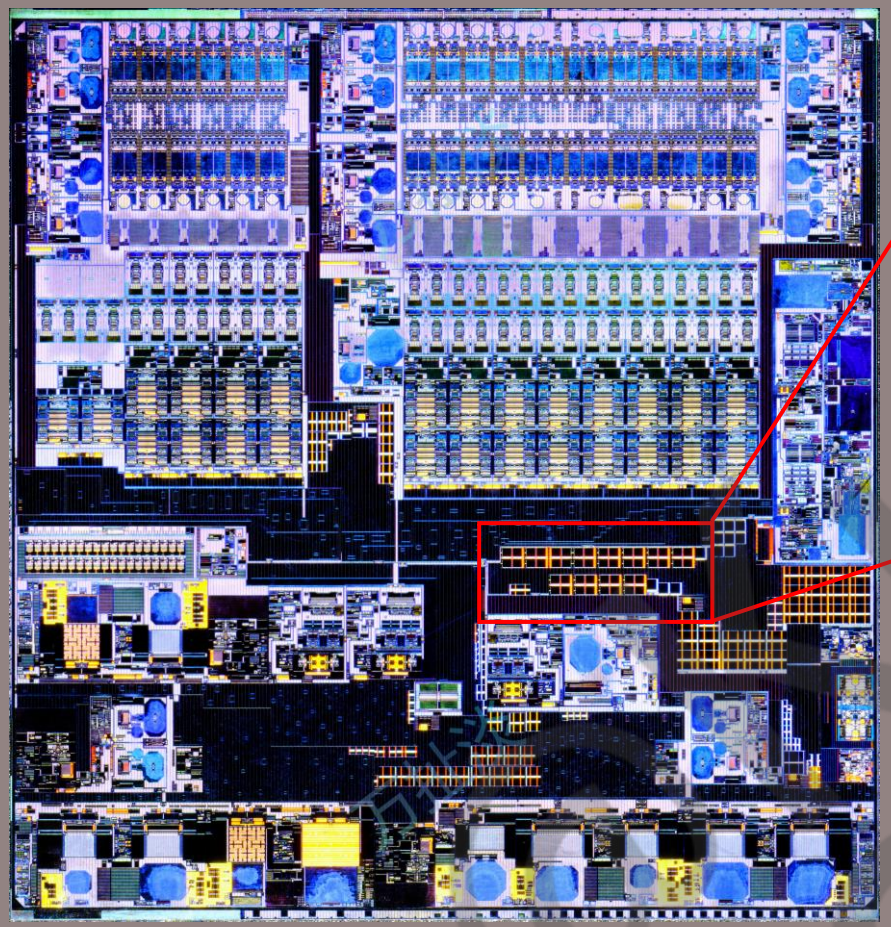


C1 Modem Chip

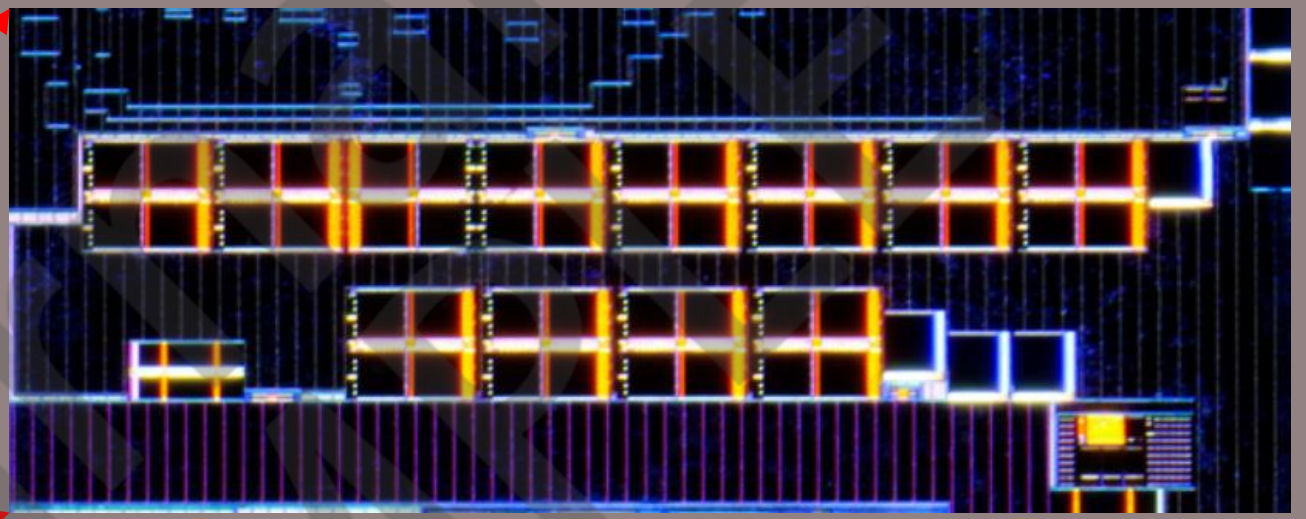
Process identification

APL1088/APL1114

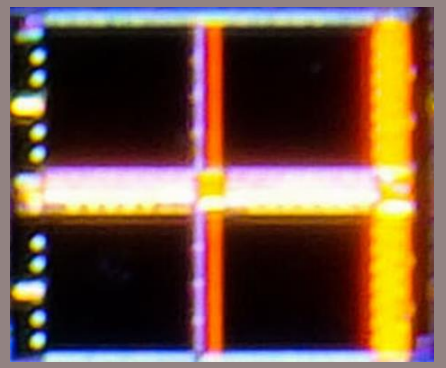
Process identification-APL1088



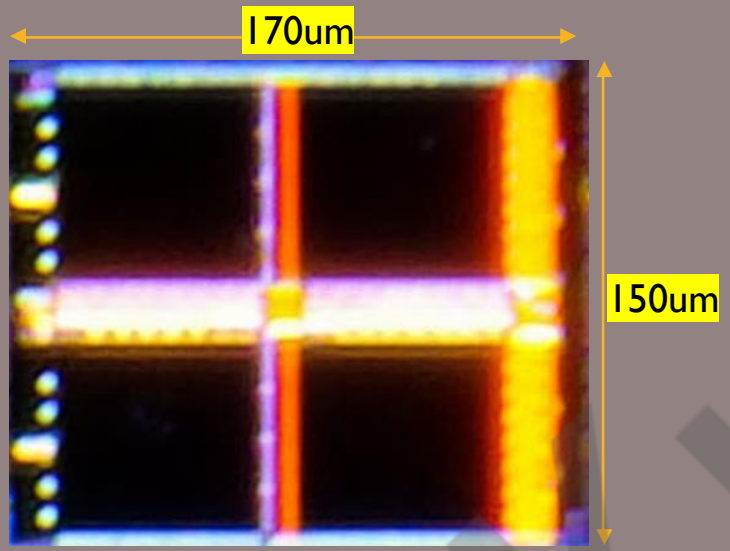
APL1088 Frontside



In APL1088,have some SRAM Block IP #1



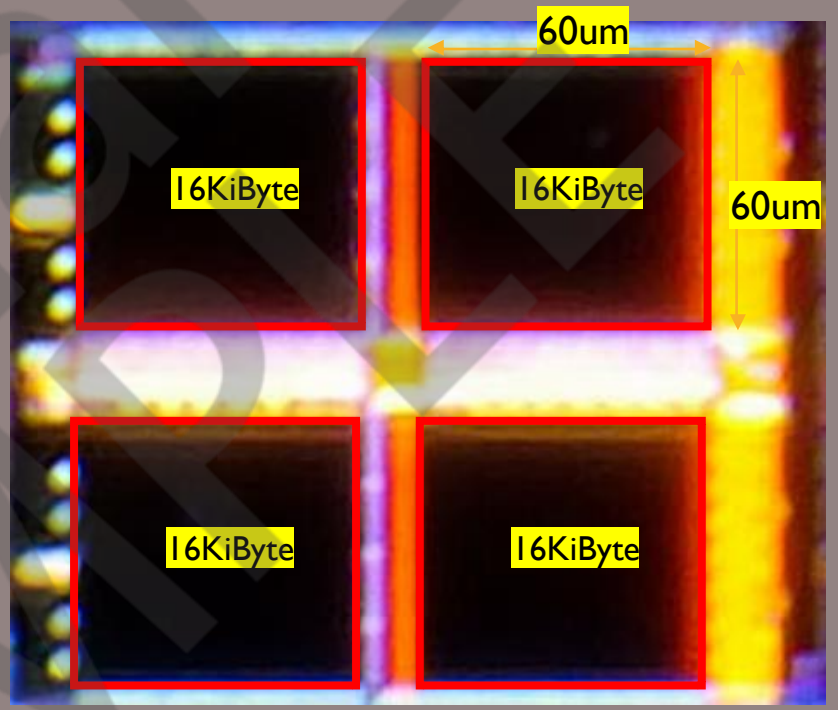
Process identification-APL1088



64KiByte SRAM IP #1

Size: 64KiB

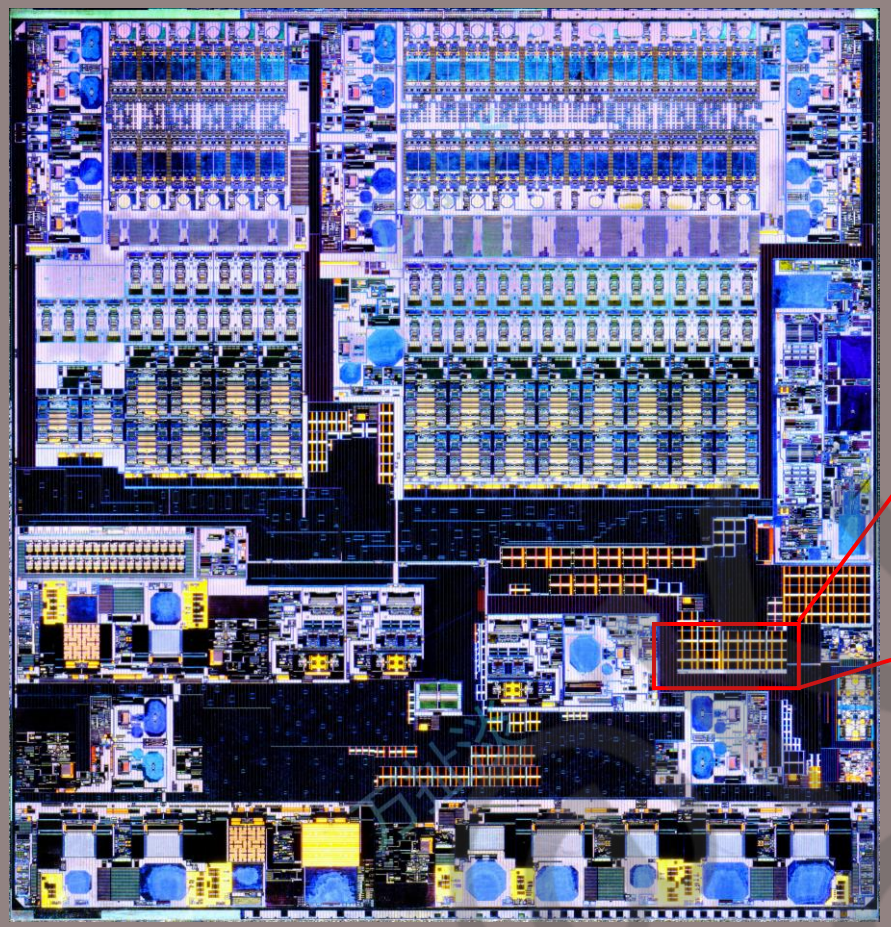
0.0255mm2/64KiB
2,509.80KiB/mm2
19.60Mbit/mm2



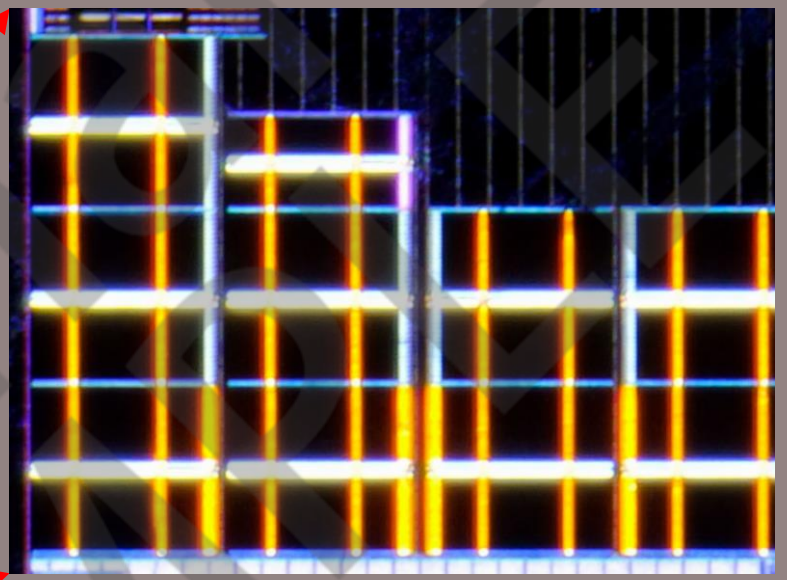
SRAM bit cell by used: 14,400um2
Proportion: 56.47%

SRAM Bit cell Density: 0.027465um2/bit

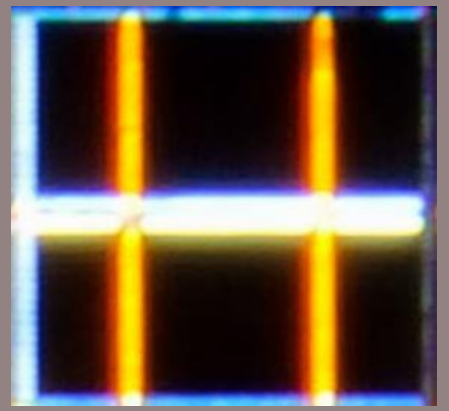
Process identification-APL1088

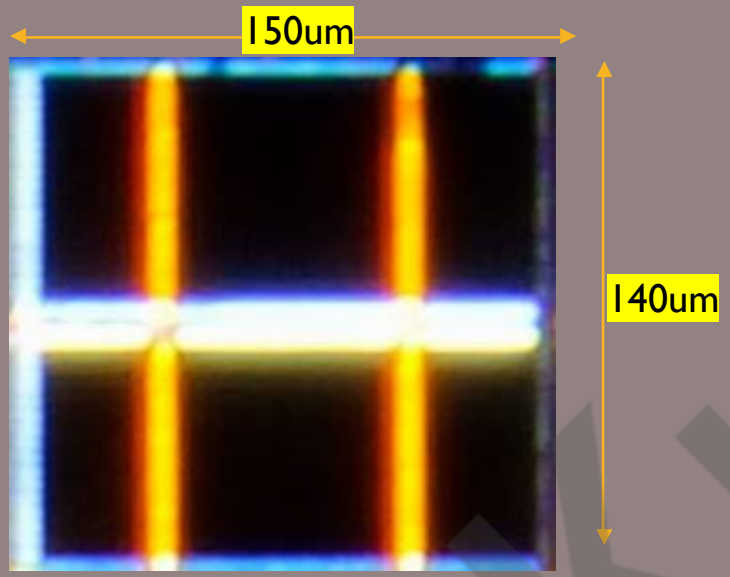


APL1088 Frontside



In APL1088 ,have some SRAM Block IP #2

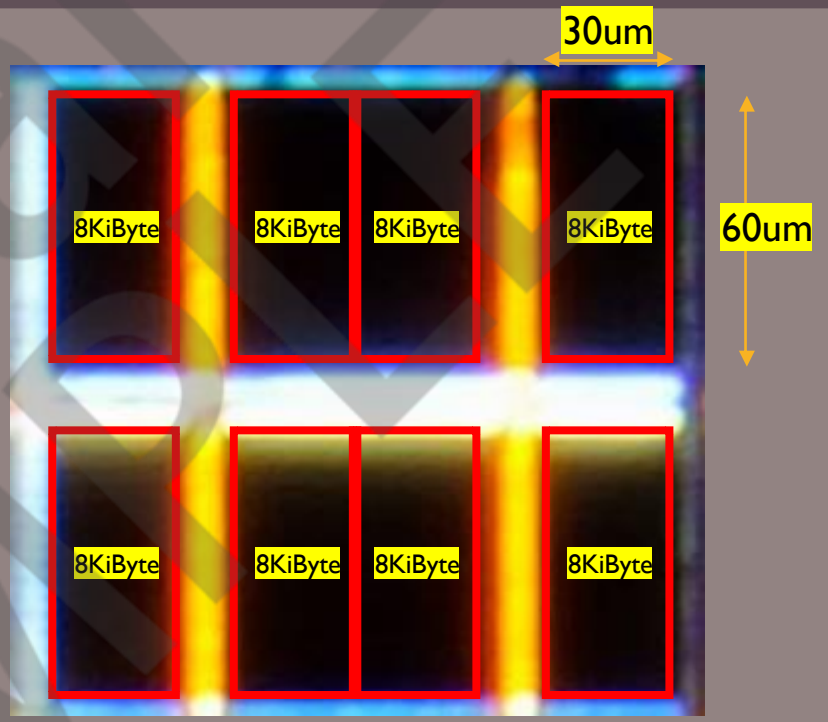




64KiByte SRAM IP #2

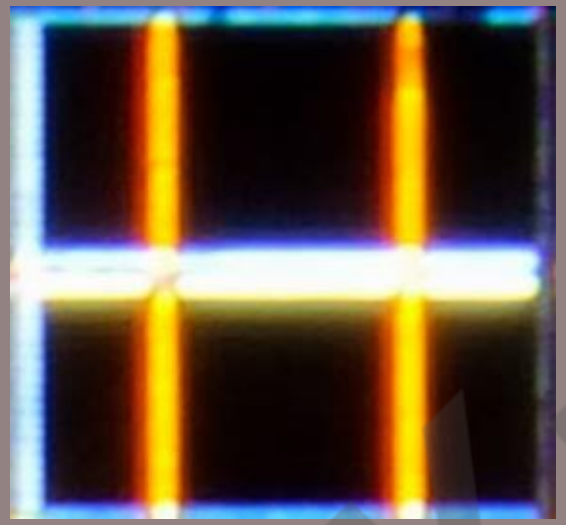
Size: 64KiB

0.021mm2/64KiB
3,047.61KiB/mm2
23.80Mbit/mm2



SRAM bit cell by used: 14,400um2
Proportion: 68.57%

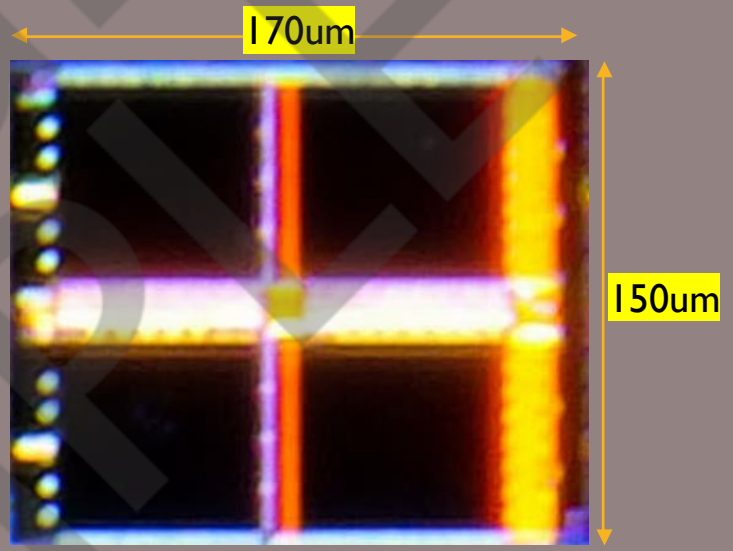
SRAM Bit cell Density: 0.027465um2/bit



APL1088 SRAM IP #2

SRAM Macro density: 23.8Mbit/mm2
SRAM bit cell Density: 0.027465um2/bit

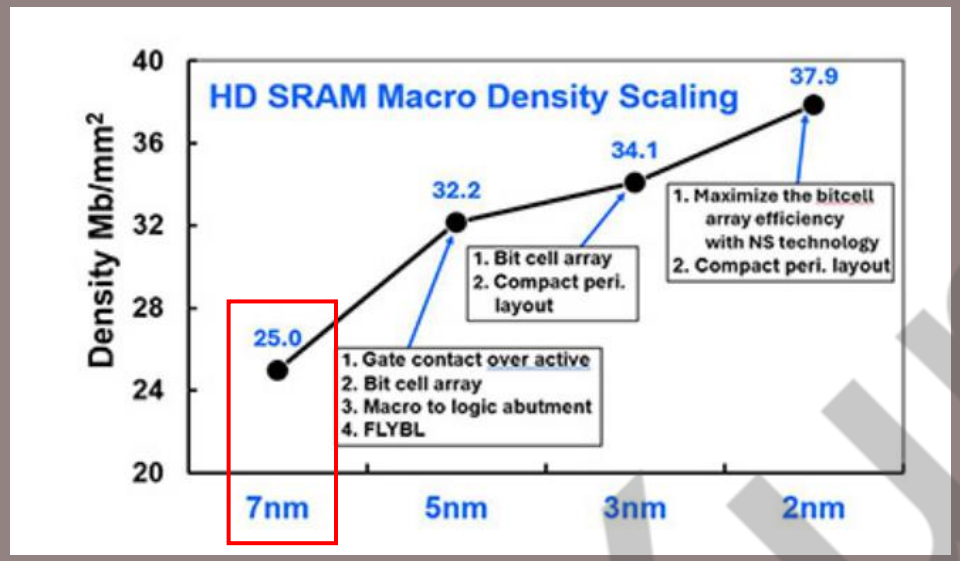
High Density SRAM Block?

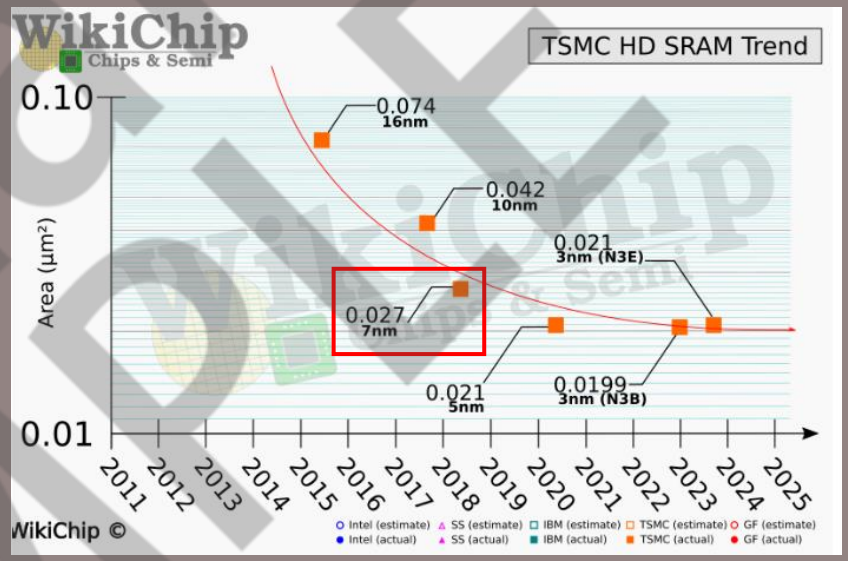


APL1088 SRAM IP #1

SRAM Macro density: 19.6Mbit/mm2
SRAM bit cell Density: 0.027455um2/bit

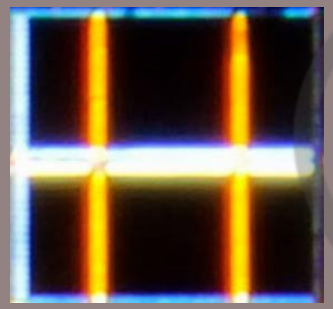
High Perf SRAM Block?





TSMC N7 SRAM Macro density: 25.0Mbit/mm2

TSMC N7 SRAM bit cell density: 0.027um2/bit



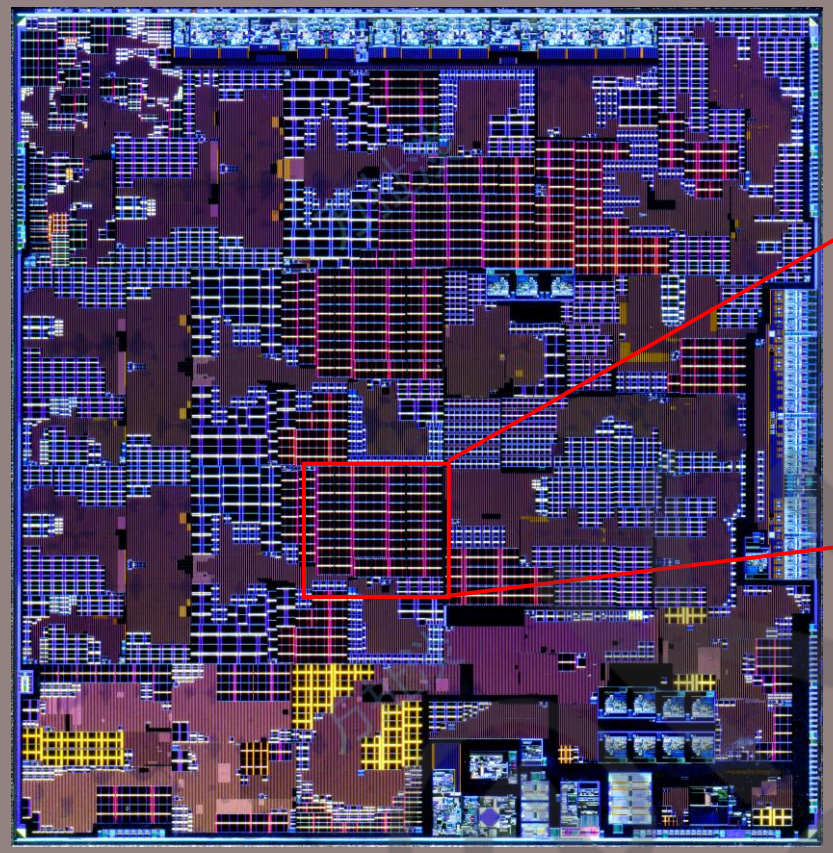
APL1088 SRAM IP #2

SRAM Macro density: 23.8Mbit/mm2

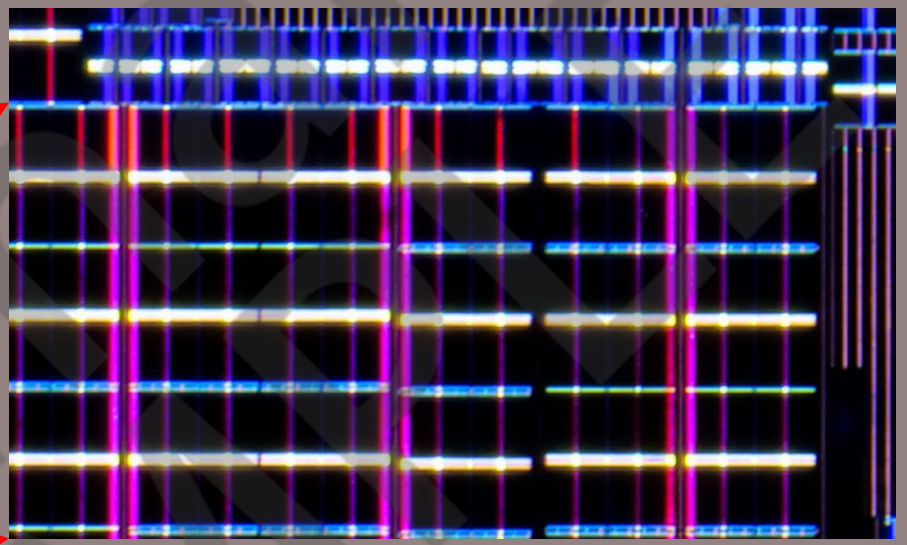
SRAM bit cell density: 0.027465um2/bit

APPLE APL1088
Used TSMC N7 Family

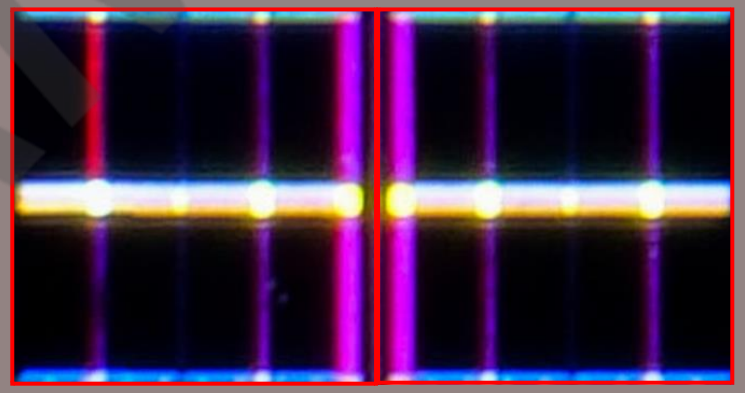
Process identification-APL1114

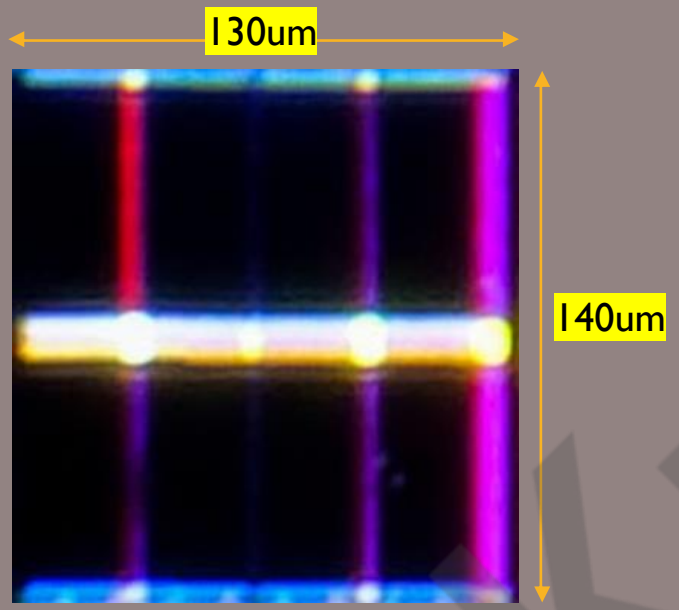


APL1114 Frontside



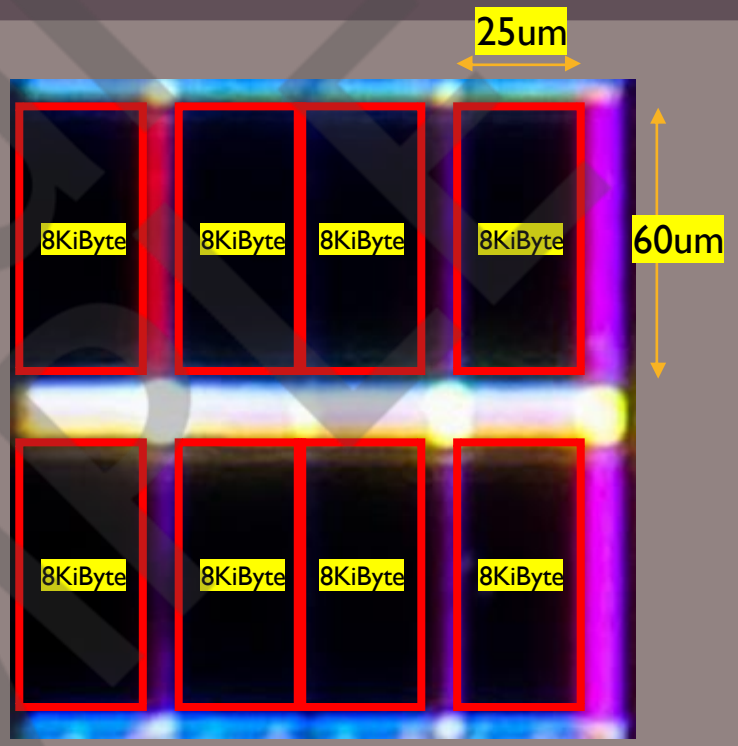
In APL1114,have some SRAM Block IP #3





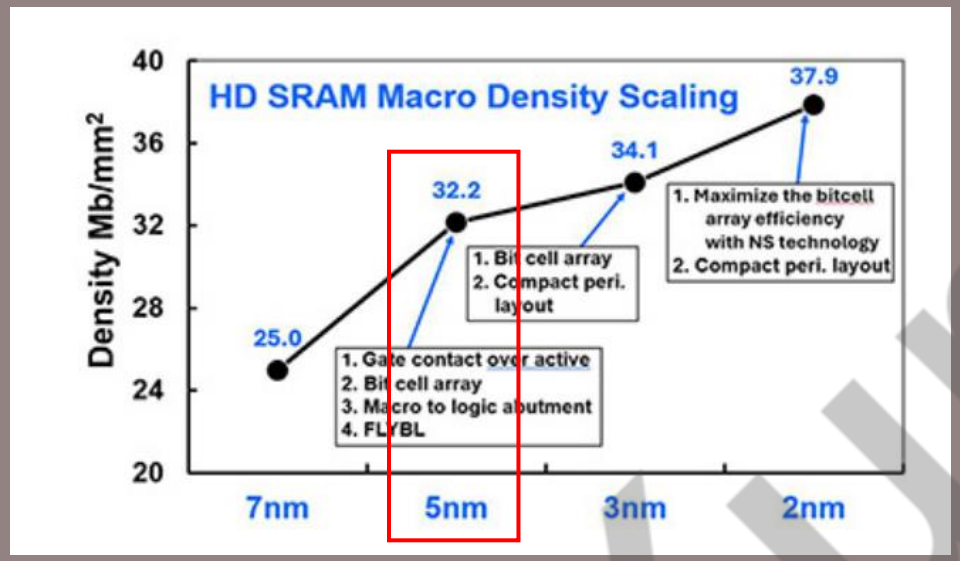
64KiByte SRAM IP #3
Size: 64KiB

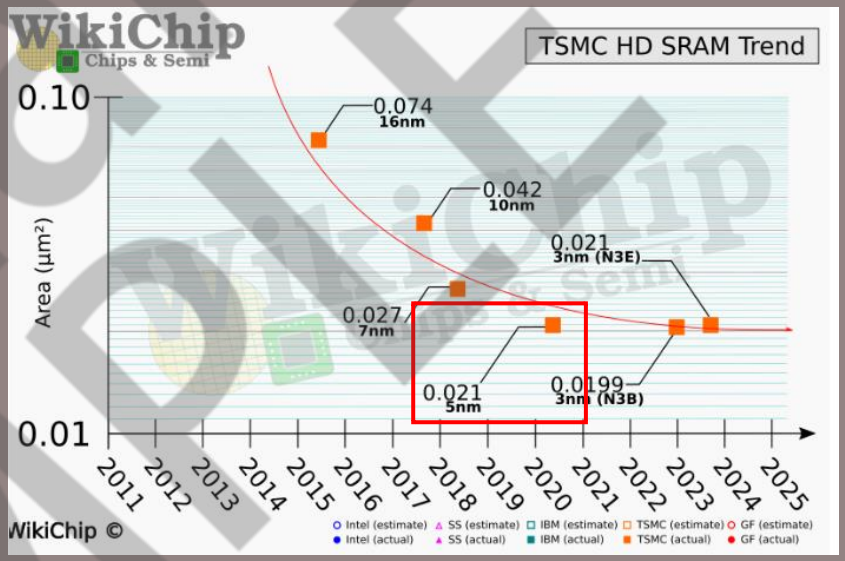
0.0182mm2/64KiB
3,516.48KiB/mm2
27.47Mbit/mm2



SRAM bit cell by used: 12,000um2
Proportion: 65.93%

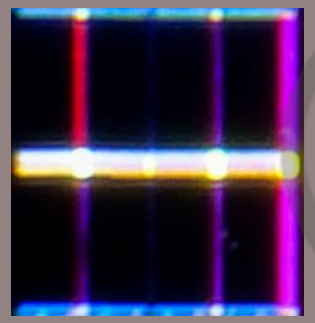
SRAM Bit cell Density: 0.02403um2/bit





TSMC N5 SRAM Macro density: 32.2Mbit/mm2

TSMC N5 SRAM bit cell density: 0.021um2/bit



APL1114 SRAM IP #3

SRAM Macro density: 27.47Mbit/mm2

SRAM bit cell density: 0.02403um2/bit

Bigger than N7 HD
Smaller than N5 HD

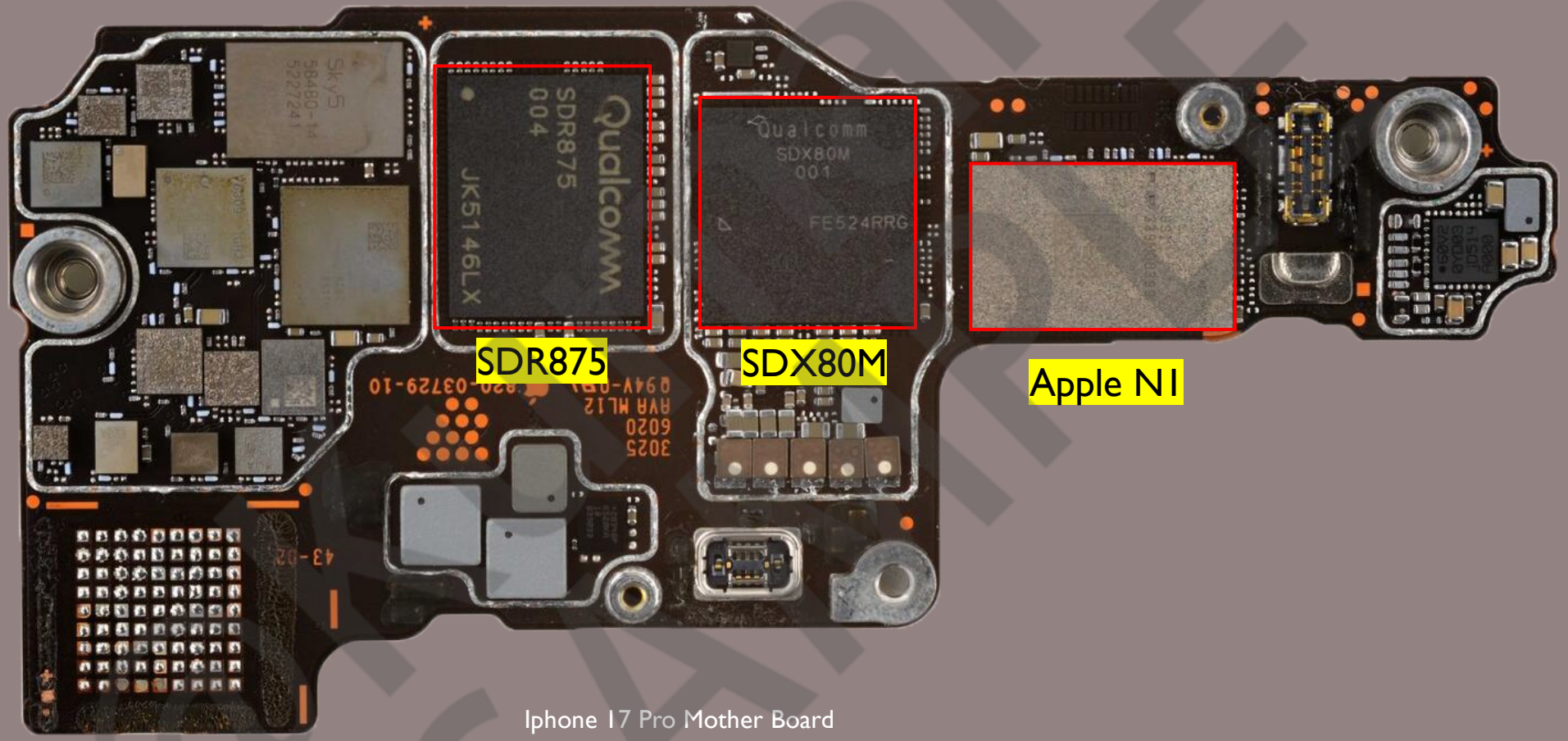
APPLE APL1114
Used TSMC N5 Family

Bigger than N7 HD
Smaller than N5 HD

N1 Analyze

On chip analyze

N1 Analyze-Package

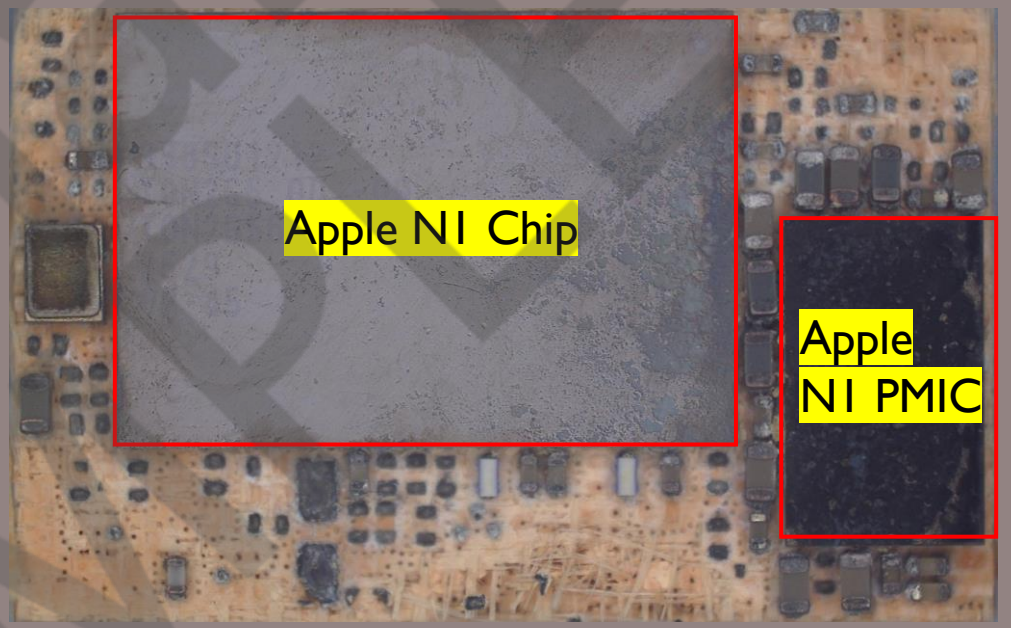


Iphone 17 Pro Mother Board

N1 Analyze-Package

Apple N1 Package

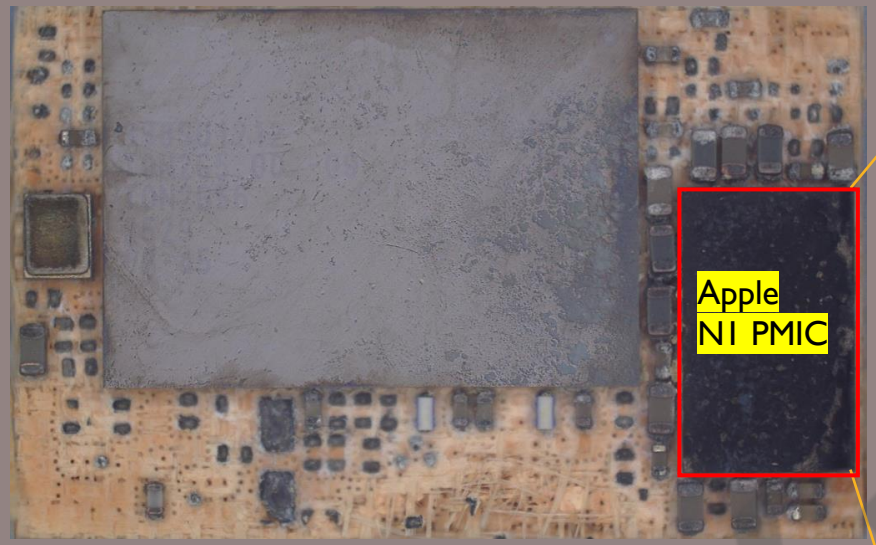
Decaped



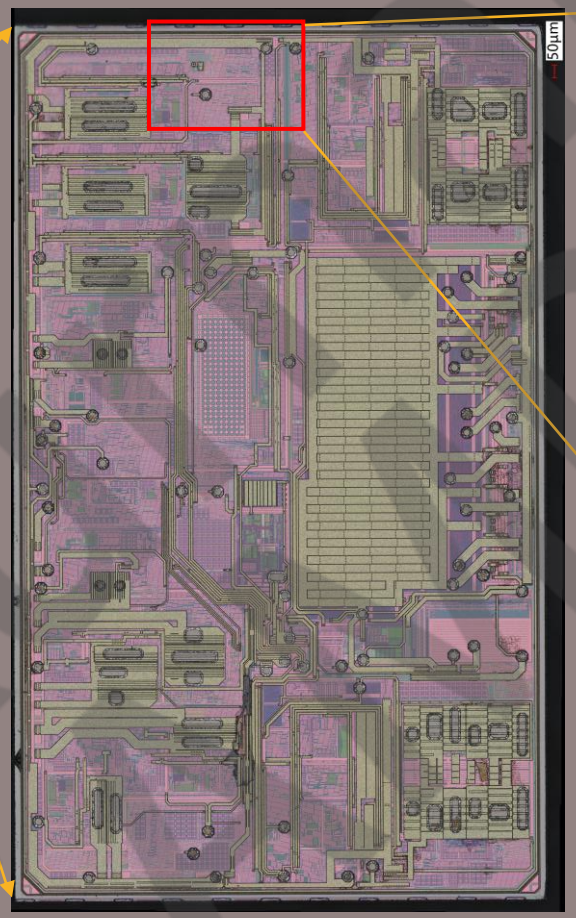
Apple N1 Package

Used SiP (System in Package)

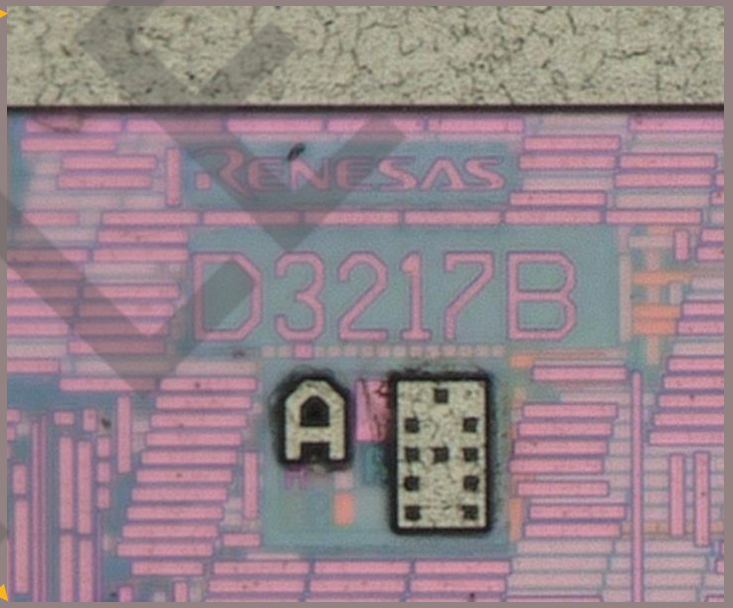
N1 Analyze-Package-PMIC



Apple N1 Package



Apple N1 PMIC



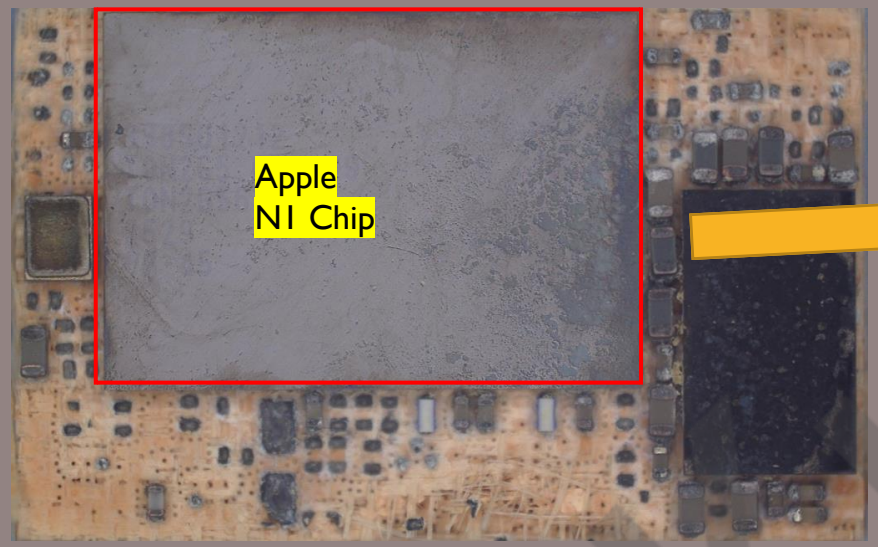
Apple N1 PMIC Diemark

Die size: 6.73mm2 (2.02mm x 3.33mm)

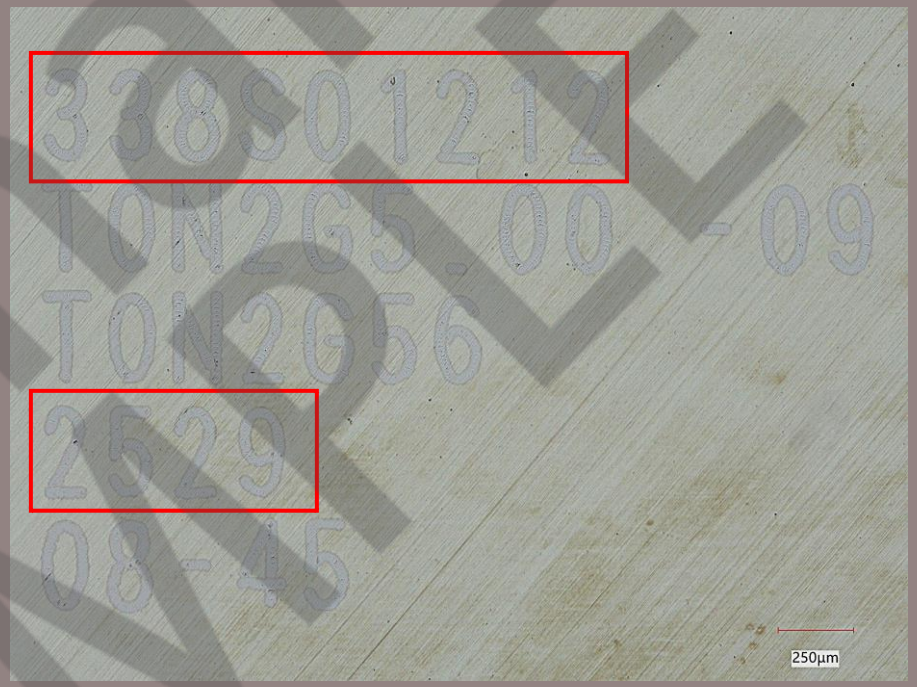
Chip made by RENESAS

Die Mark: Renesas D3217B

N1 Analyze-Package-N1 Chip



Apple N1 Package



Apple N1 Top mark

Product name: 338S01212

Made/Package data: Year 2025 Week 29

N1 Analyze-Package-N1 Chip

Apple N1 Dieshot

Die size: 27.8mm2

with out seal ring: 6.20mm x 4.33mm

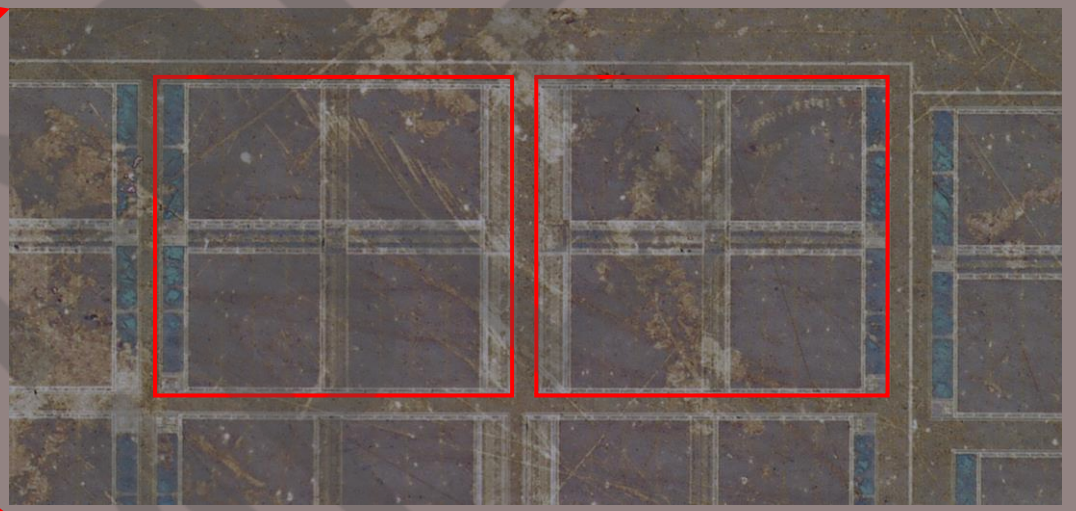
Apple N1 Diemark

Die Mark : TM SX10

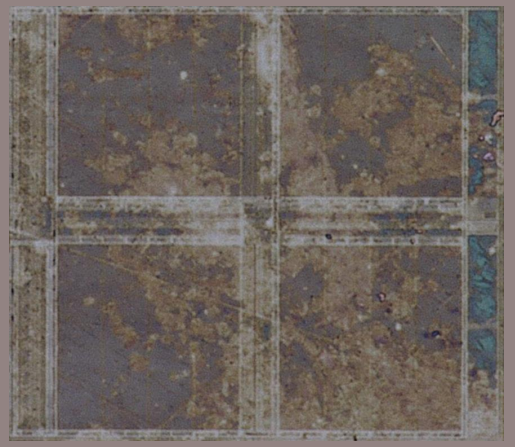
TSMC Tap Out Mark
Tap Out in year 2024

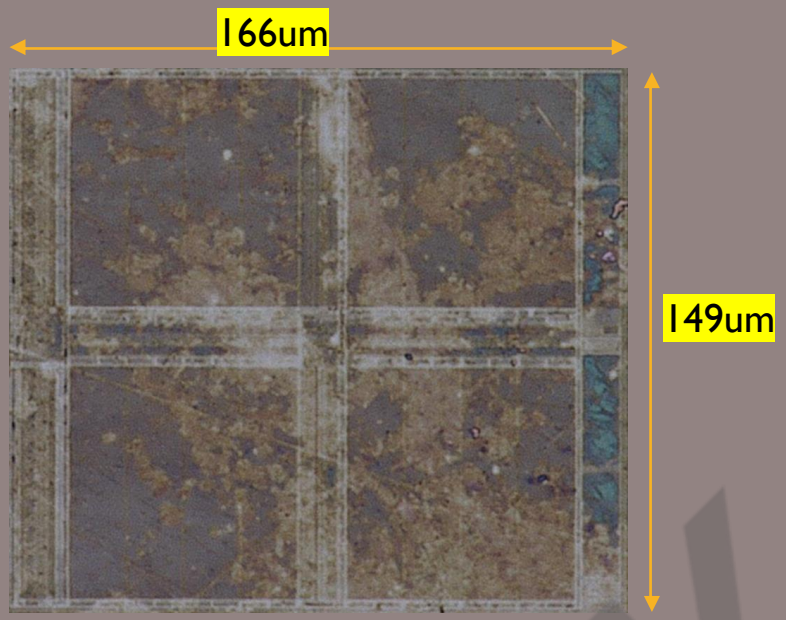
Process identification-N1

Apple N1 Dieshot



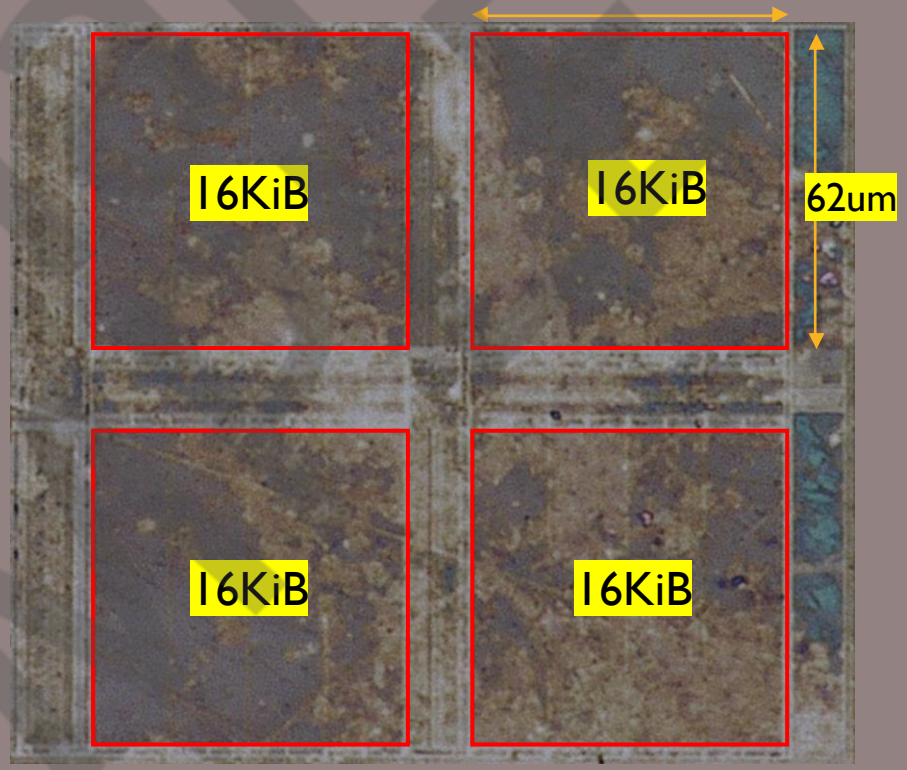
In Apple N1 ,have some SRAM Block IP #4





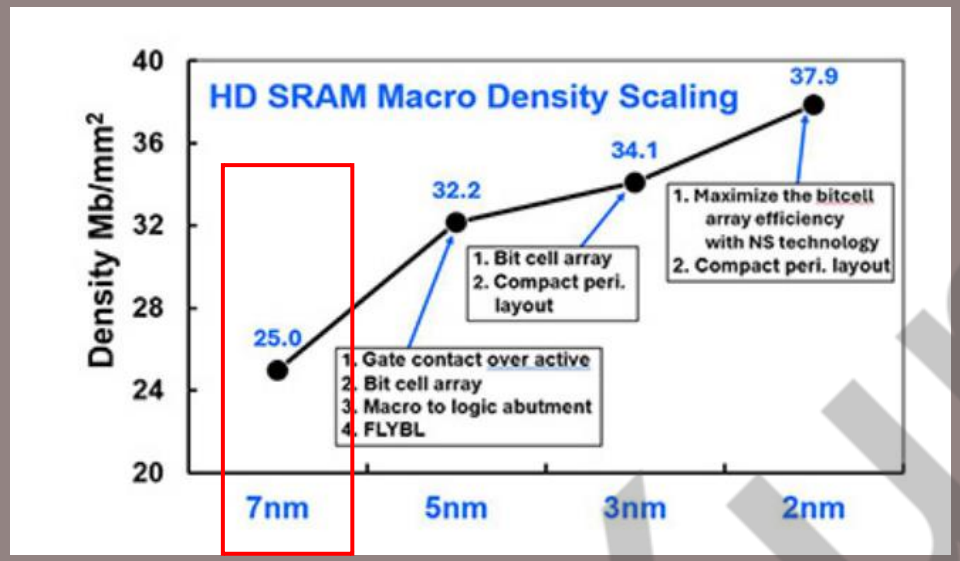
64KiByte SRAM IP #4
Size: 64KiB

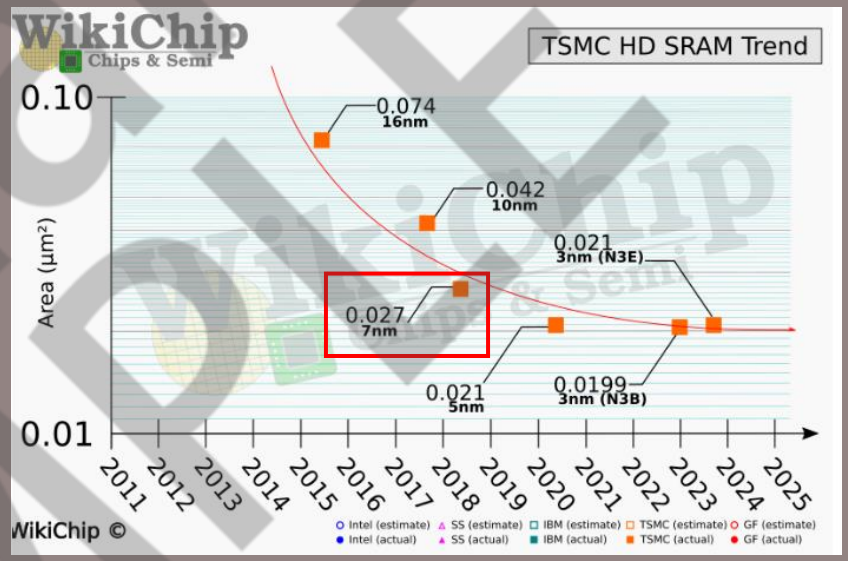
0.024734mm2/64KiB
2,587.53KiB/mm2
20.215Mbit/mm2



SRAM bit cell by used: 15,376um2
Proportion: 62.165%

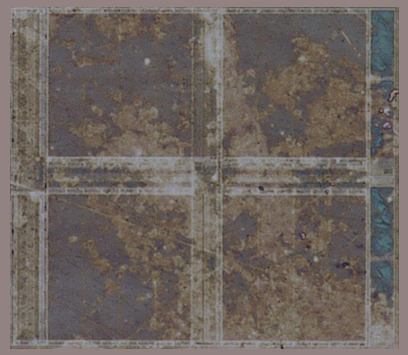
SRAM Bit cell Density: 0.029327um2/bit





TSMC N7 SRAM Macro density: 25.0Mbit/mm2

TSMC N7 SRAM bit cell density: 0.027um2/bit



Apple N1 SRAM IP #4

SRAM Macro density: 20.215Mbit/mm2

SRAM bit cell density: 0.029327um2/bit

Bigger than N7 HD

Bigger than N7 HD

APPLE N1
Used TSMC N7 HP