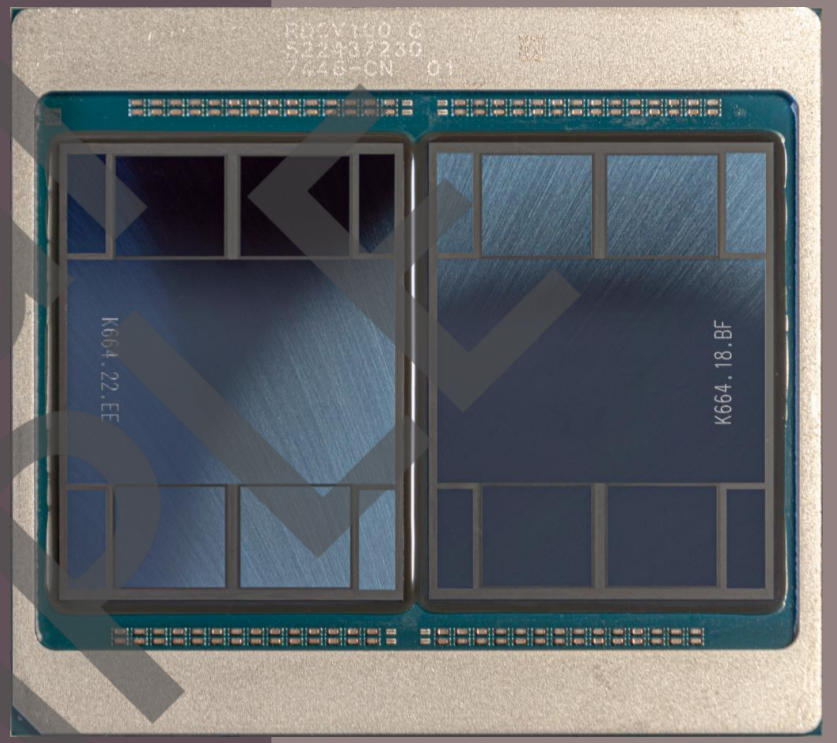
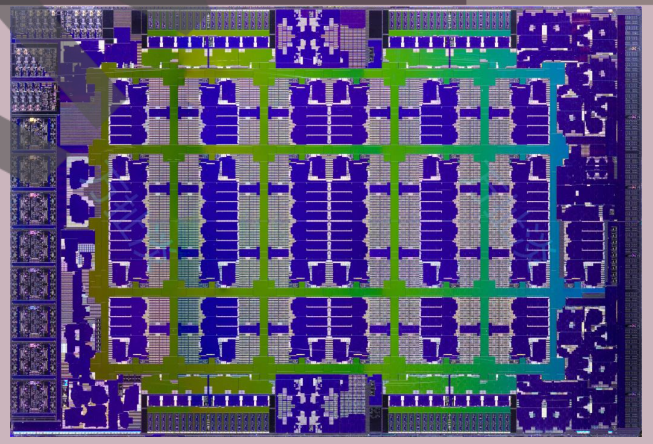
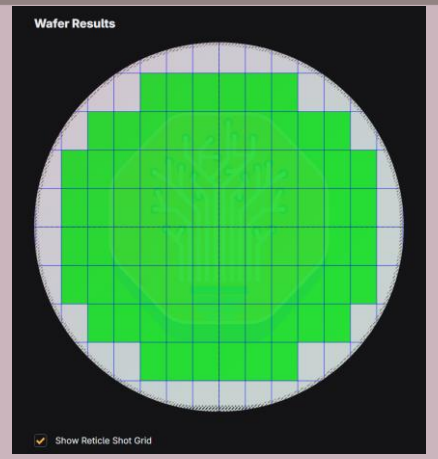
Huawei Ascend 910C

On chip analyze

V1







@Kurnal

Verison of this Report

Version	Date	Updates	Anthor
V0	2025/07/16 21:25	Working	Kurnal
V1	2025/07/21 19:48	Finish	Kurnal
B站工坊			

About Authors

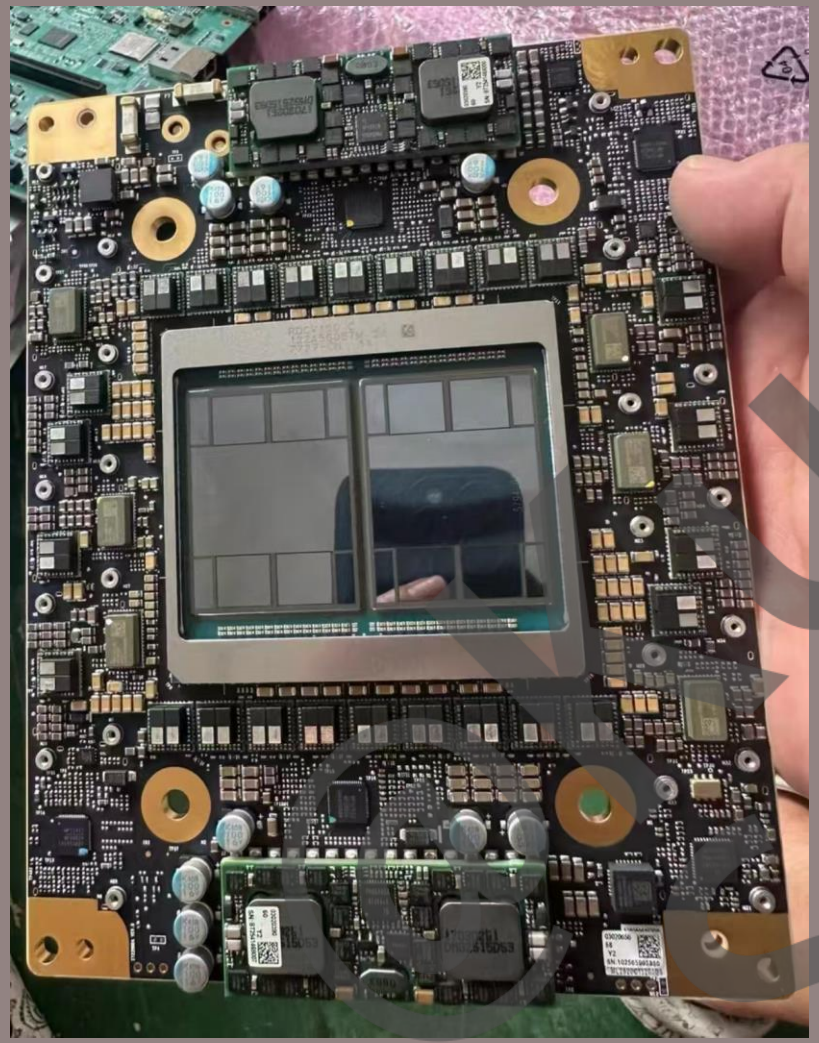
This Report is made From @Kurnal

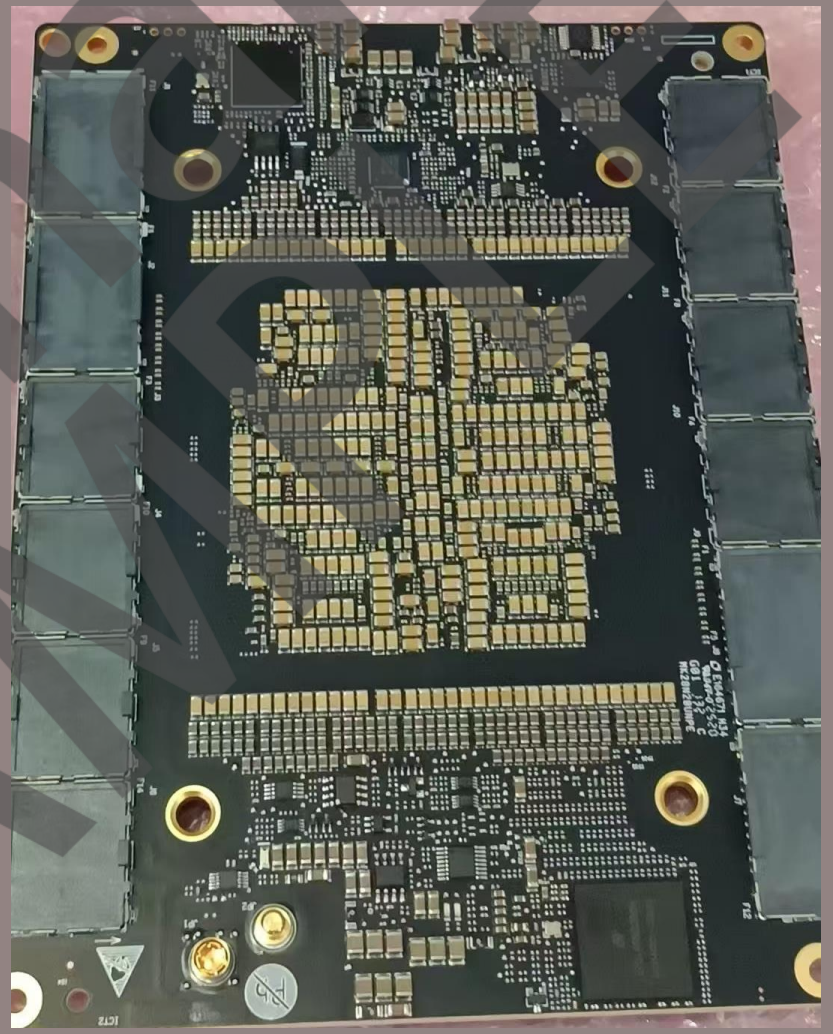
BiliBili: @Kurnal
X: @Kurnalsalts
WeChat: KurnalWeChat

Package analyze

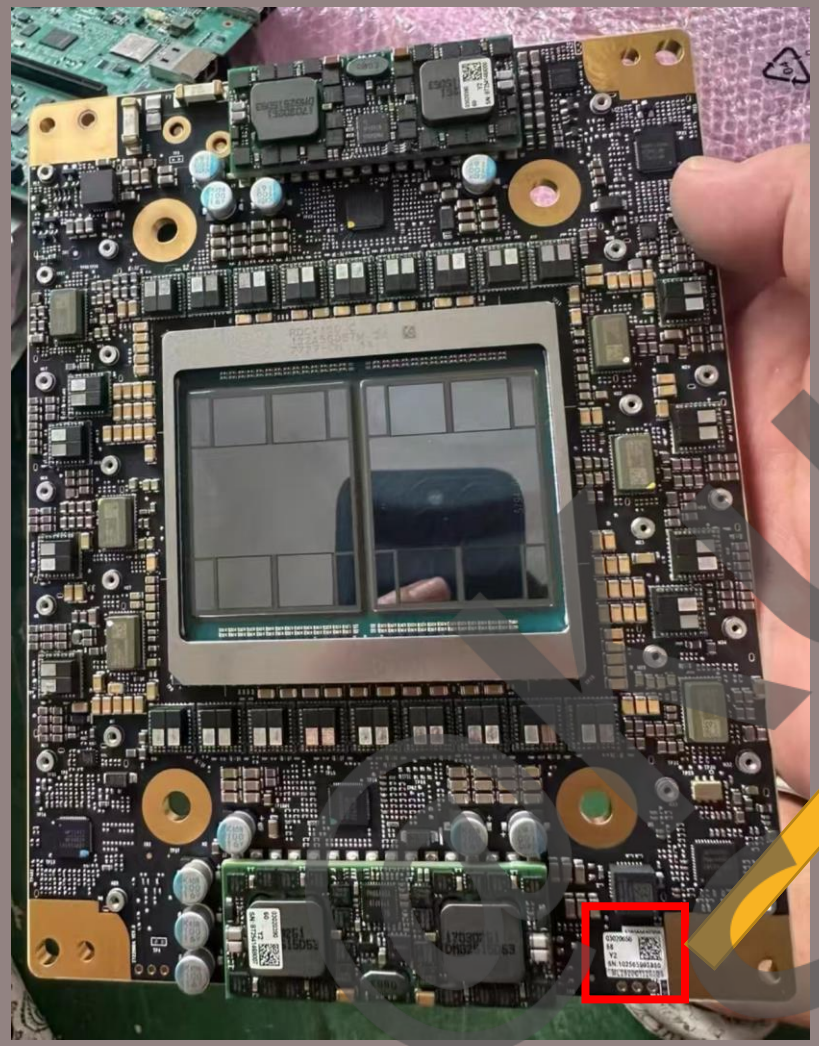
Ascend 910C

Ascend910C Package



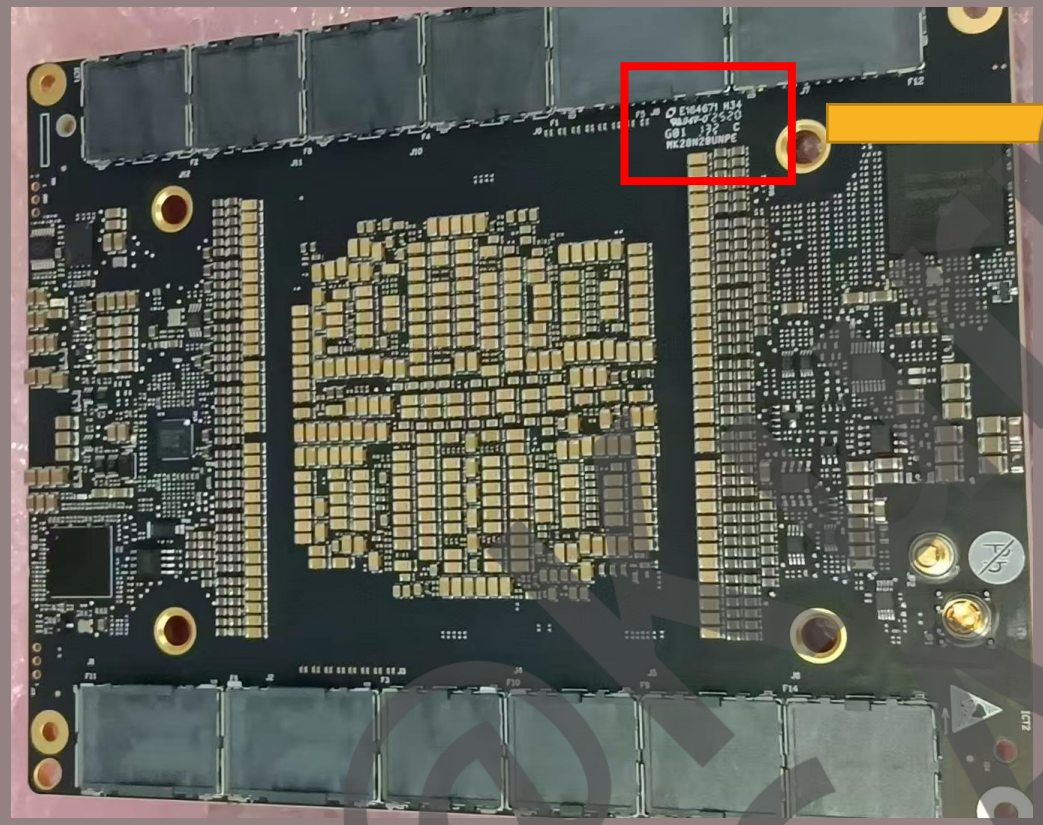


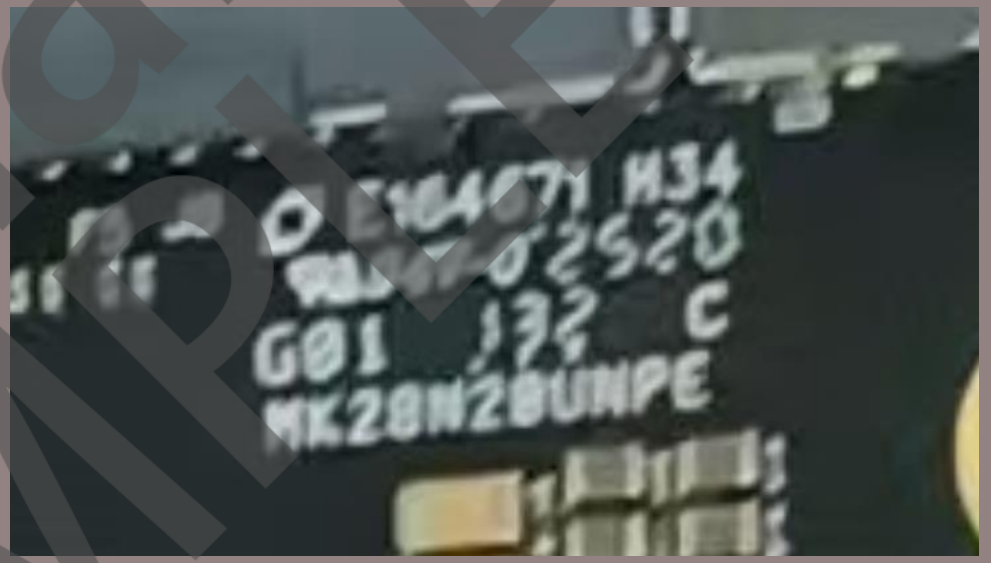
Ascend910C Package



Mother Board Rev：V2

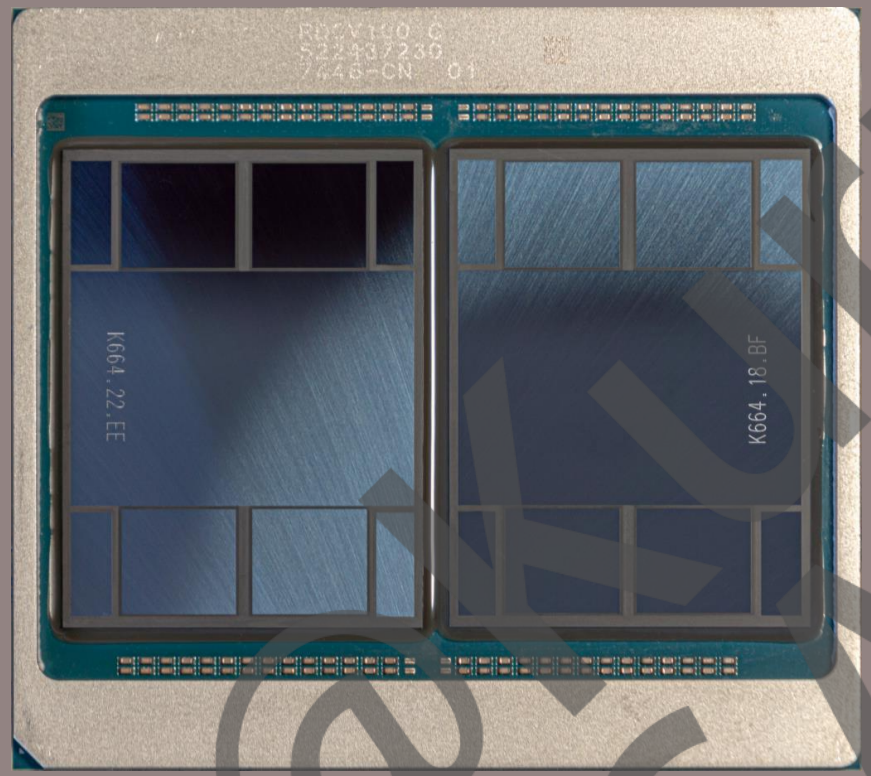
Ascend910C Package



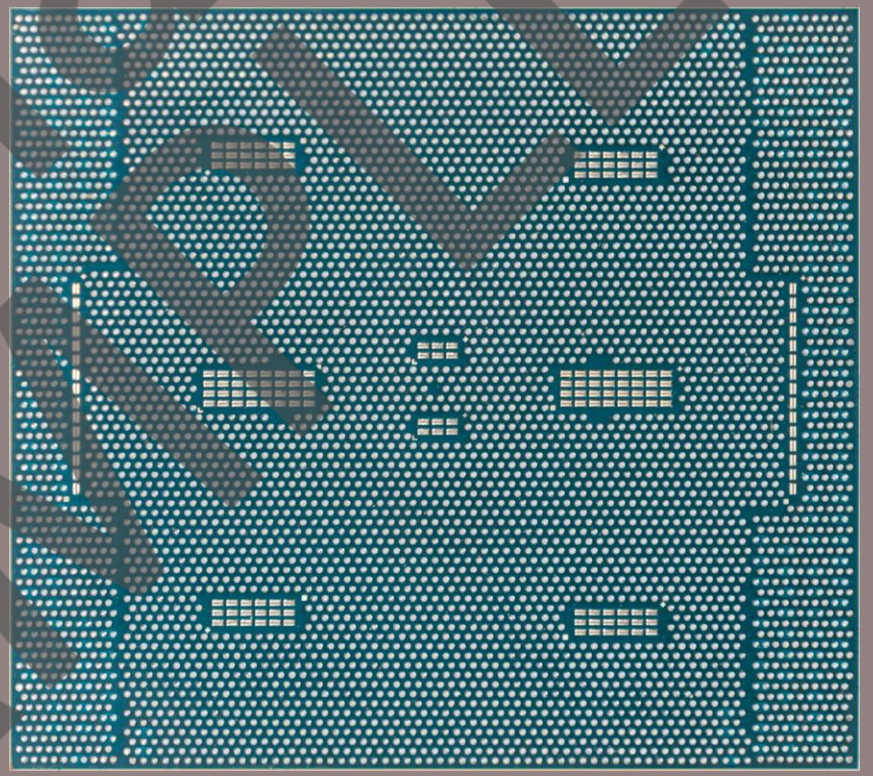


Mother Board made in Year 2025 Week 20

Ascend910C Package

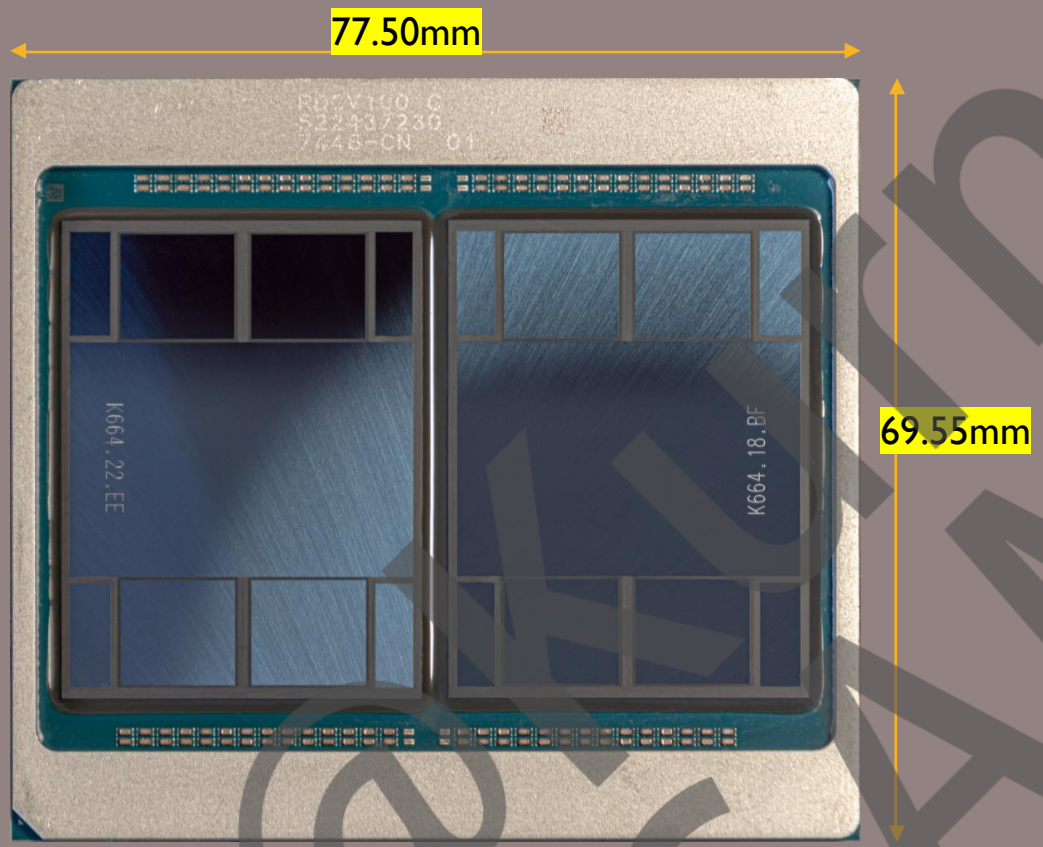


Ascend 910C Front view



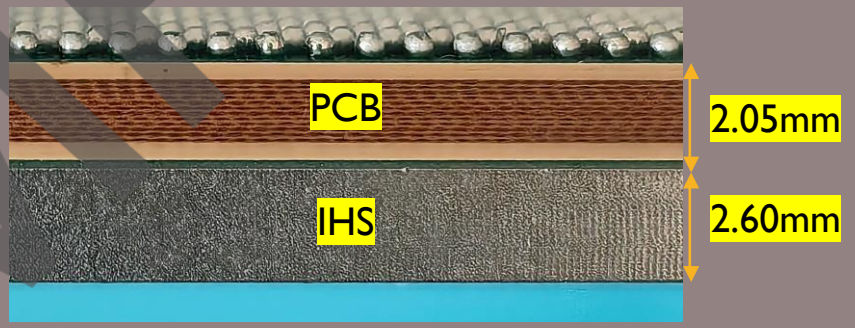
Ascend 910C Bottom view

Ascend910C Package



Ascend 910C Front view

Package:	BGA
Dimensions:	69.55mm x 77.50mm
Ball Pitch:	1.00mm
Ball Diameter:	0.60mm

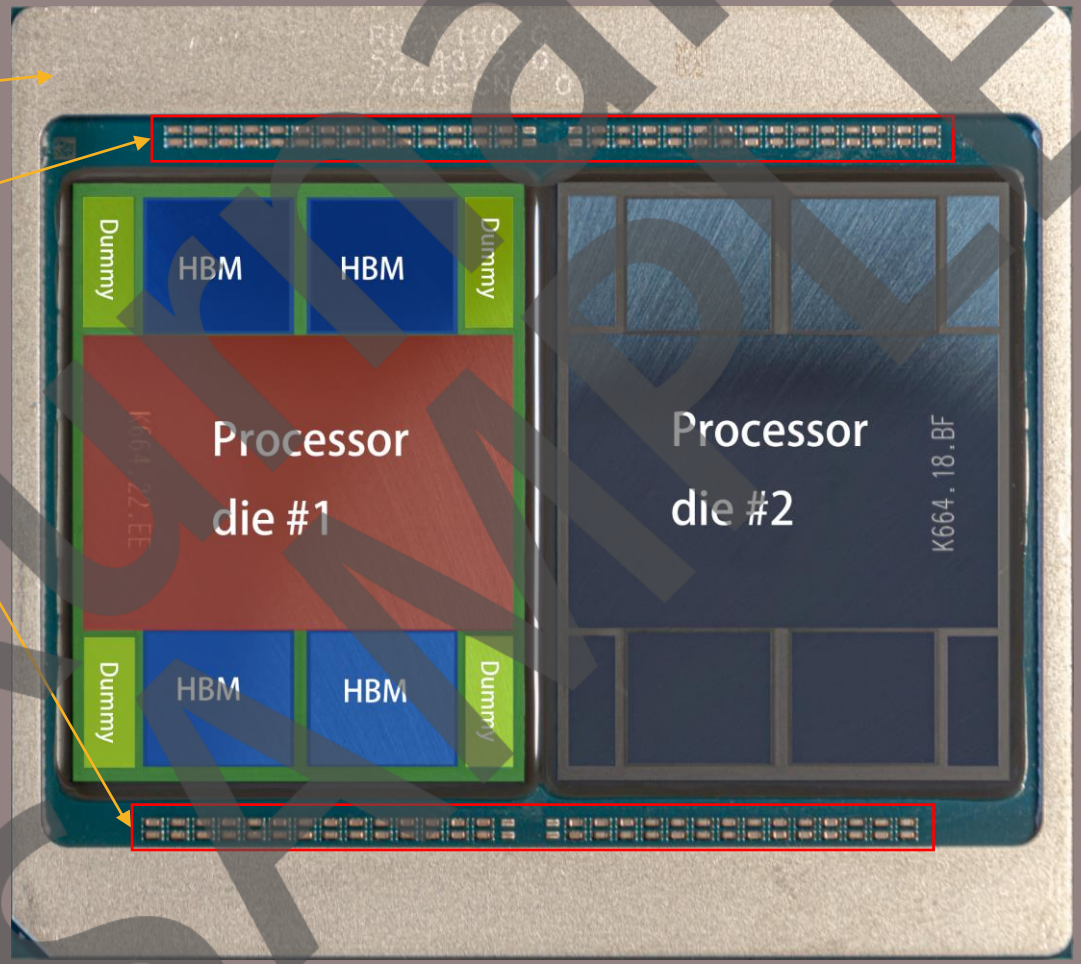


Ascend 910C Sectional view

Ascend910C Package

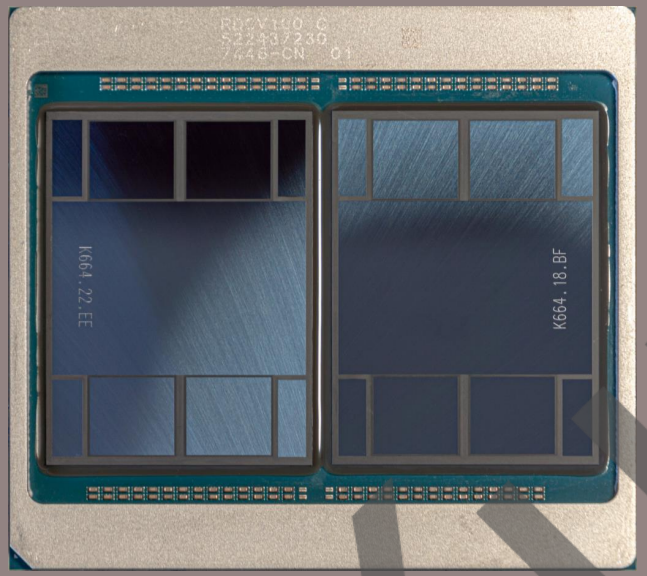
Stiffener Ring

Passive Capacitors

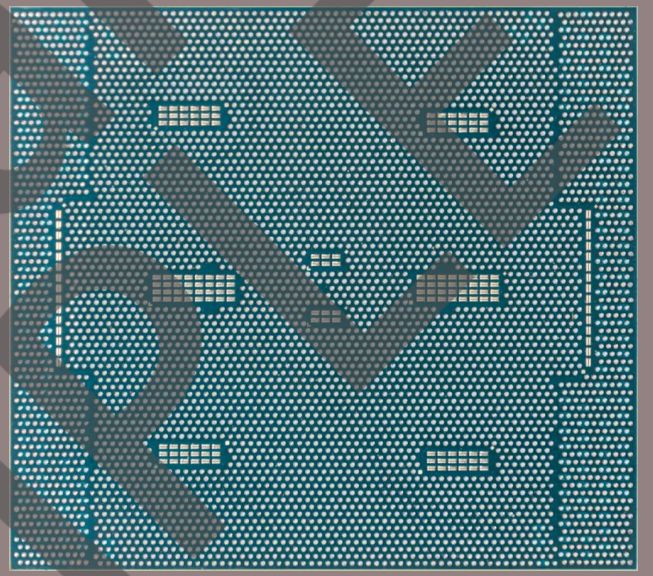


Red: Processor Die
Blue: HBM Dram Stack
Yellow: Dummy Die
Green: Molding

Ascend910C Package



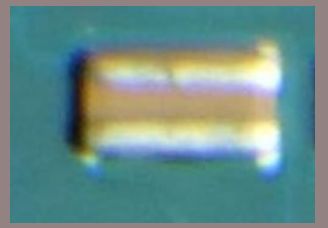
Ascend 910C Front view



Ascend 910C Bottom view

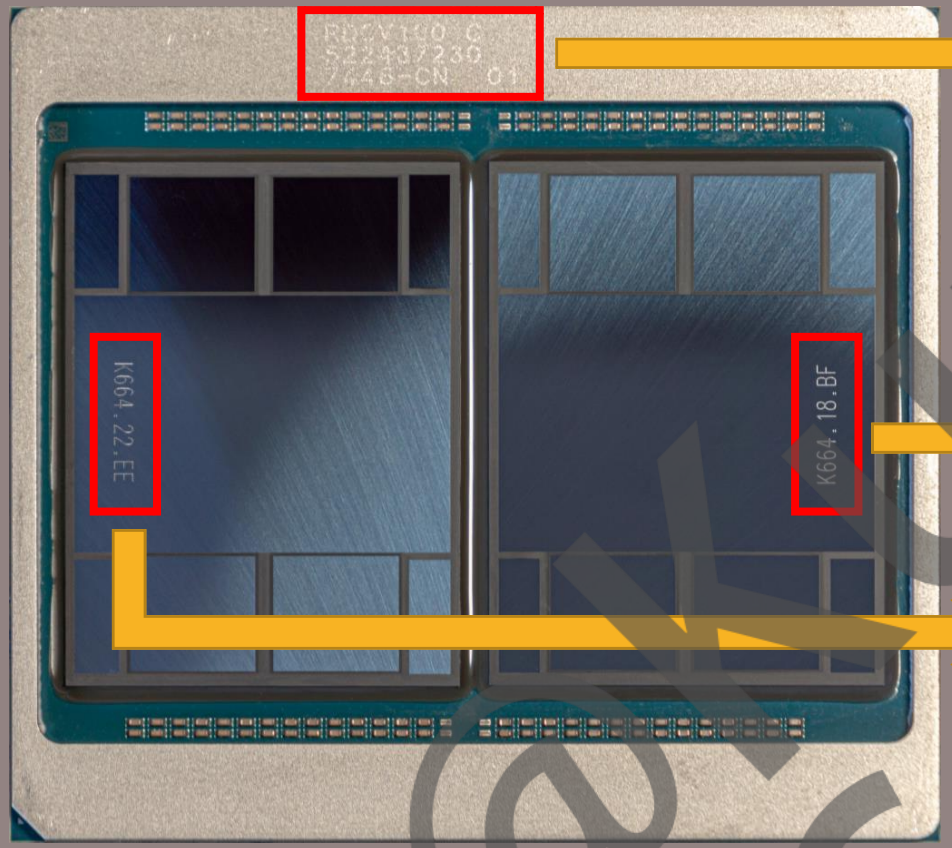
0204 Capacitor x 8
(capacitors on the Front side)

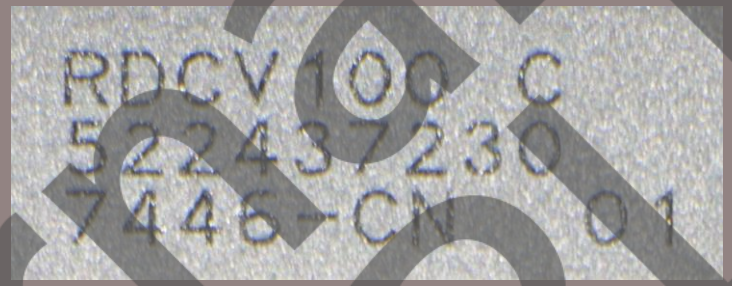
0402 Capacitor x 112
(capacitors on the Front side)



0204 Capacitor x 178
(capacitors on the back side)

Ascend910C Package-Diemark

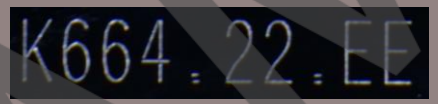




Package Mark
RDCV100 C
522437230
7446-CN 01

Ascend 910 C ?

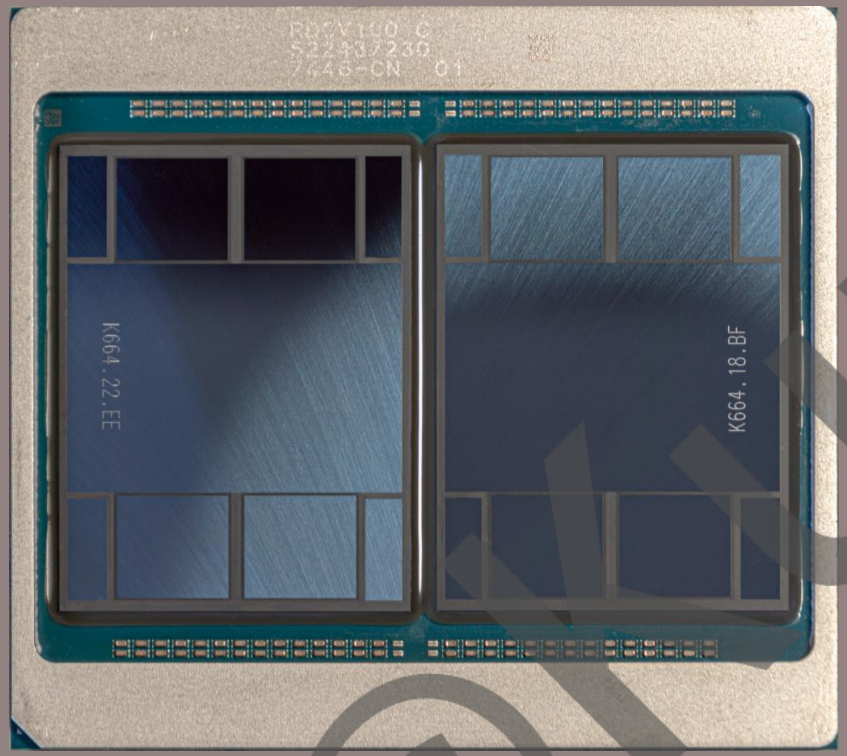
Die Mark
K664 18 BF



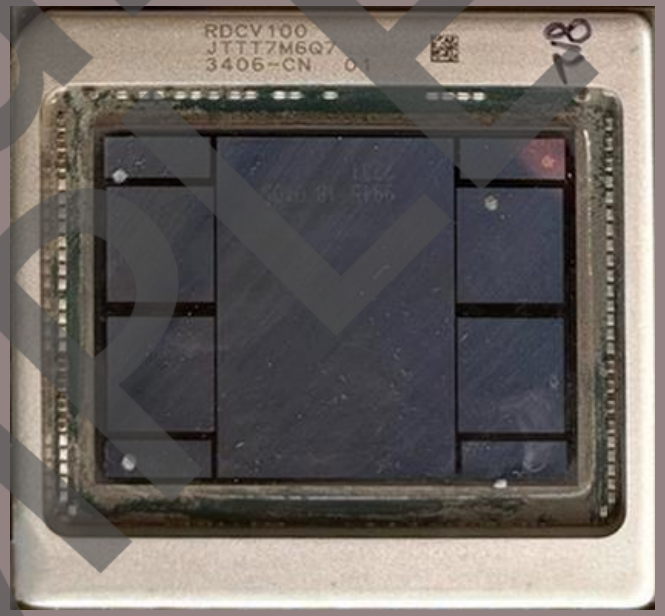
Die Mark
K664 22 EE

Package in Year2024 Week 37?

Ascend910C Package-Diemark



Package Mark
RDCV100 C
522437230
7446-CN 01

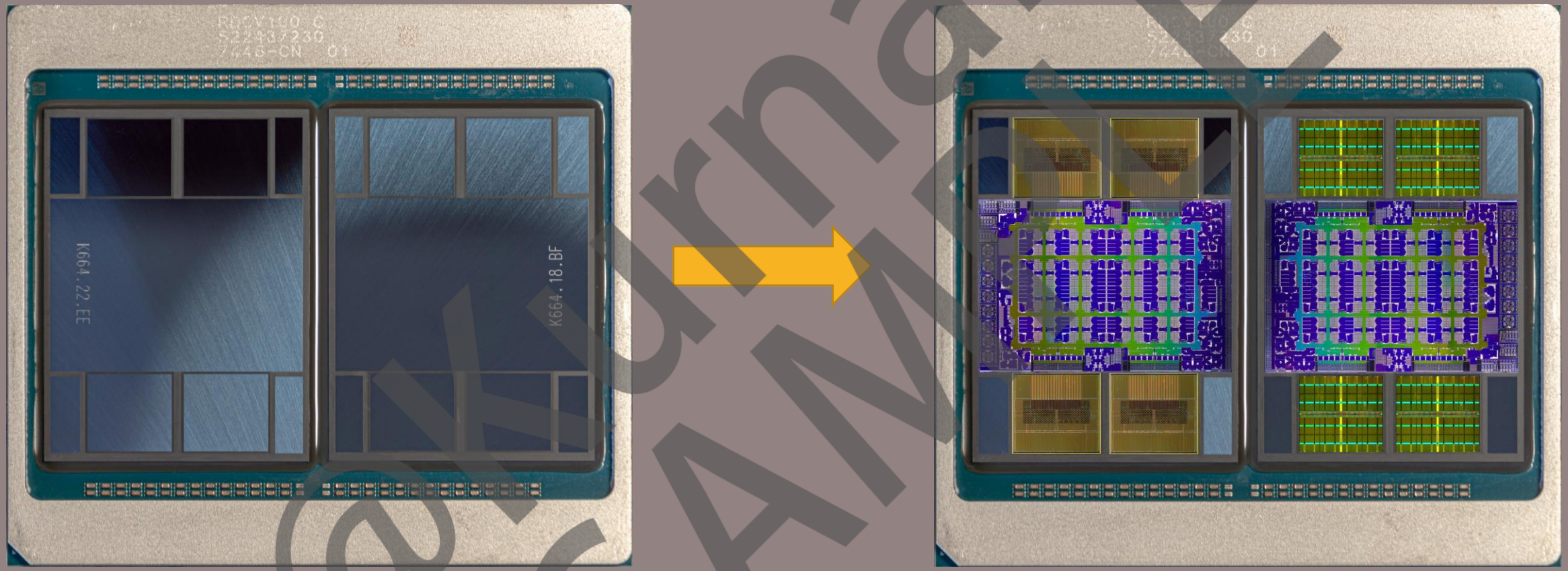


Package Mark
RDCV100
JTTT7M6Q7
3406-CN 01

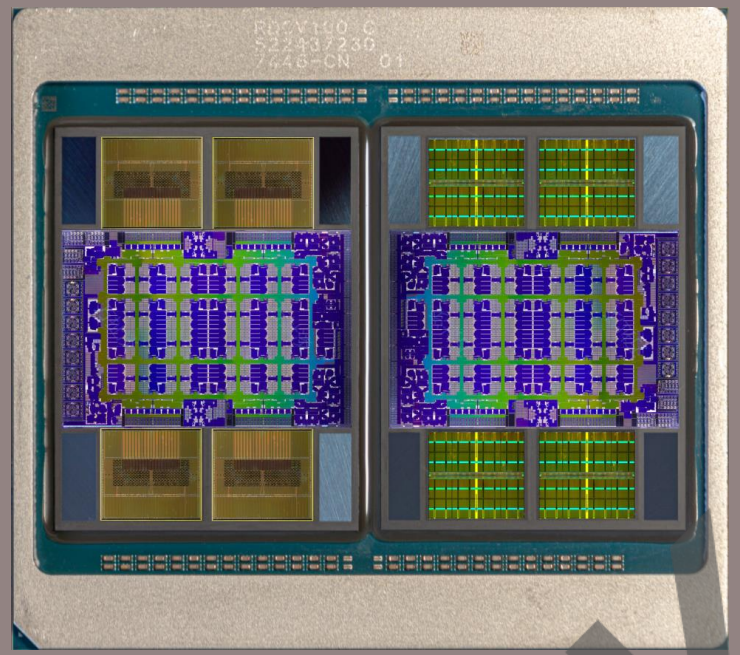
Decaped

Chip analyze

Ascend910C Decaped



Ascend910C Decaped

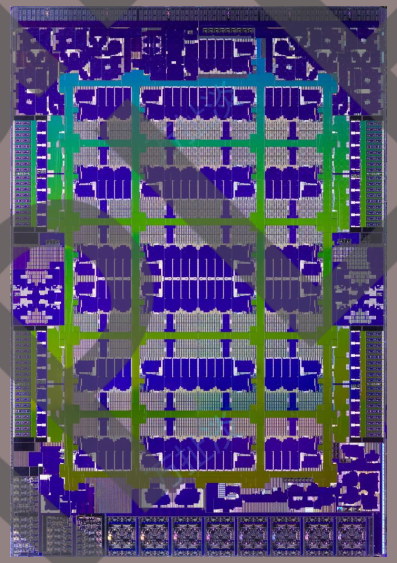


Package size 69.55mm x 77.50mm

No image

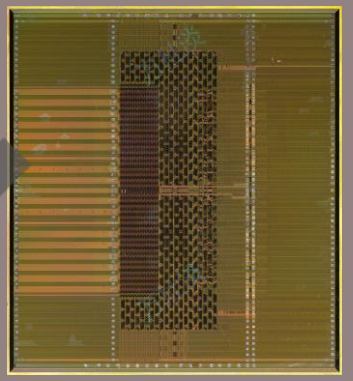
Si interposer

Ascend 910C Si interposer
Package size: 44 x 33



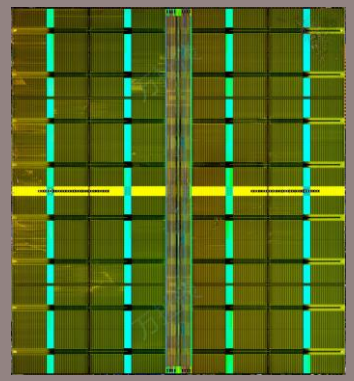
Processor die

Processor Die
Package size: 21.32x31.22



HBM Logic Die

HBM Logic Die x4
Package size: 9.59x10.52

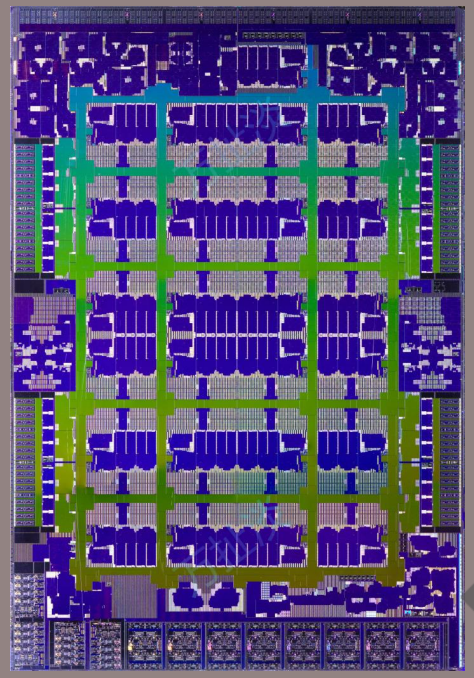


HBM Memory Die

HBM Memory Die 4x8
Package size: 9.59x10.52

Package opening reveals
8HBM Dram Stack(8 Logic dies+64 DRAM Dies) (1:8)
2 Processor Die
2 Si Interposer
8 Dummy Die

Process Die-Die Per Wafer

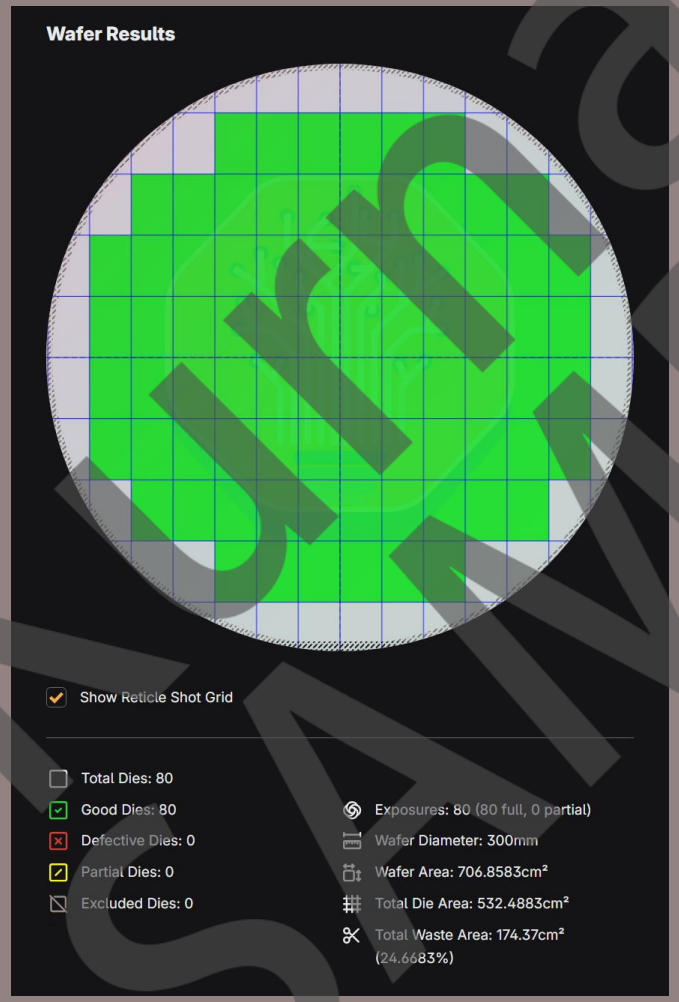


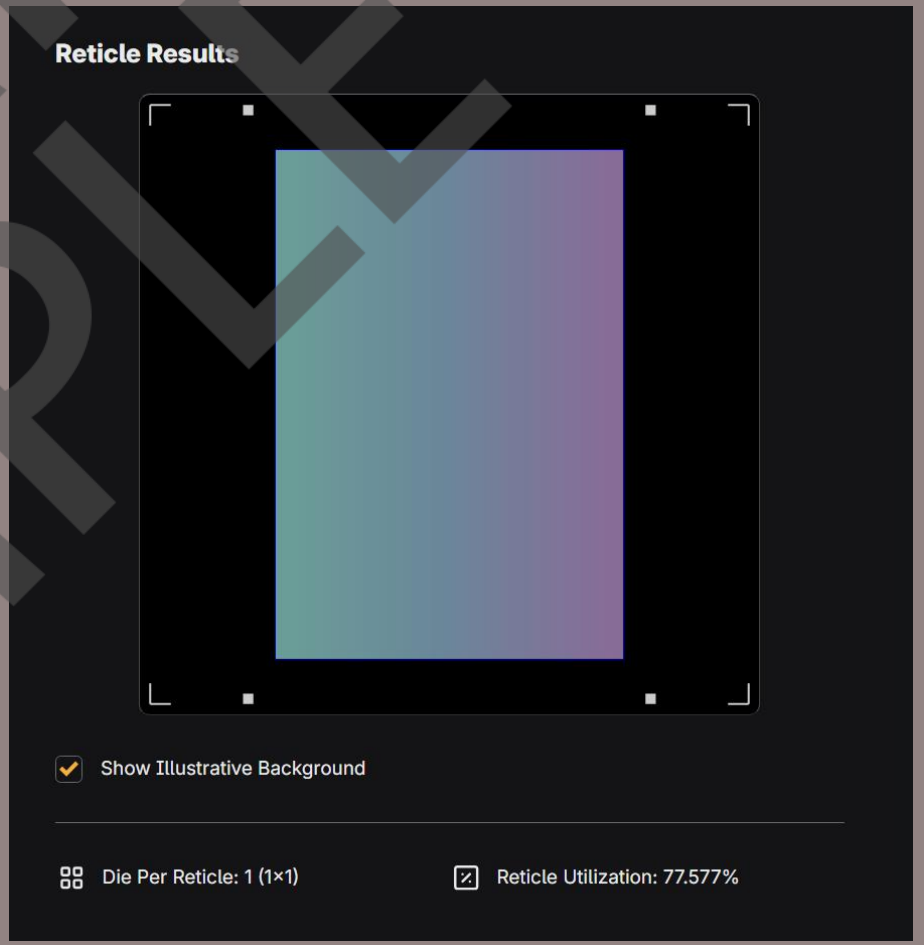
Processor Die

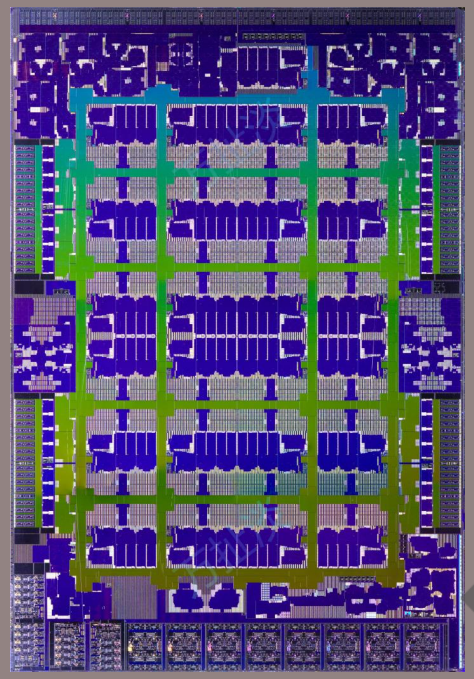
Package size: 21.32x31.22

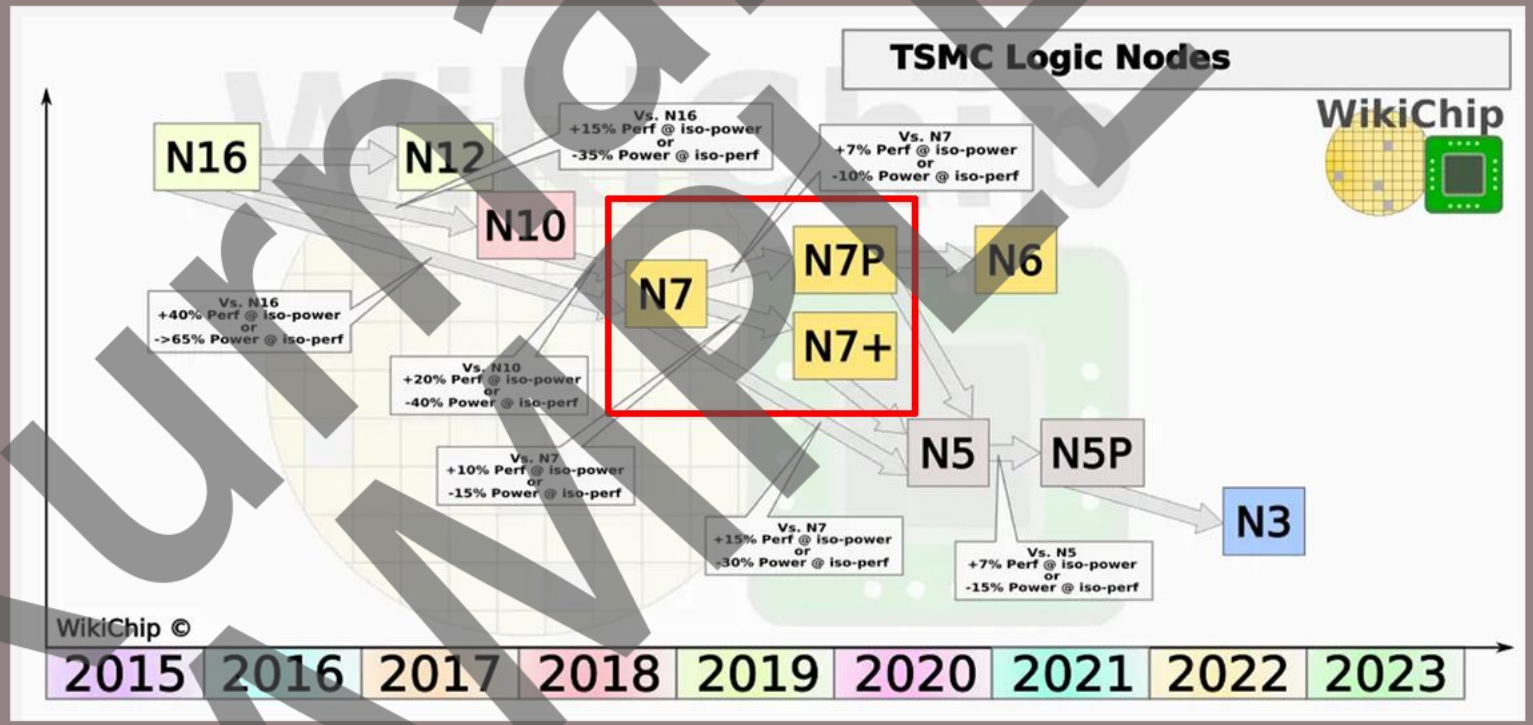
Die Per Wafer 80

Die Per Mask 1:1









Ascend 910C Processor Die

Made By TSMC N7 Level

Si interposer-Die Per Wafer

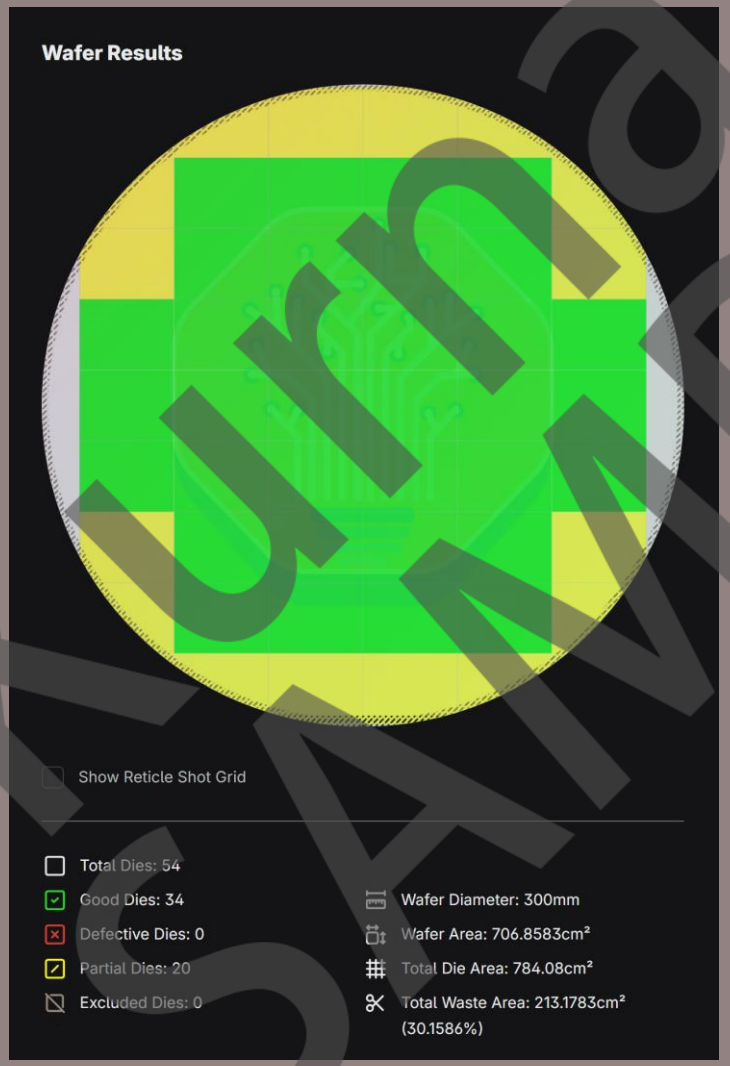
No image

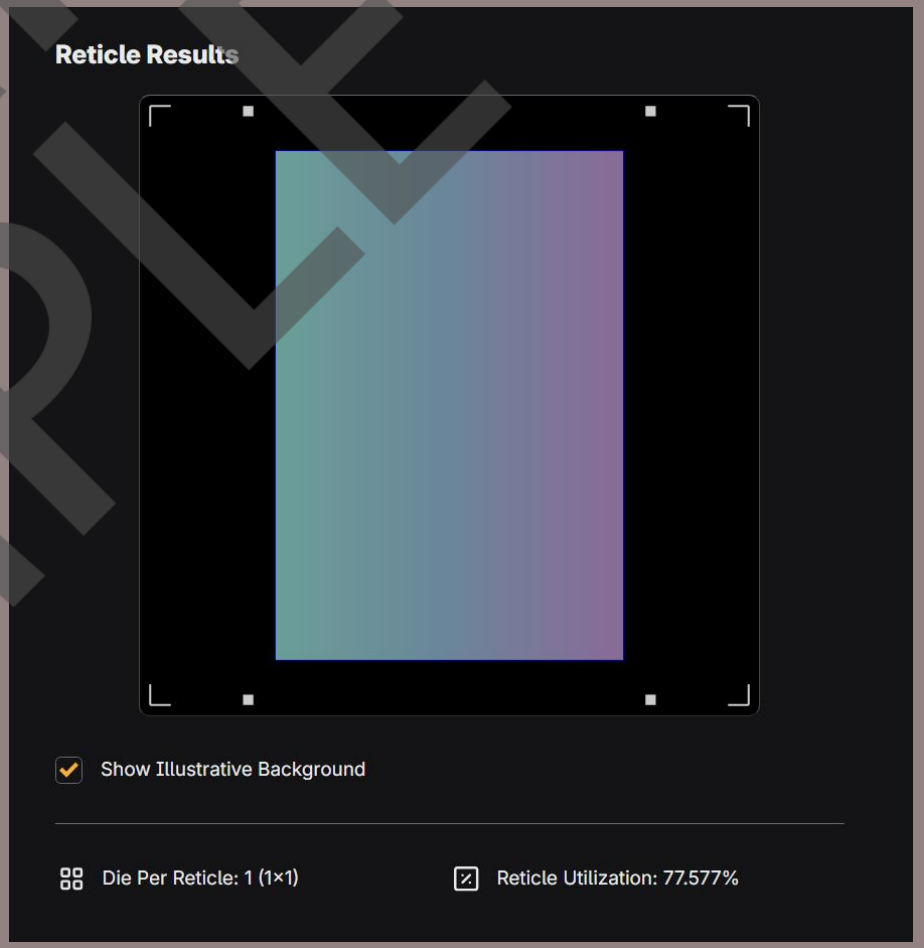
Si interposer

Ascend 910C Si interposer
Package size: 44 x 33

The interposer need 2 lithos

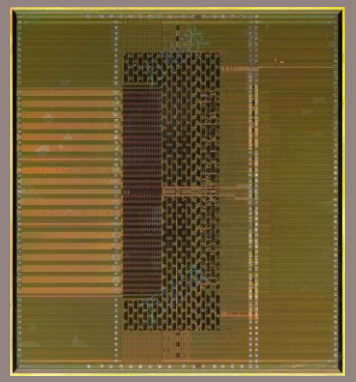
Die Per Wafer 34
Die Per Mask 1:2





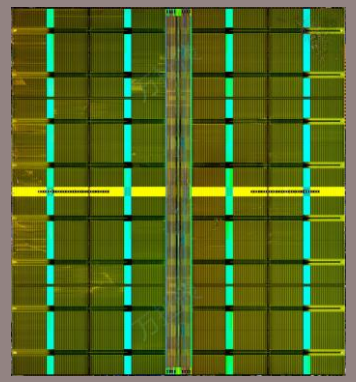
Need 2 Mask

HBM Dram Stack-Die Per Wafer



HBM Logic Die

Package size: 9.59x10.52

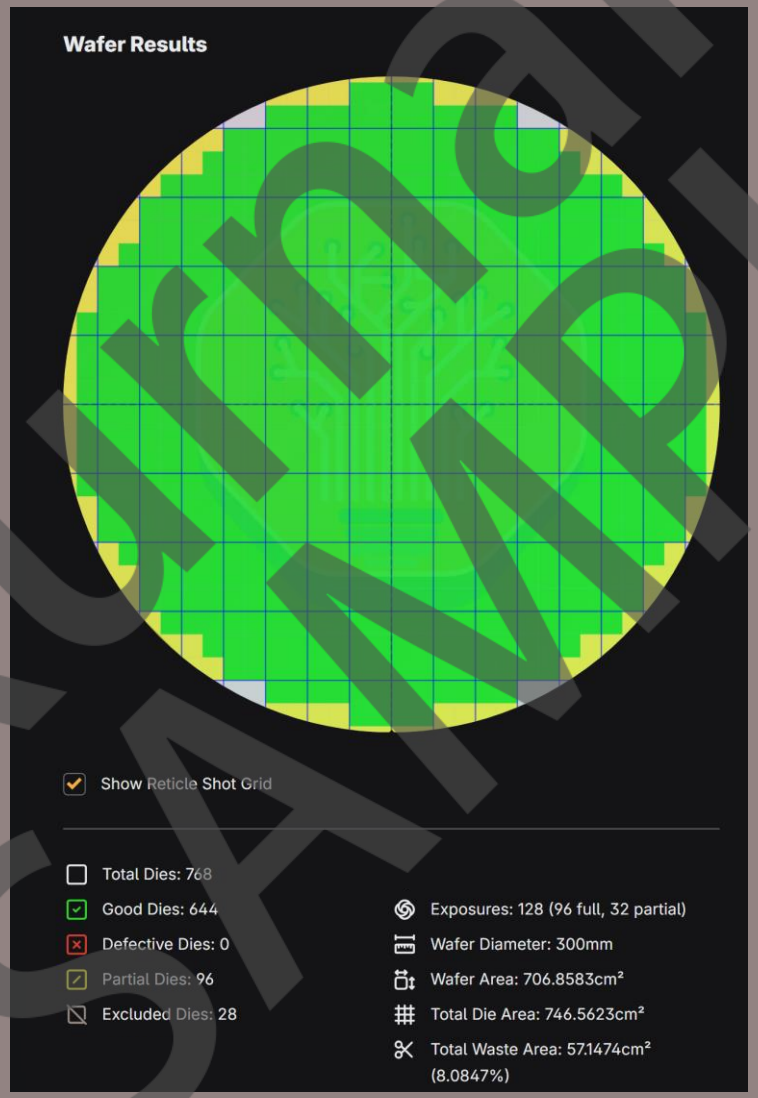


HBM Memory Die

Package size: 9.59x10.52

Die Per Wafer 644

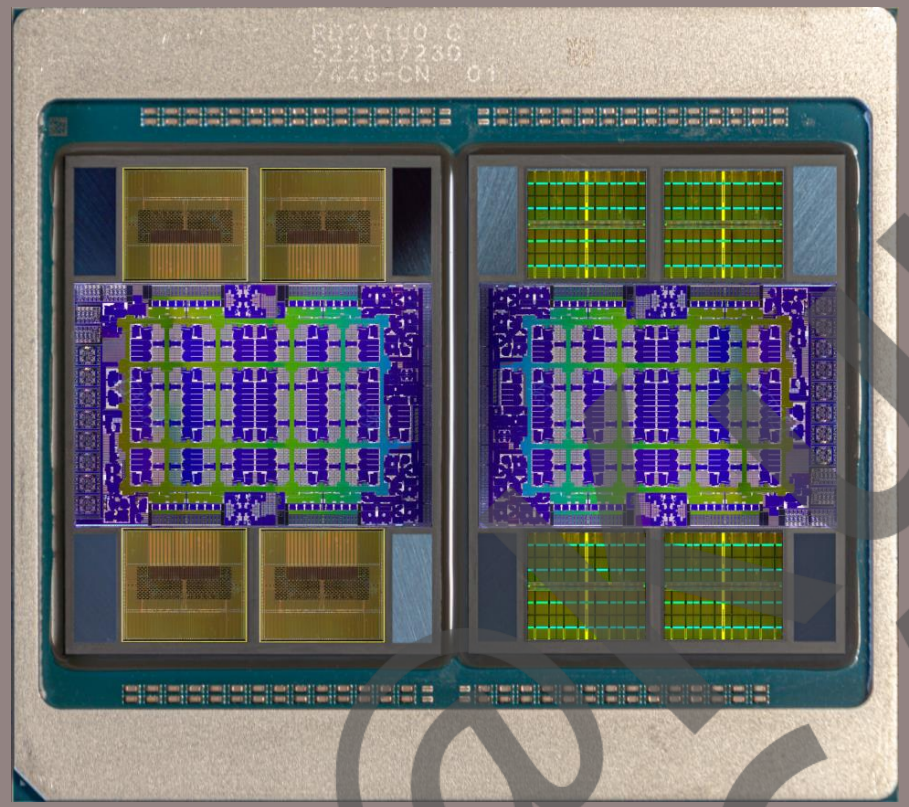
Die Per Mask 6:1

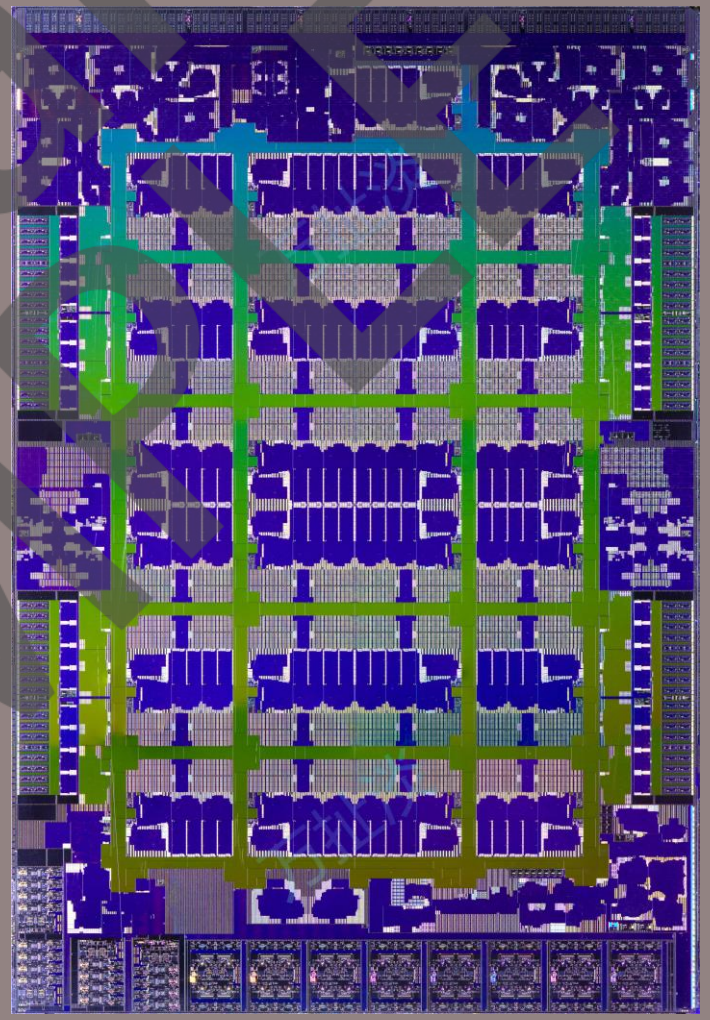


Decaped

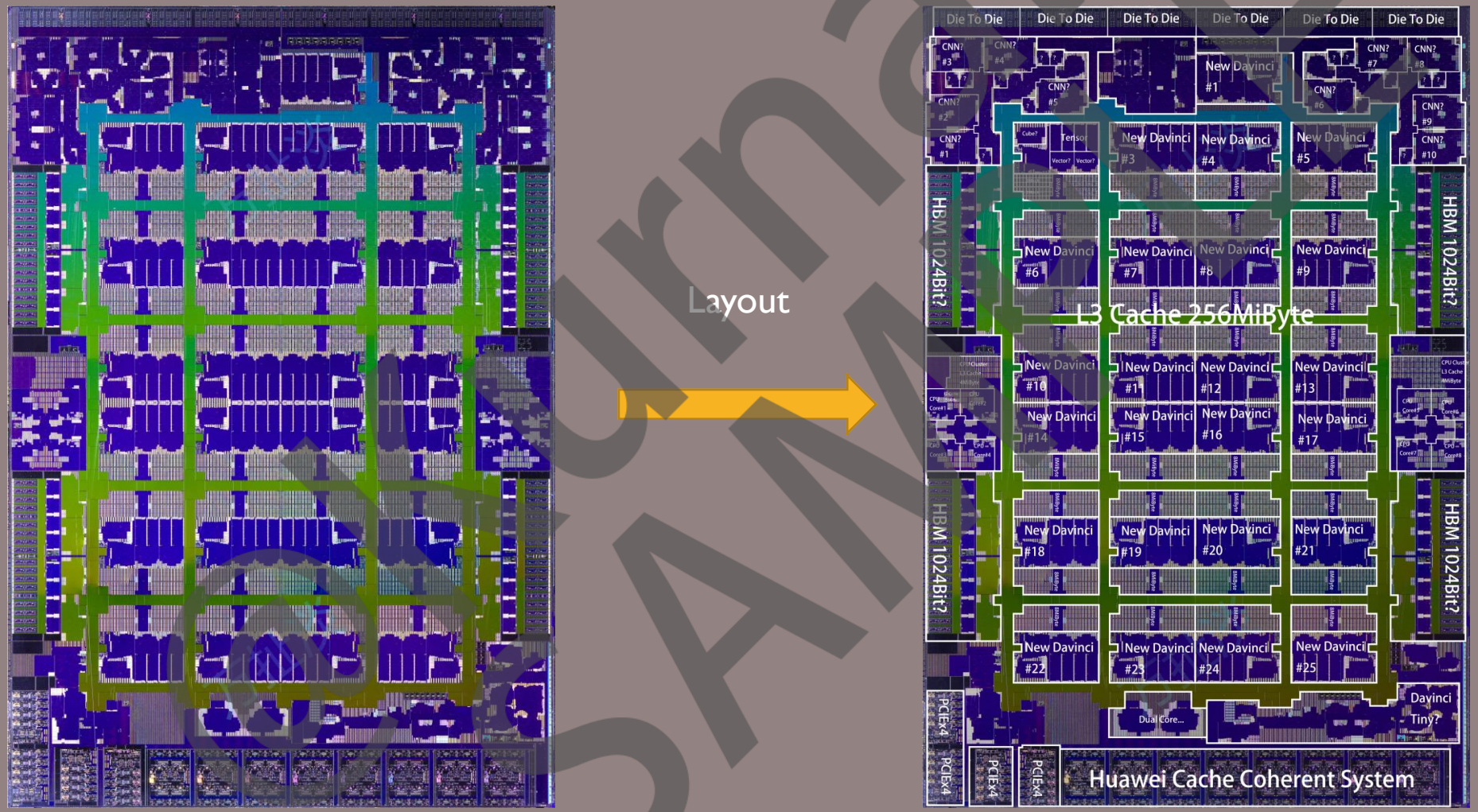
Ascend 910C

Decapped-Dieshot

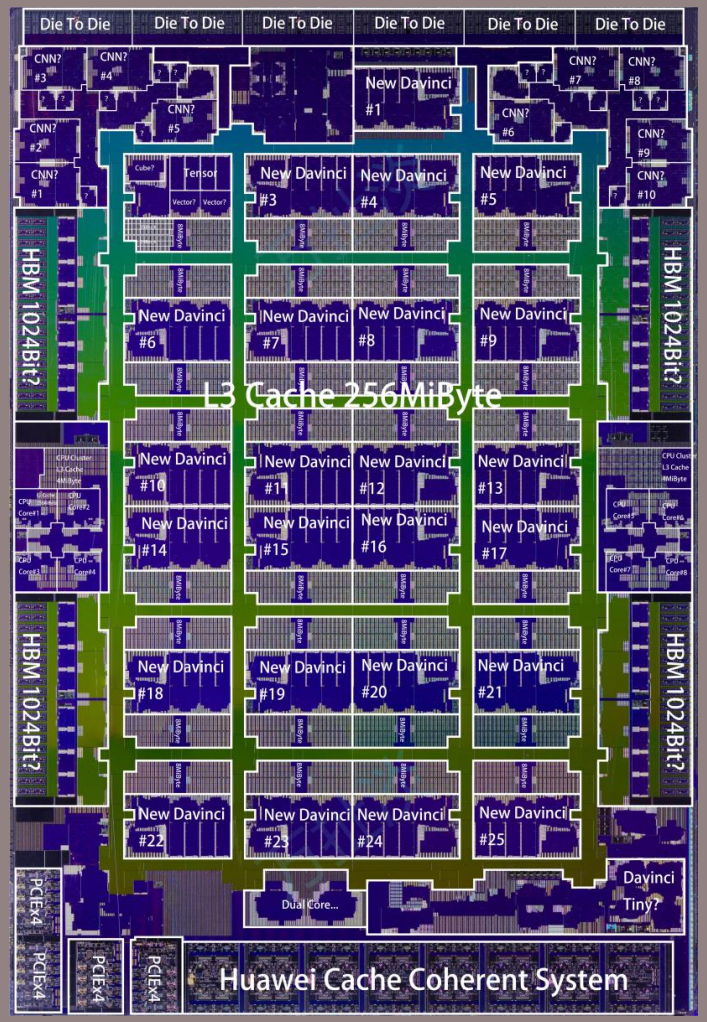




Decapped-Dieshot



Decapped-Dieshot



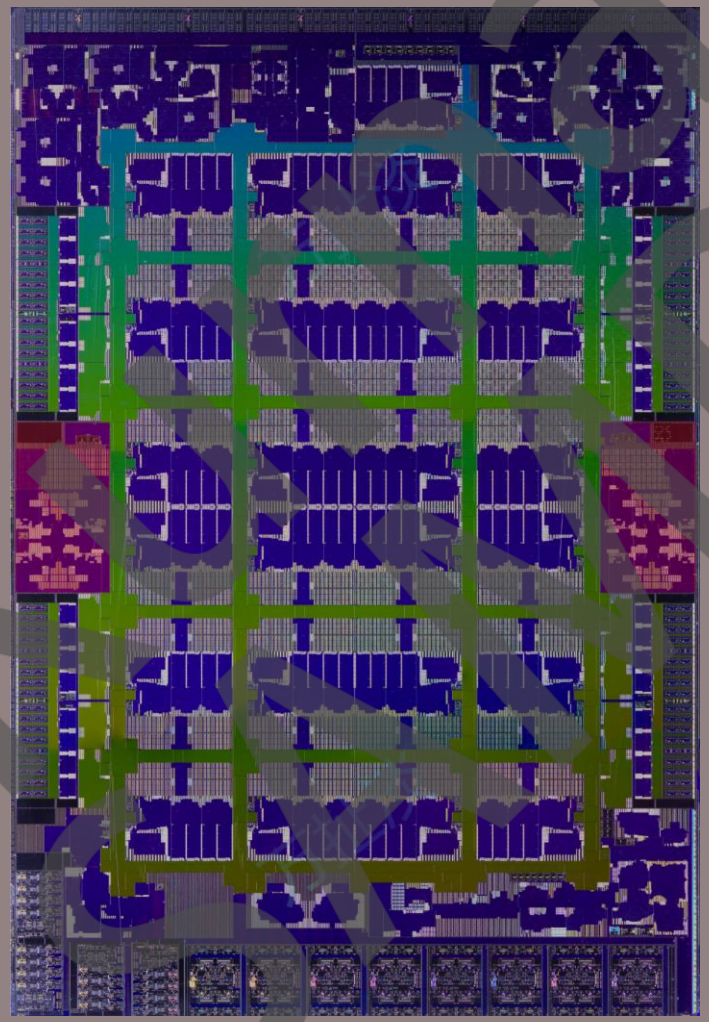
Davinci NPU Core number :	25
NPU L3 Cache:	256MiB
CPU Cluster:	2x4
CPU L3 Cache:	4Core per 4MiB
CPU L2 Cache:	256KiB
IO:	
HBM Channel:	4x1024Bit=4096Bit
PCIE channel:	4x4
Die to Die:	6 Cluster
Huawei Cache coherent :	Have

On chip analyze

CPU

On chip analyze-CPU

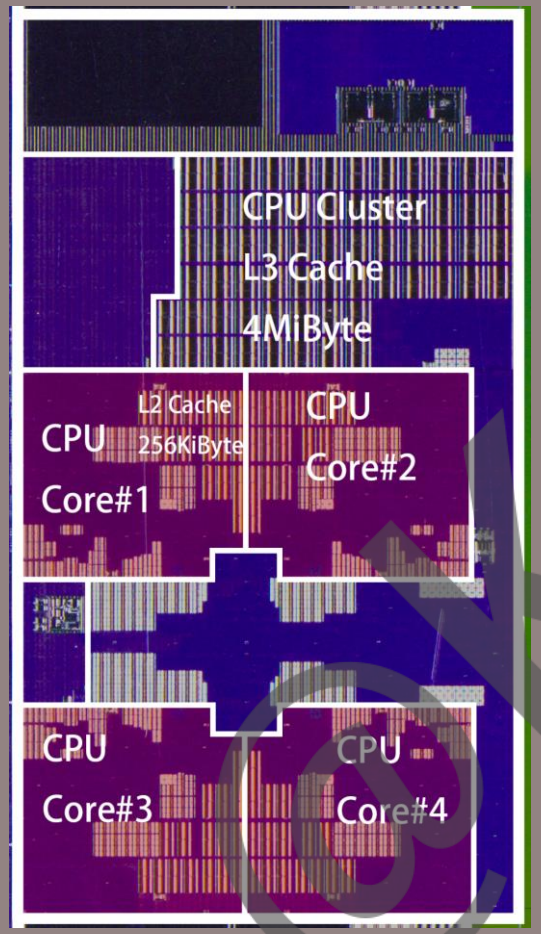
CPU Cluser #1 （4Core）

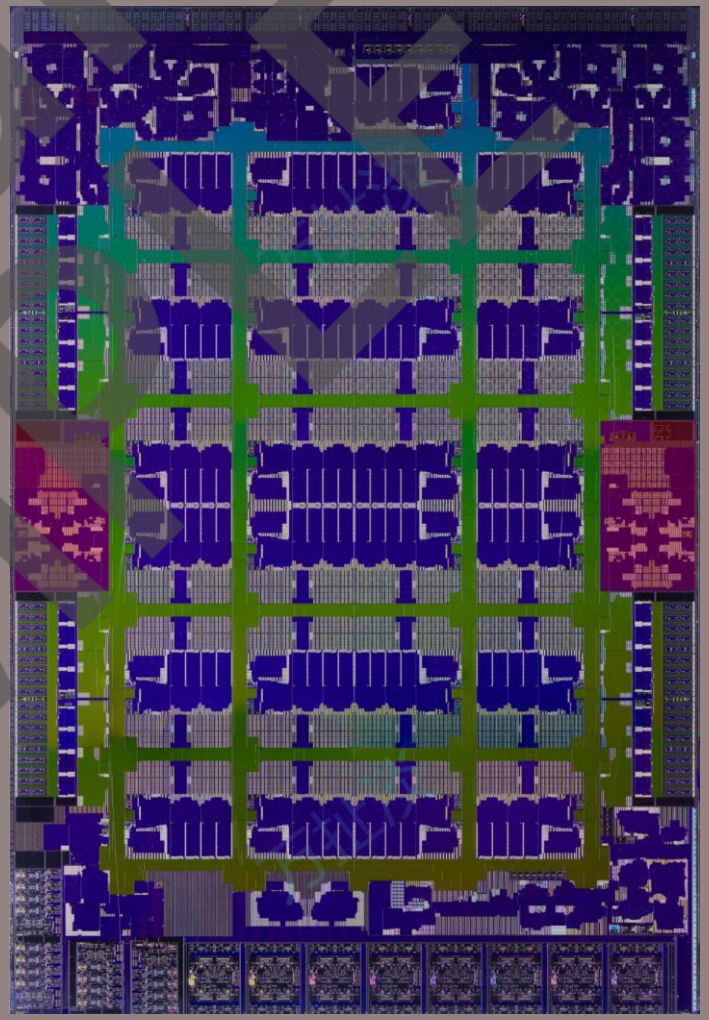


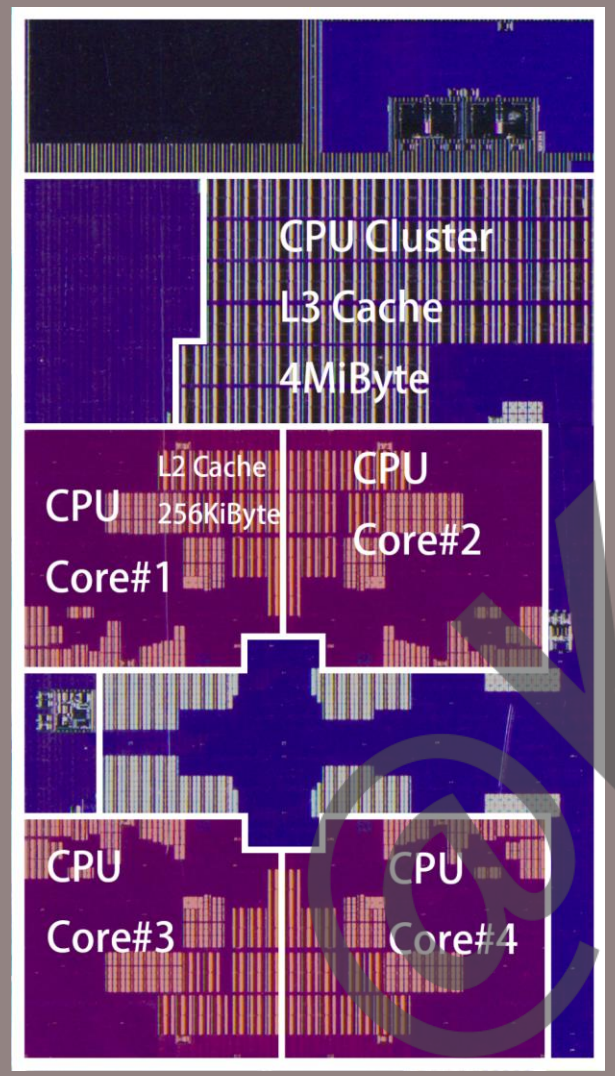
CPU Cluser #2 （4Core）

On the chip left and right
There have 2 CPU Cluster
Mirror each other

On chip analyze-CPU



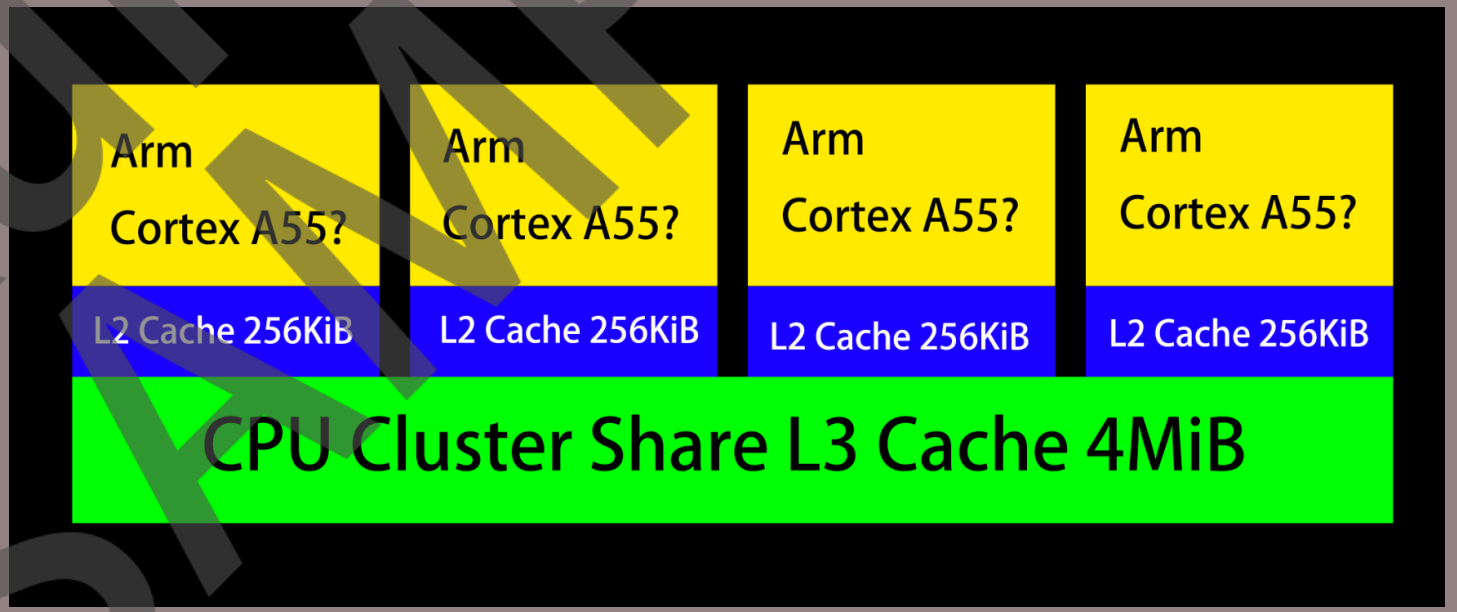




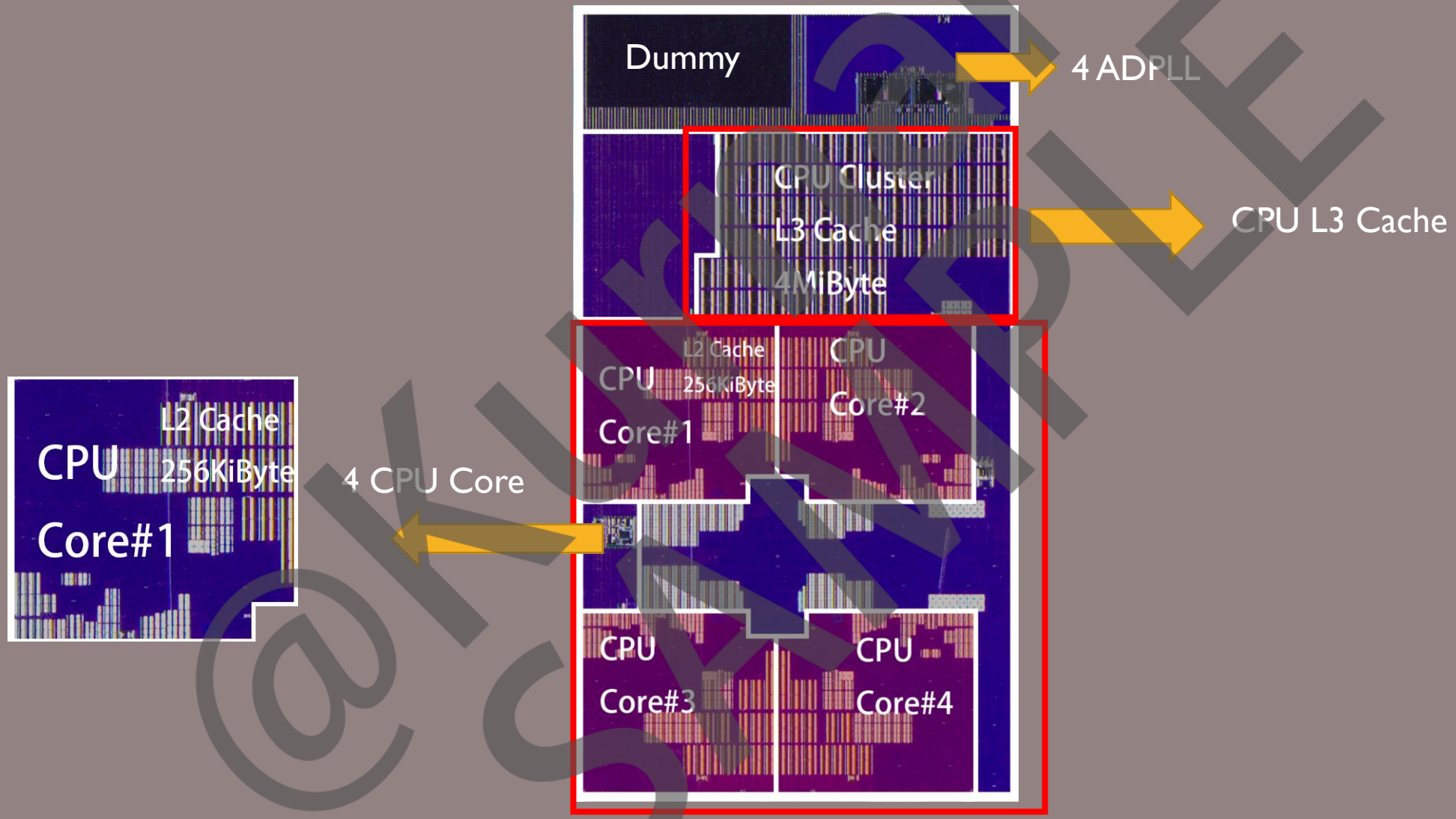
4 CPU Core share 4MiB L3 Cache

1 CPU Core have self 256KiB L2 Cache

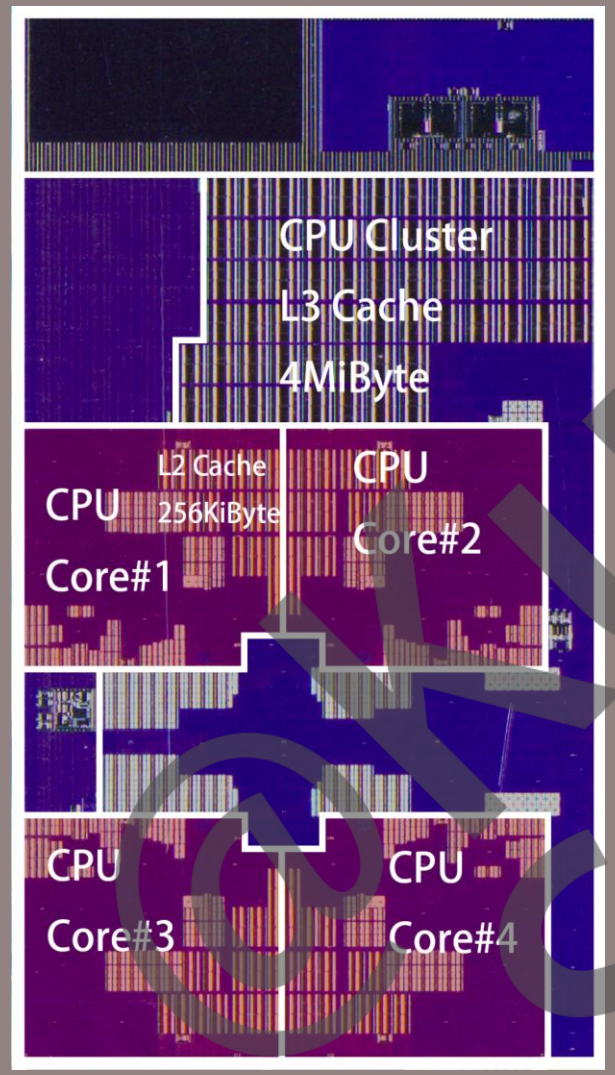
Looks like Arm Cortex A55?

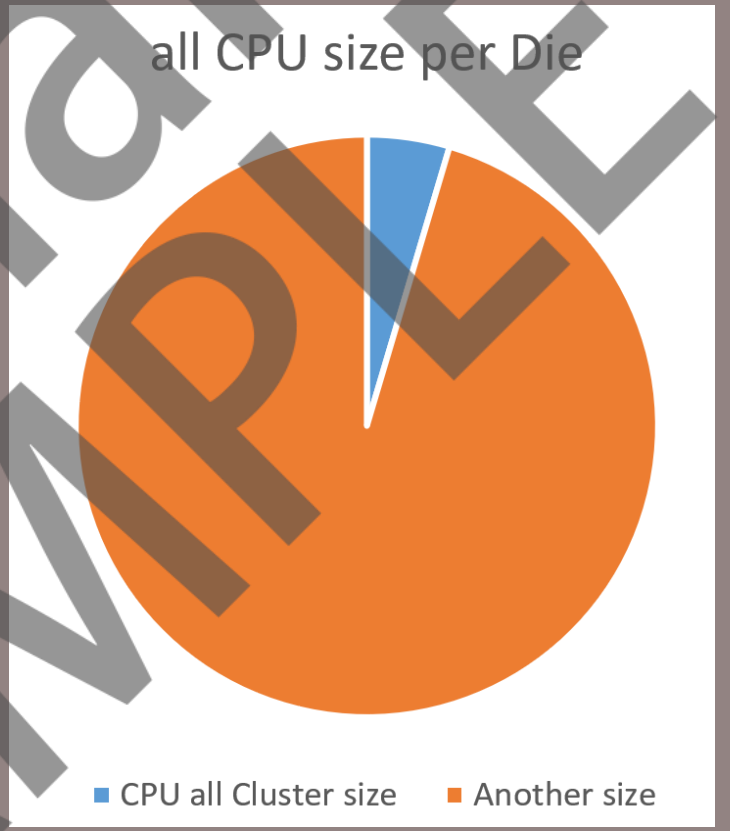


On chip analyze-CPU



On chip analyze-CPU

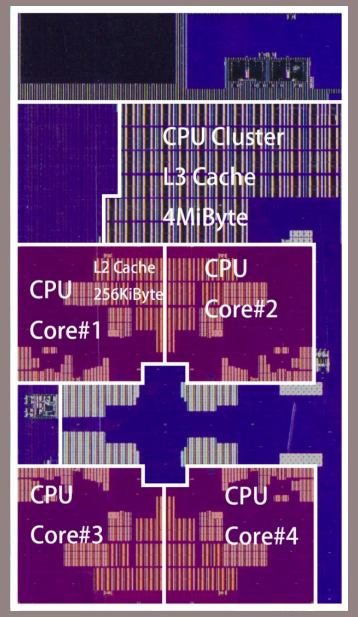


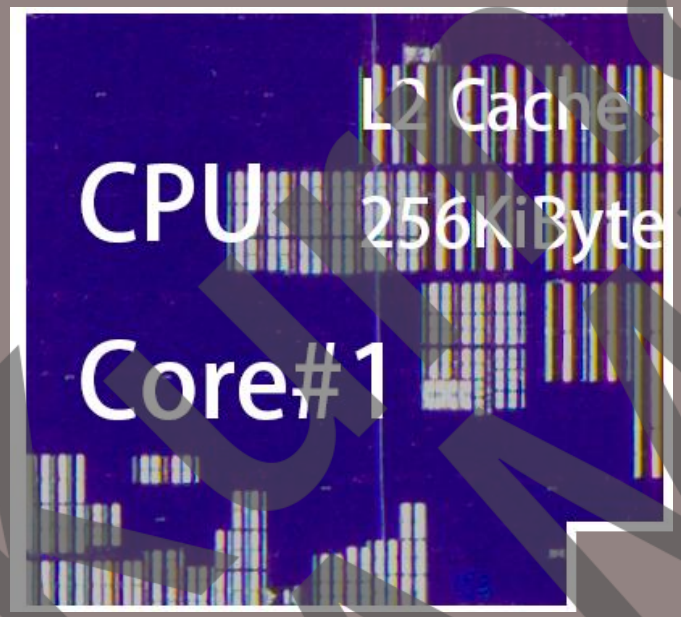


CPU Cluster area: 15.27mm2 x2

2.294%/4.588% of all Dies

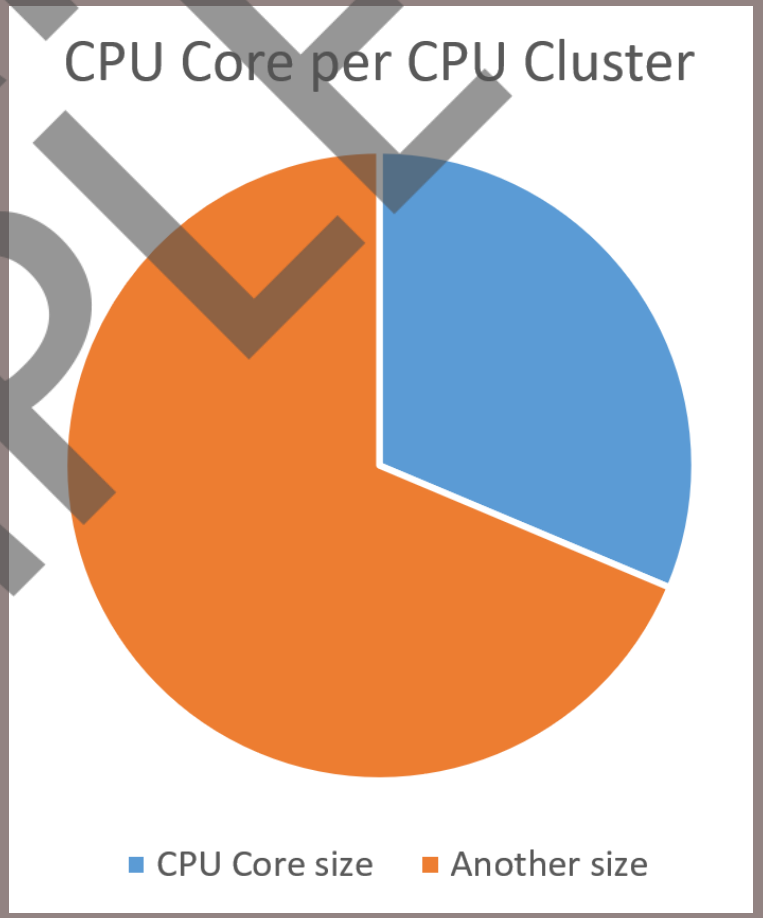
On chip analyze-CPU

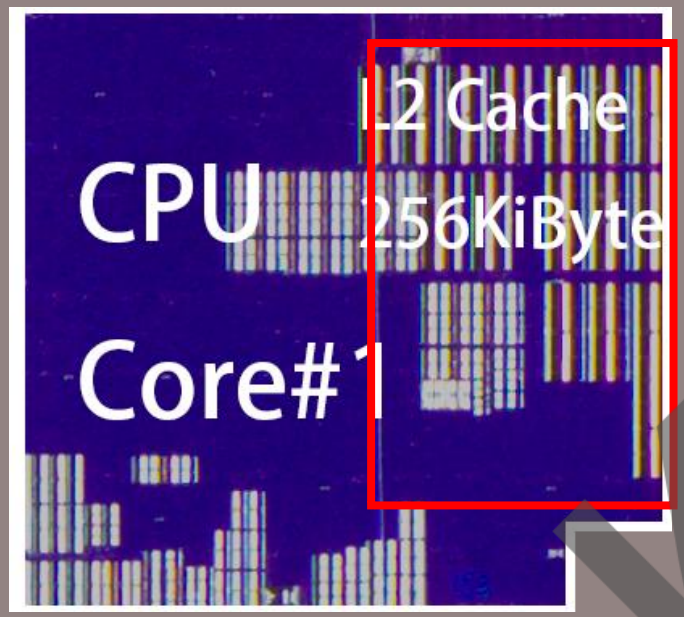


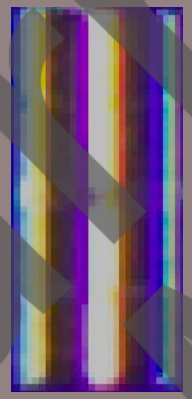


CPU Core size: 1.564mm2

10.24%/40.97% of CPU Cluster



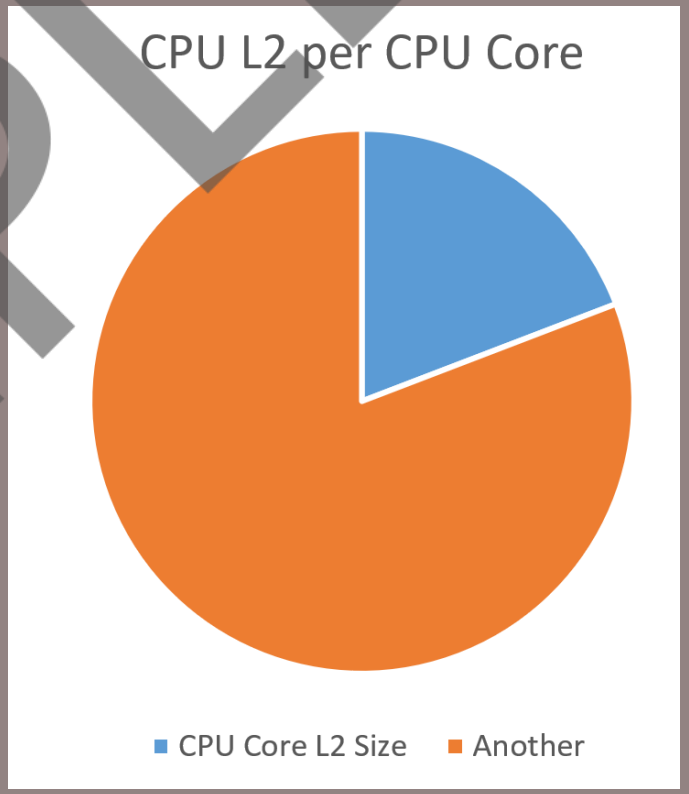




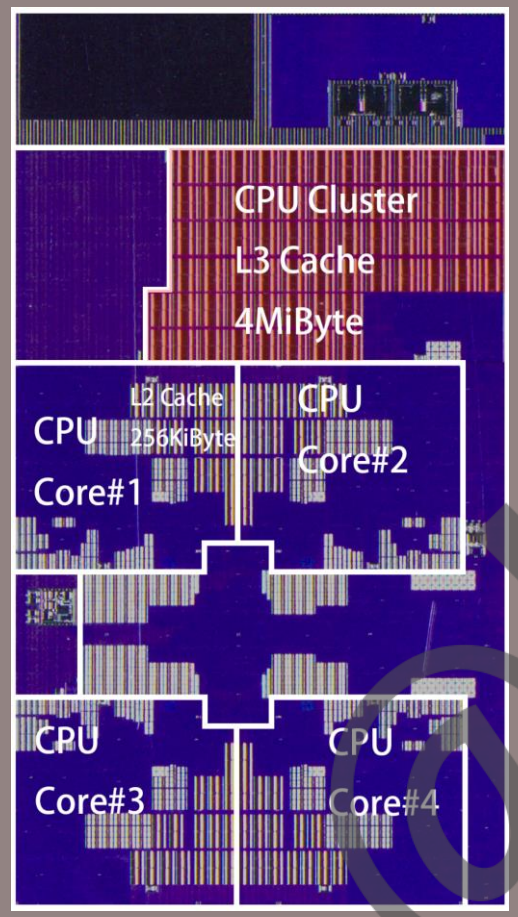
CPU L2 sram Block: 16KiB
Cache Density: 0.8928MiB/mm2
1.12mm2/MiB

CPU L2 Cache: 256KiB
L2 Cache size: 0.3mm2

CPU L2 per CPU Core: 19.18%

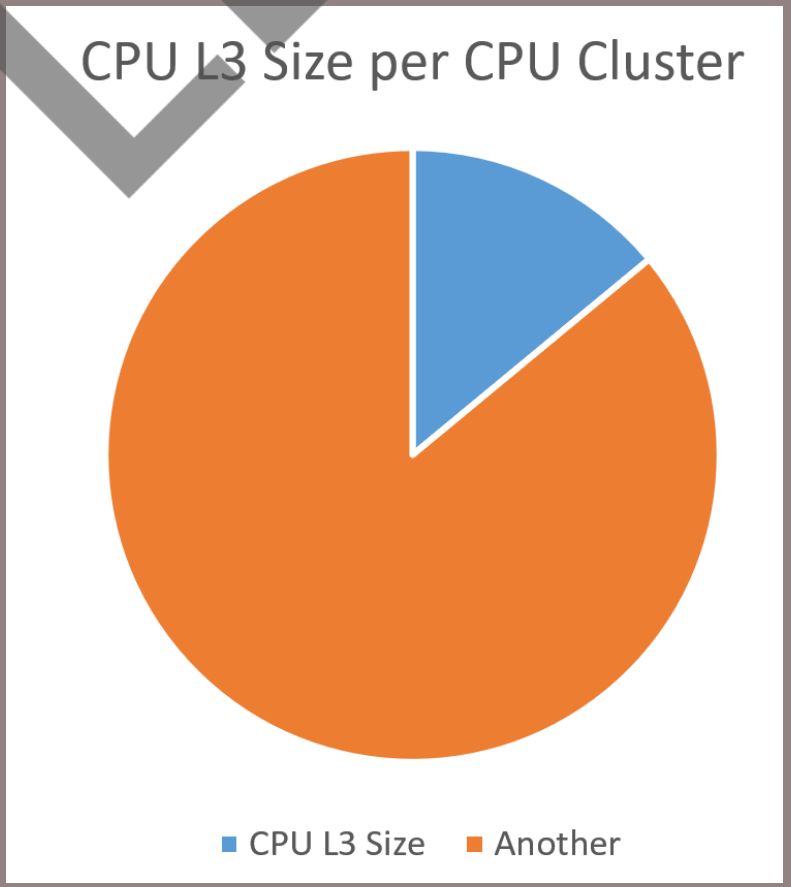


On chip analyze-CPU-L3 Cache

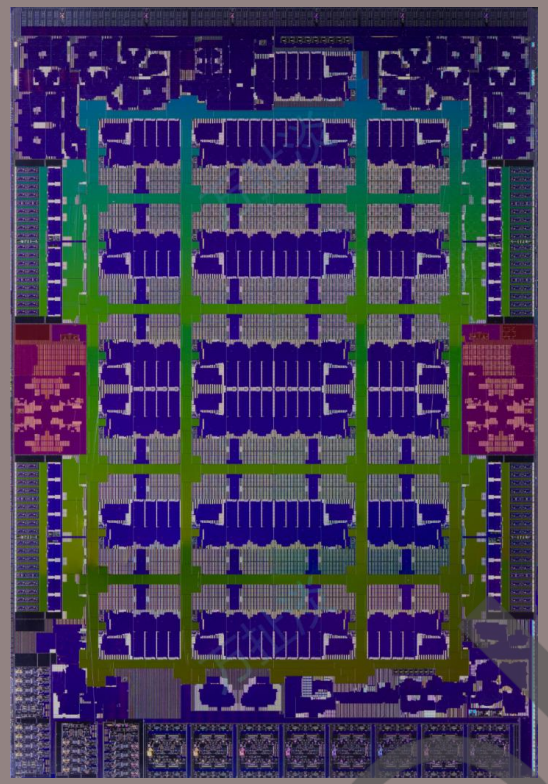


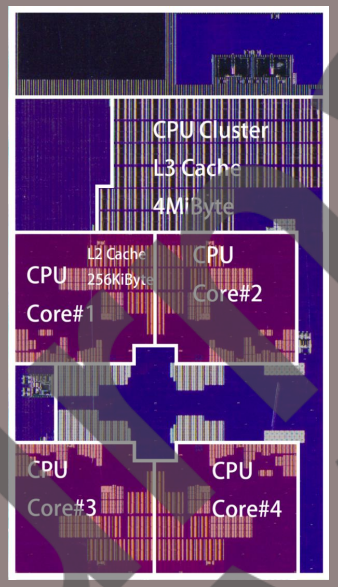
CPU L3 Cache size: 2.138mm2
CPU L3 sram Block: 64KiB
Cache Density: 2MiB/mm2
0.5mm2/MiB

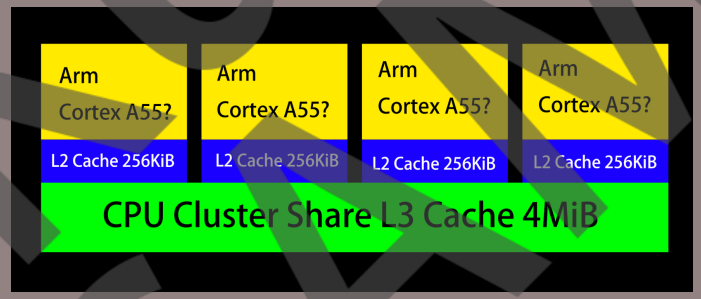
CPU L3 per CPU Core: 19.18%

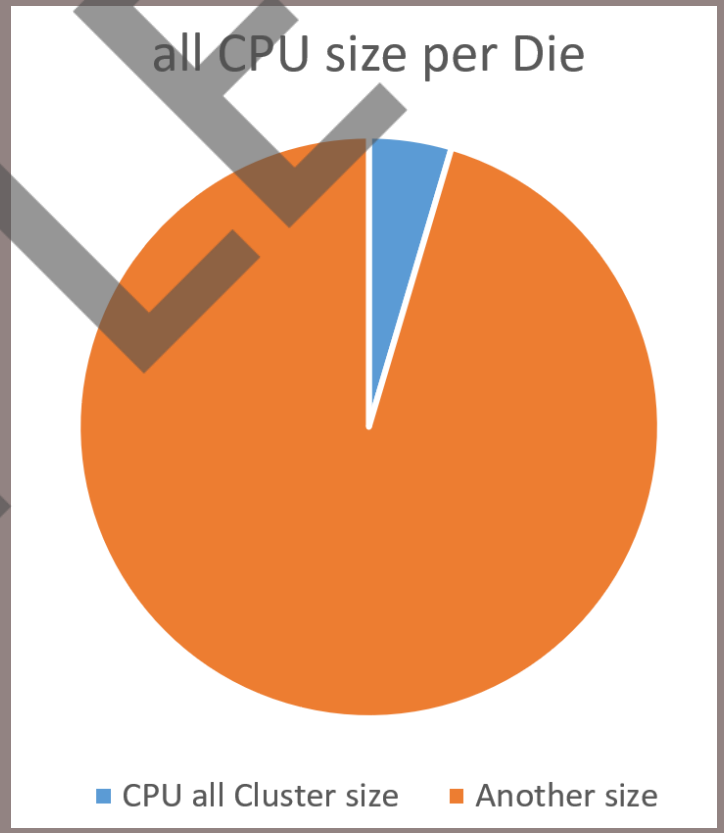


On chip analyze-CPU-End



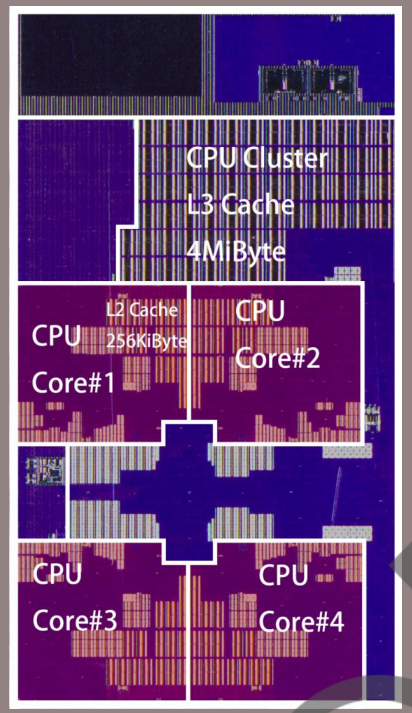


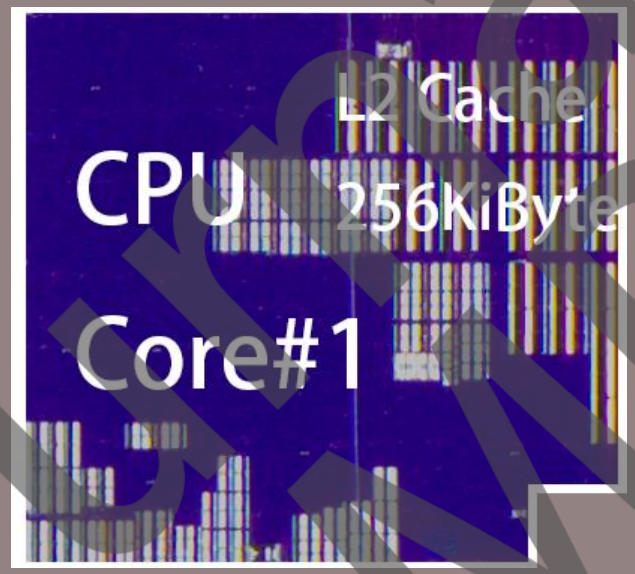


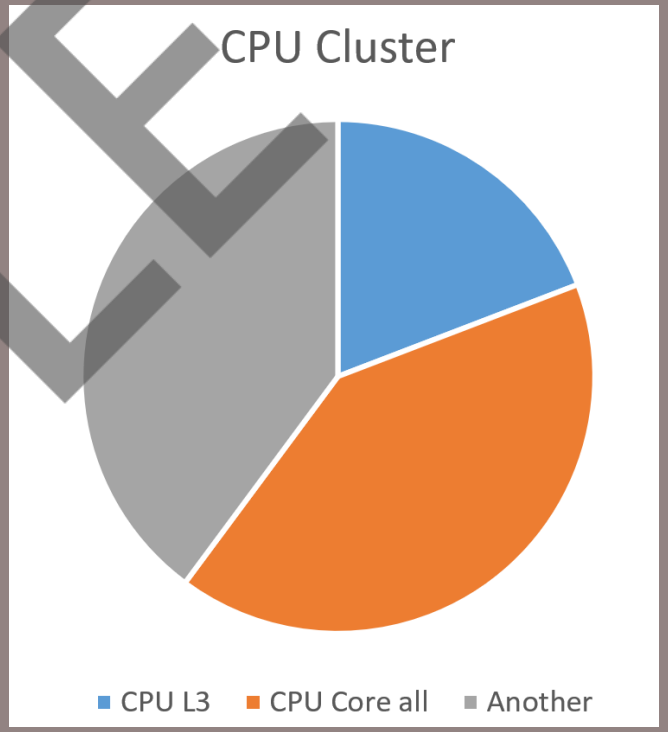


In general,
Each Processor die has 2 CPU clusters
Each with 4 cores that are suspected to be Arm A55, sharing 4MiB of L3
In totally Ascend 910C has 4x4=16Core CPU

CPU accounts for 4.58% of all dies







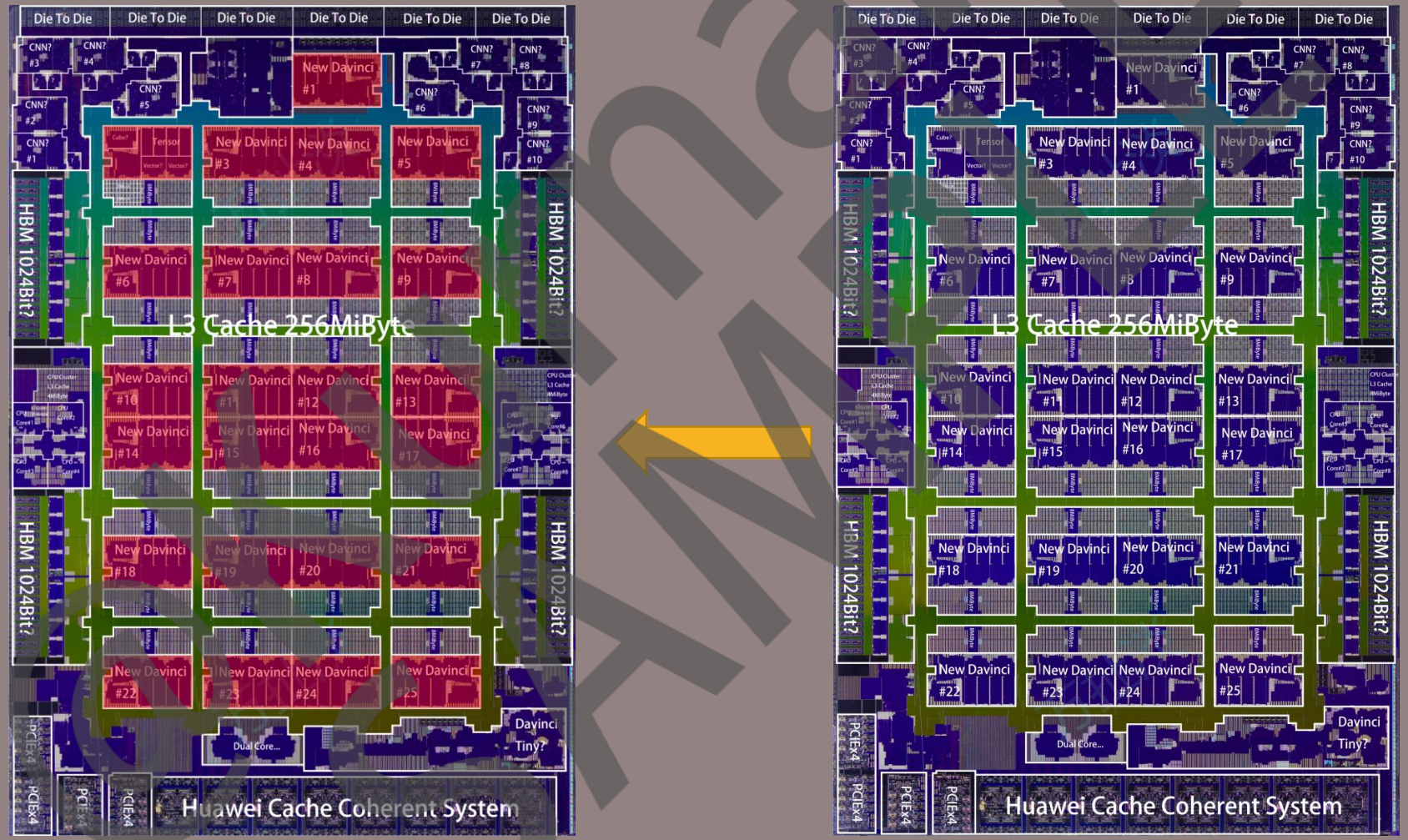
In the CPU cluster
40.97% of the area is the CPU core
and 19.18% of the area is the 4MiB L3 of the CPU.

	Per Cluster
CPU L3	19.18%
CPU Core	40.97%

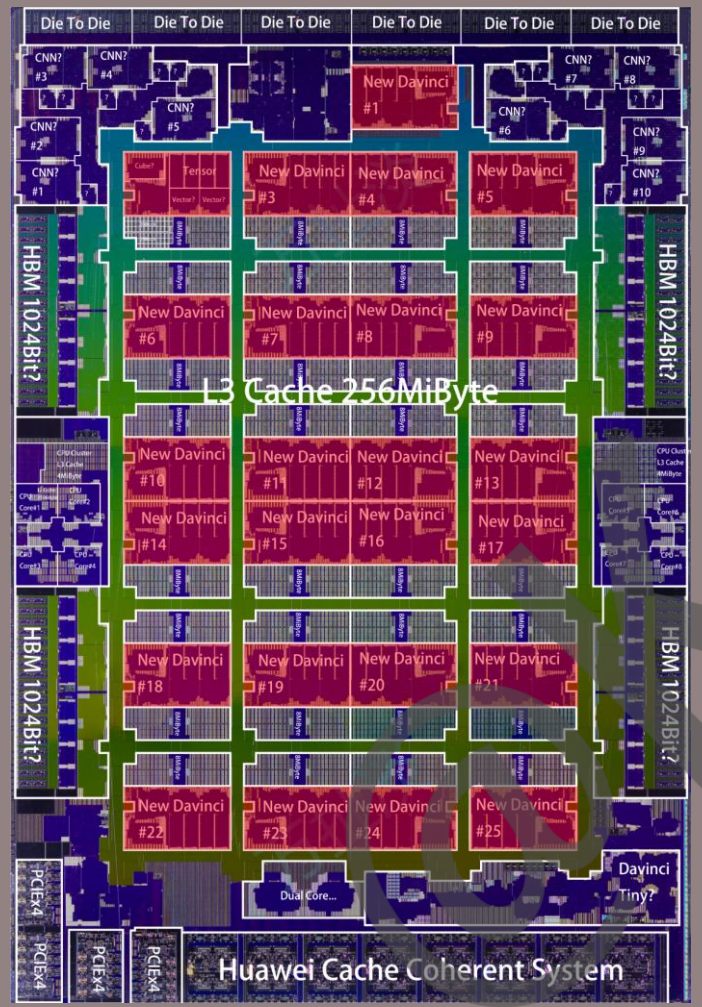
On chip analyze

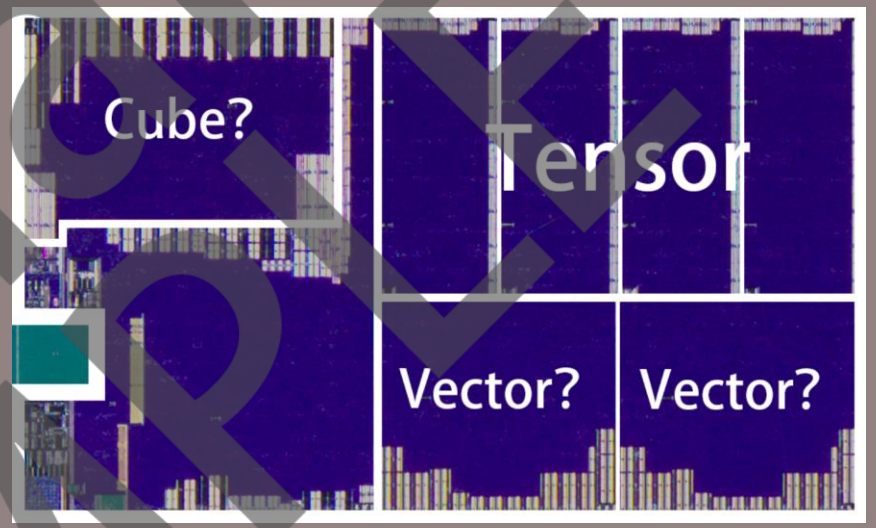
NPU

NPU Core



NPU Core





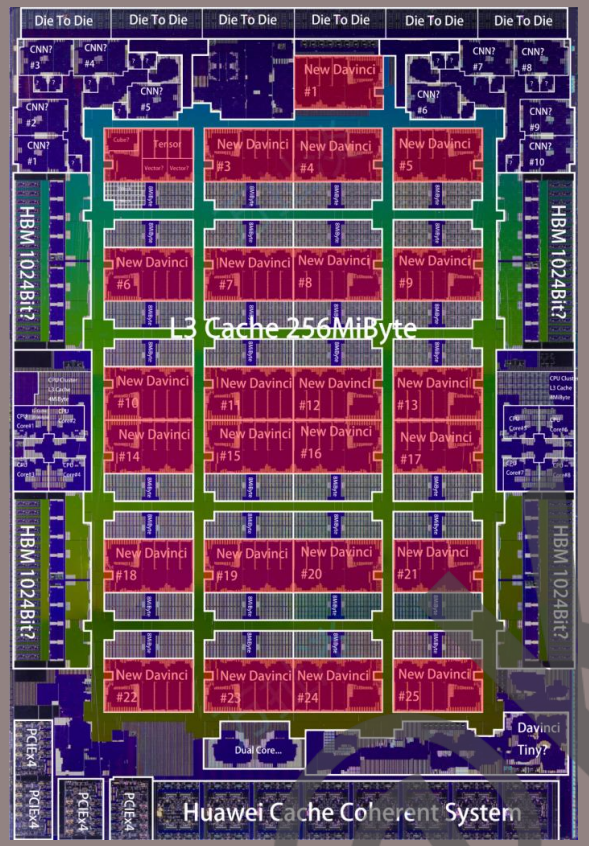
There have 25 Cores NPU in Ascend 910C Processor Die

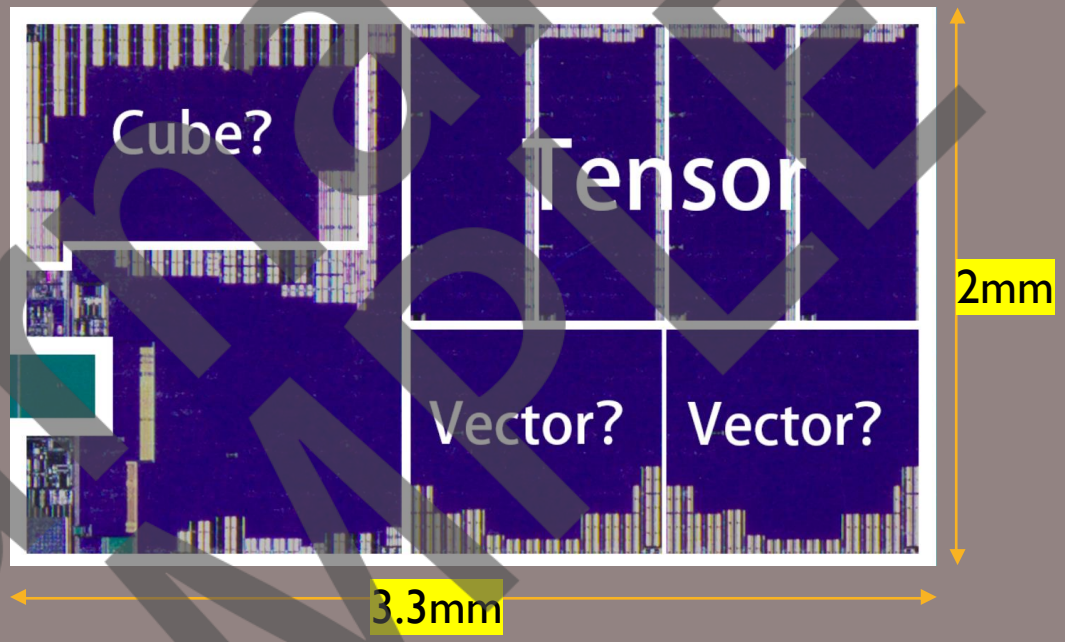
NPU L3

x 32

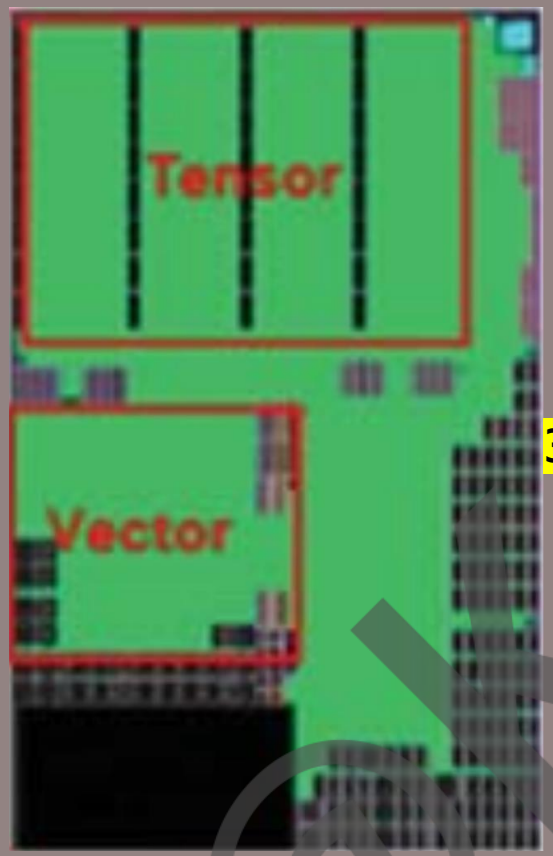
There have 256MiB L3 Cache in Ascend 910C Processor Die

NPU Core





NPU Core size: 6.51mm2



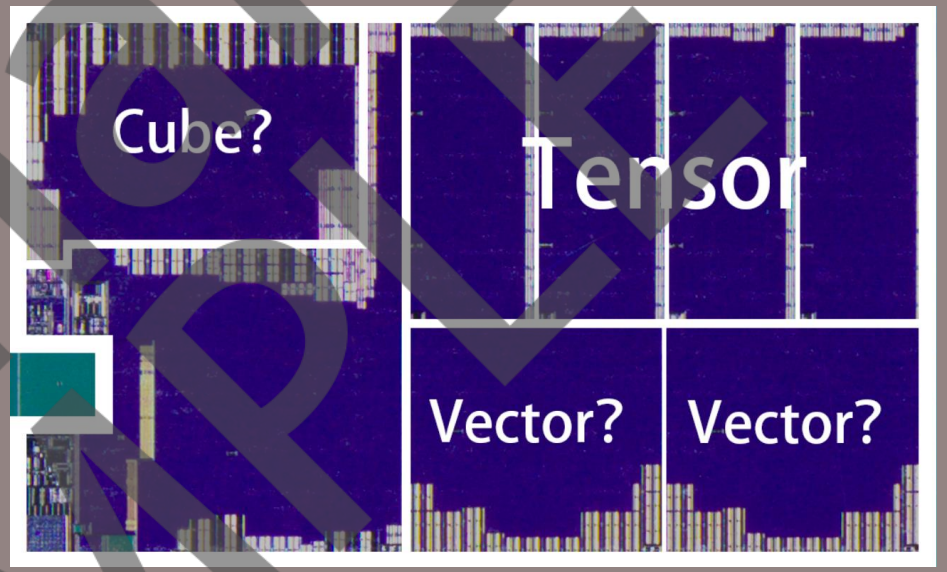
3mm

1.9mm

Ascend 910 NPU Core

NPU Core size： 5.18mm2

Same Rule



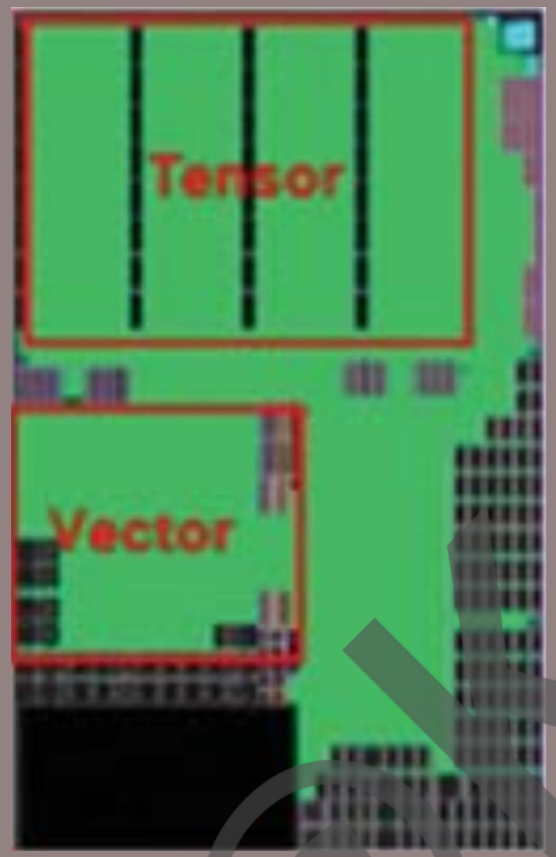
2mm

3.3mm

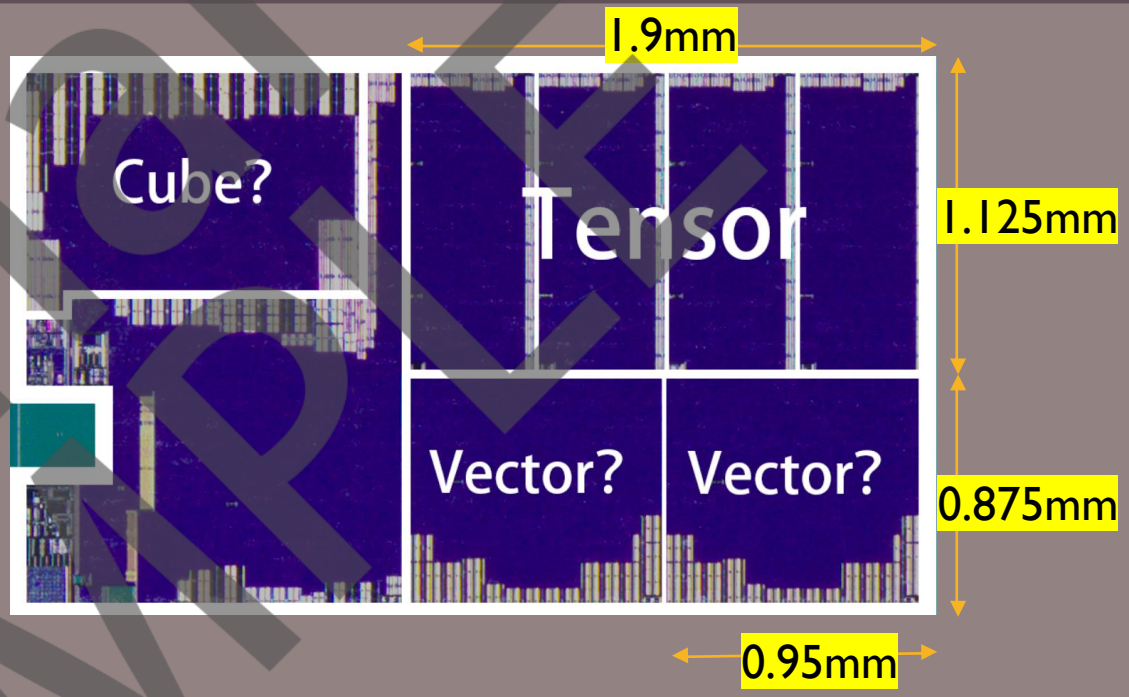
Ascend 910C NPU Core

NPU Core size： 6.51mm2

Bigger than 25.67%



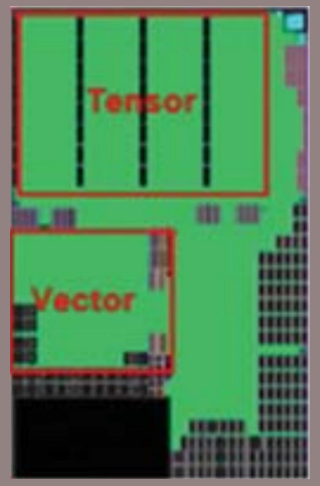
Ascend 910 7nm
8 TFLOPS Tensor 1.6mm × 1.2mm
128 GFLOPS Vector 0.9mm × 1mm



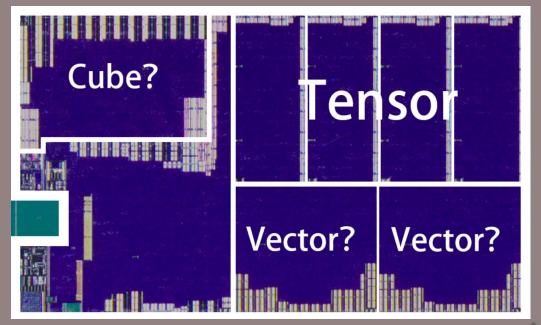
Ascend 910C NPU Core

Tensor 1.9mm x 1.125mm
Vector 0.875mm x 0.95mm

NPU Core VS Tensor

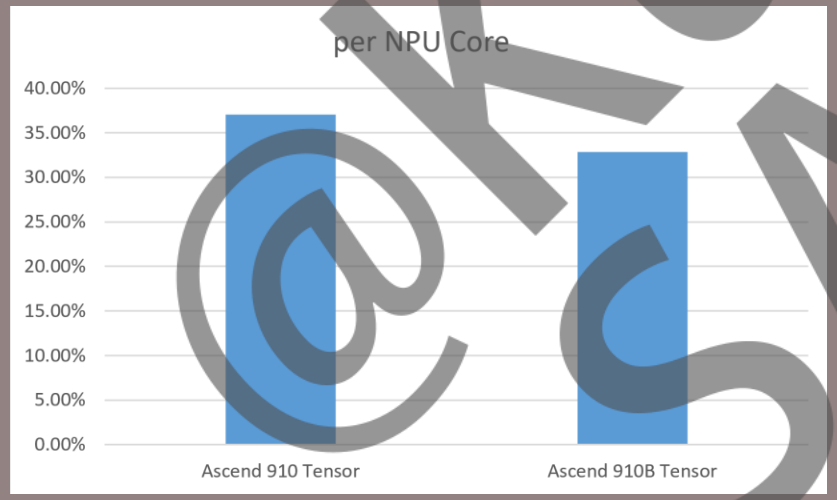


Ascend 910 NPU Core



Ascend 910C NPU Core

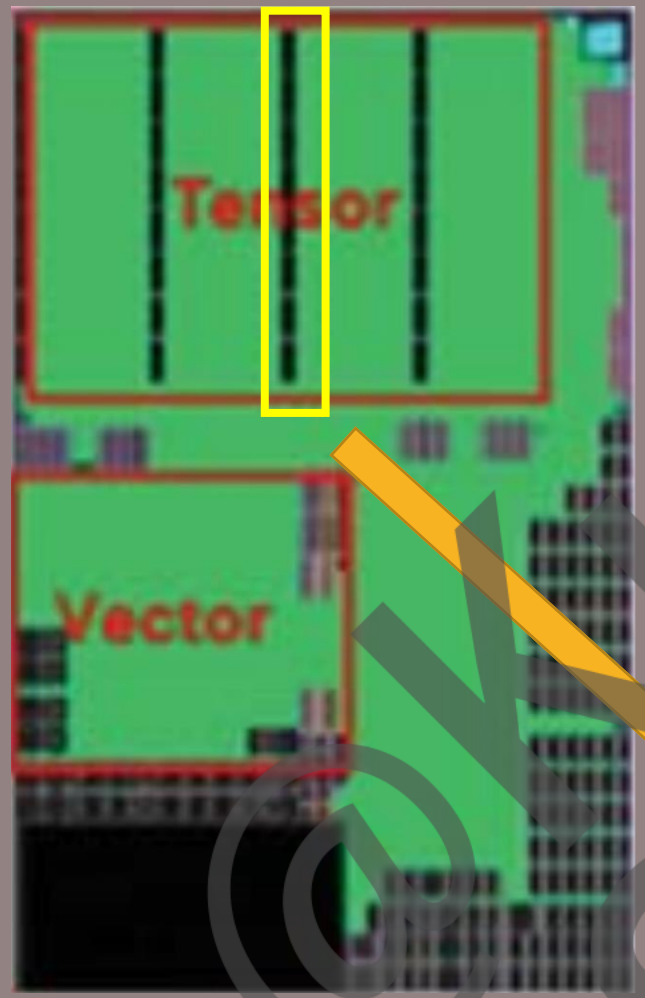
	per NPU Core
Ascend 910 Tensor	37.07%
Ascend 910C Tensor	32.83%



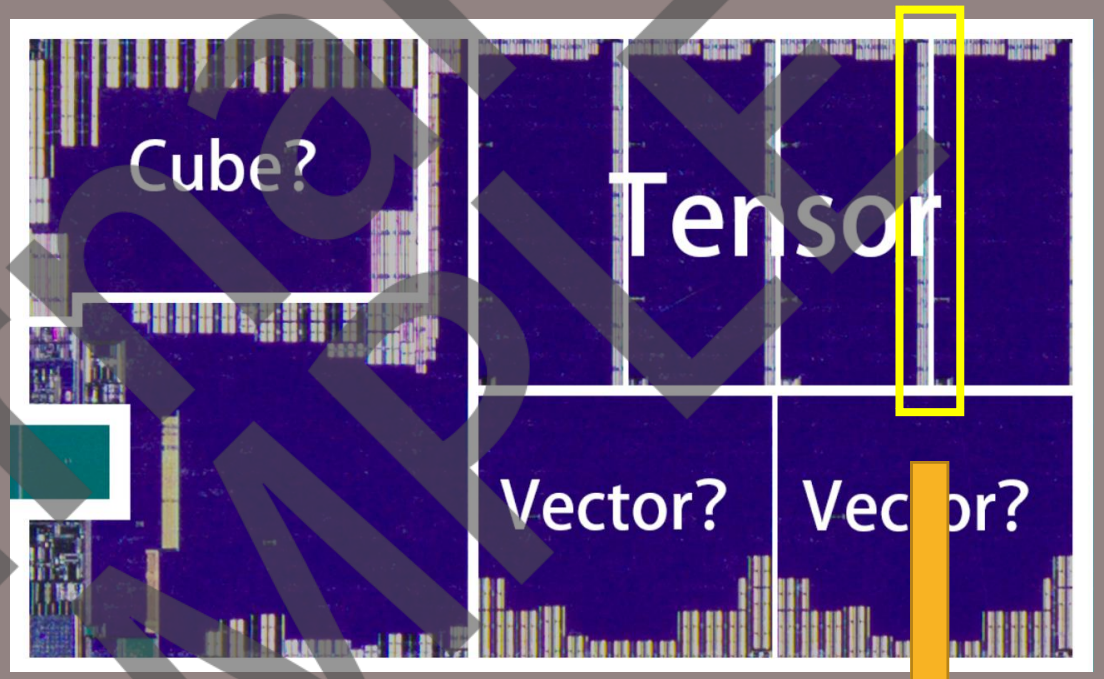
Ascend 910 Tensor	1.92
Ascend 910C Tensor	2.1375

Under the same process, the area of 910C Tensor is 11.33% larger

But in fact
the proportion of 910C Tensor in NPU cores has decreased by 4.24%.



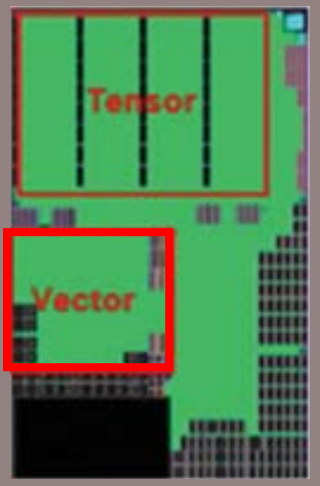
Ascend 910 NPU Core



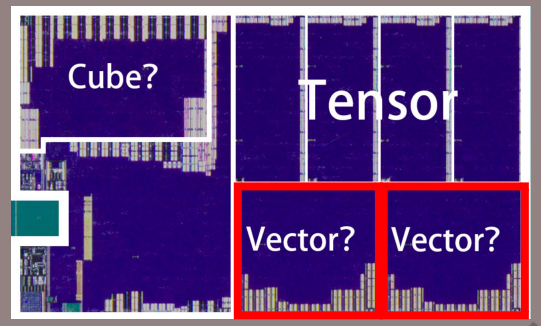
Ascend 910C NPU Core

In the 910 Tensor,
each pipeline has 8 blocks of cache,
which is the same as the 910C.

NPU Core VS Vector



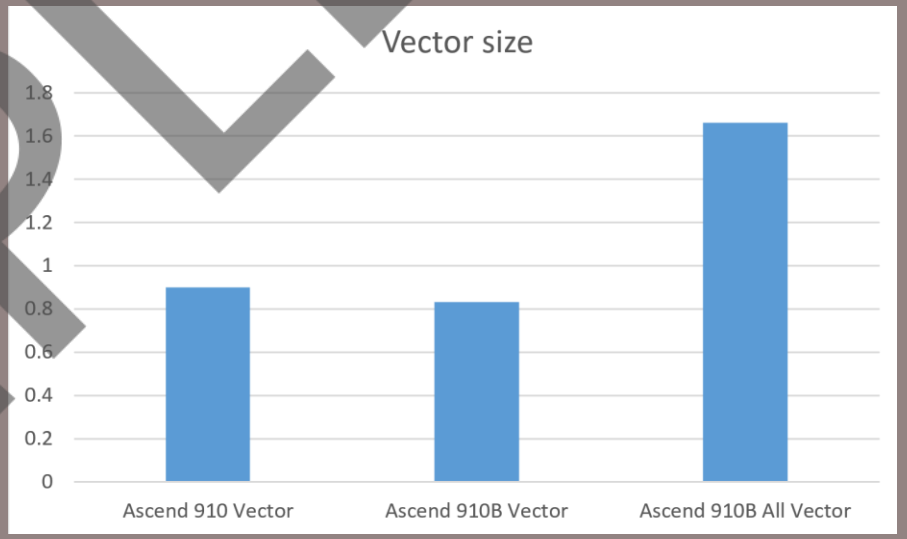
Ascend 910 NPU Core



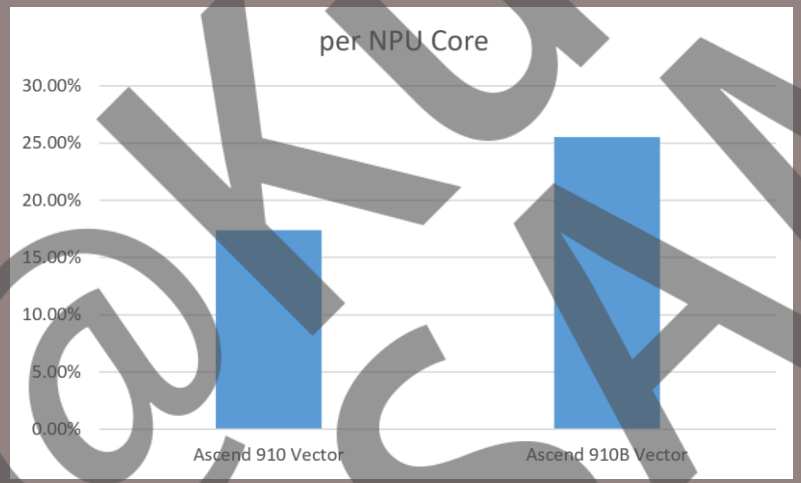
Ascend 910C NPU Core

In terms of Vector,
the 910C has two sets of Vector,
while the 910 only has one set

	size
Ascend 910 Vector	0.9
Ascend 910C Vector	0.83125
Ascend 910C All Vector	1.6625



	per NPU Core
Ascend 910 Vector	17.37%
Ascend 910C Vector	25.54%

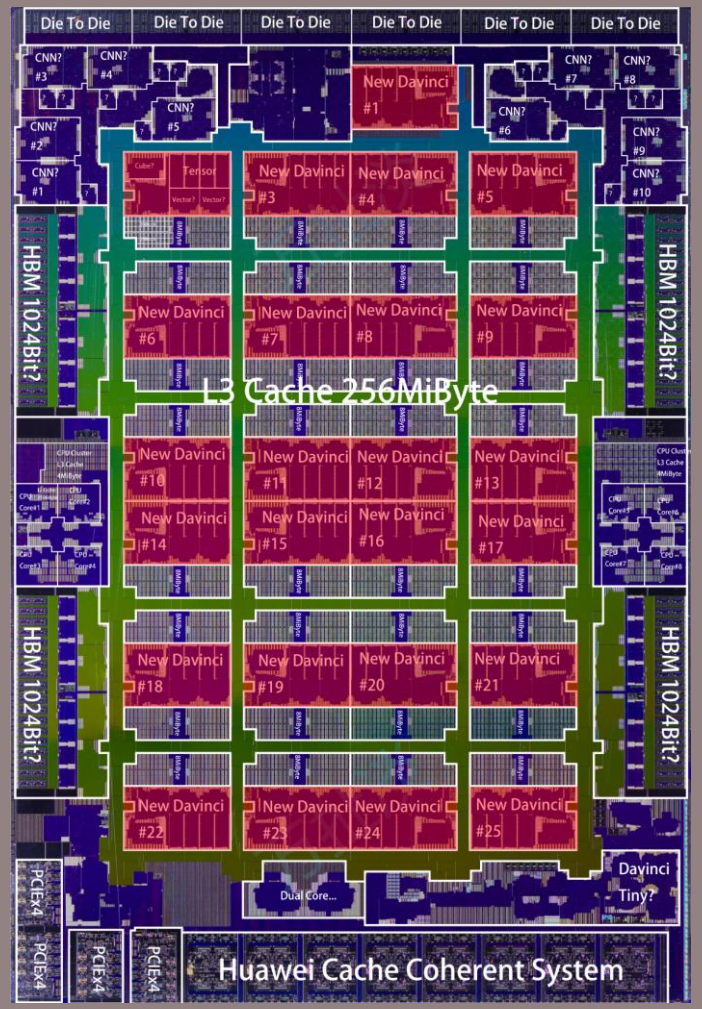


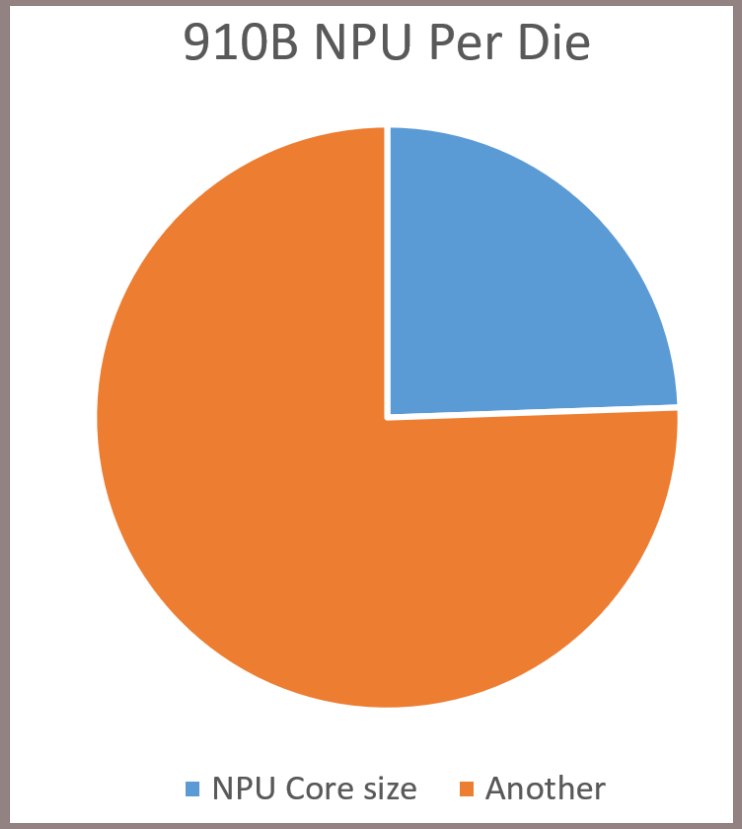
In terms of single vector,
the area of 910 is 8.27% larger than that of 910C.

But 910C has two sets of vectors,
so the area of 910C is 84.72% larger than that of 910.

Therefore,
the proportion of Vector in 910C to the entire NPU Core is 8.17% larger than that of 910.

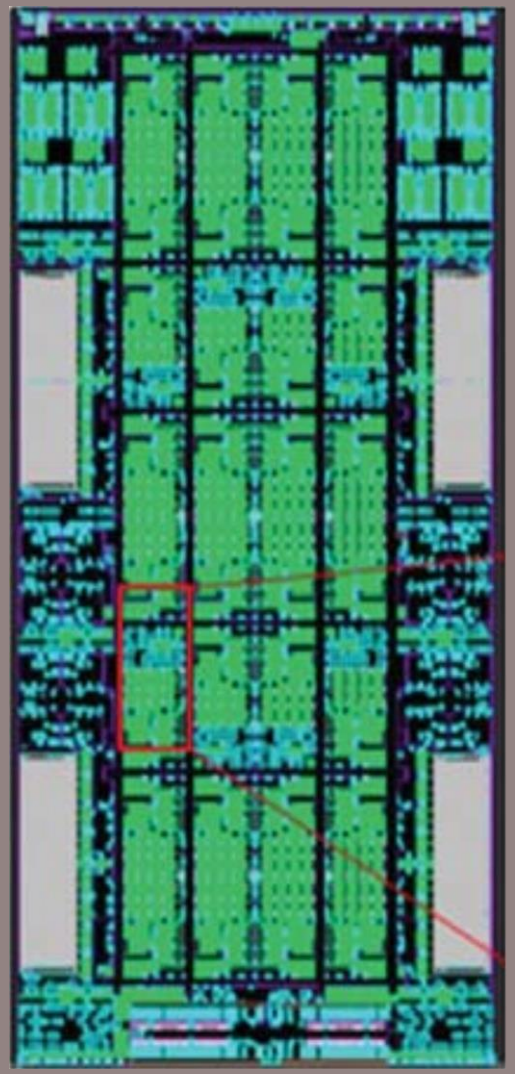
Ascend 910C NPU Core

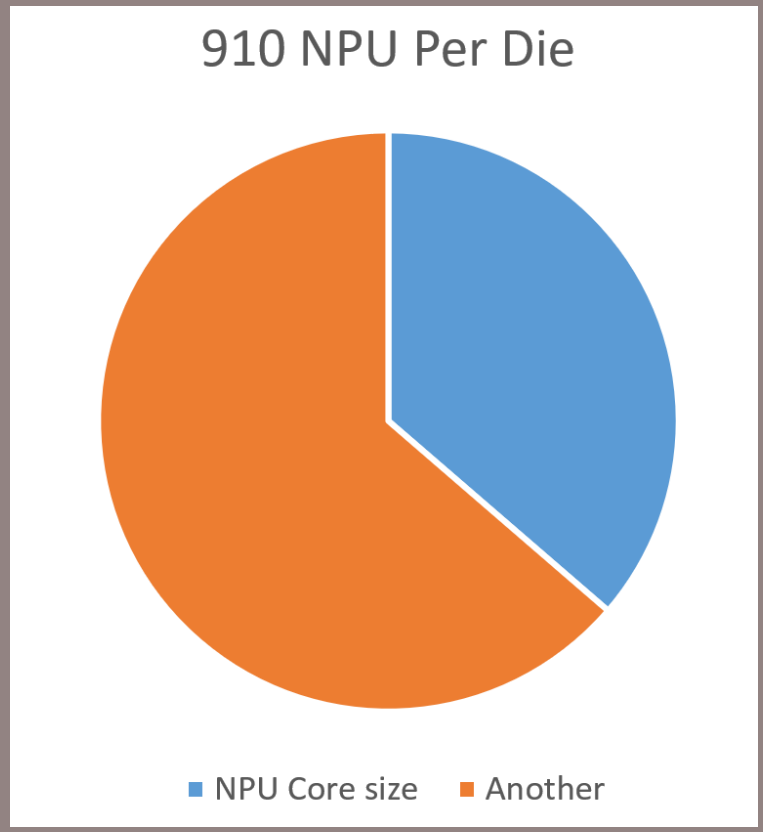




NPU Core number: 25
NPU all size: 162.75mm2
NPU Size per die: 24.45%

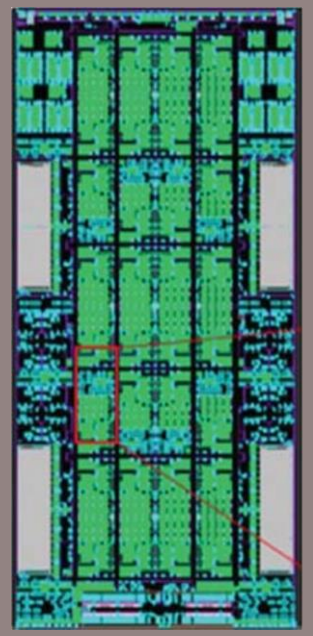
Ascend 910 NPU Core

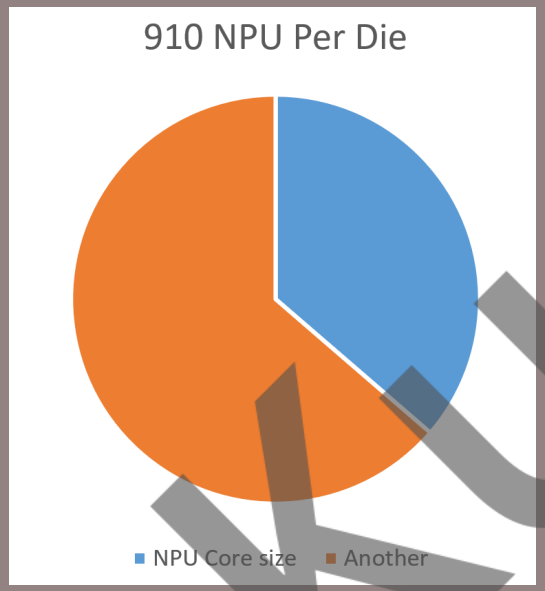


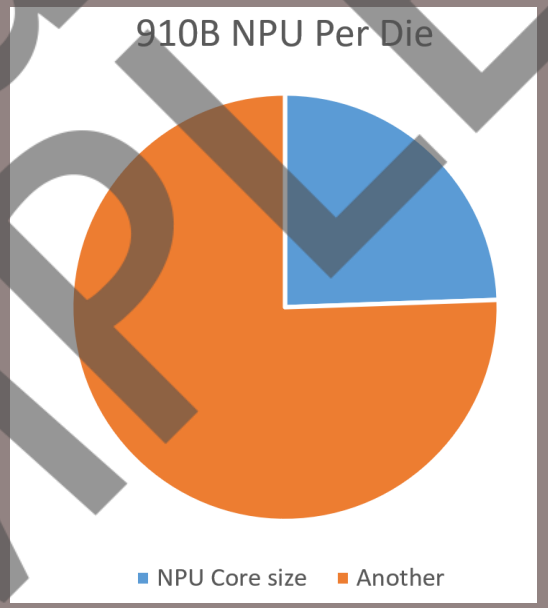


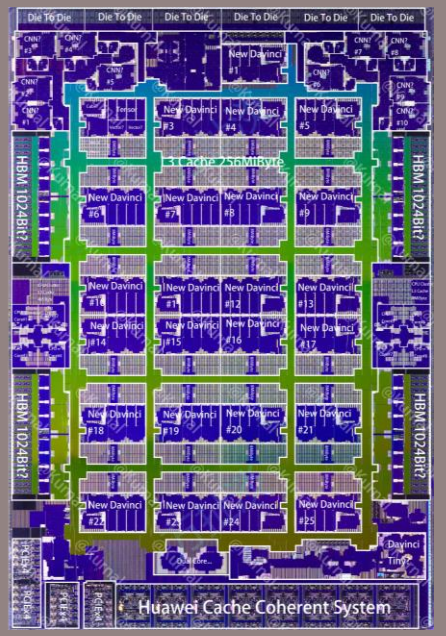
NPU Core number: 32
NPU all size: 165.76mm2
NPU Size per die: 36.33%

Ascend 910 NPU Core







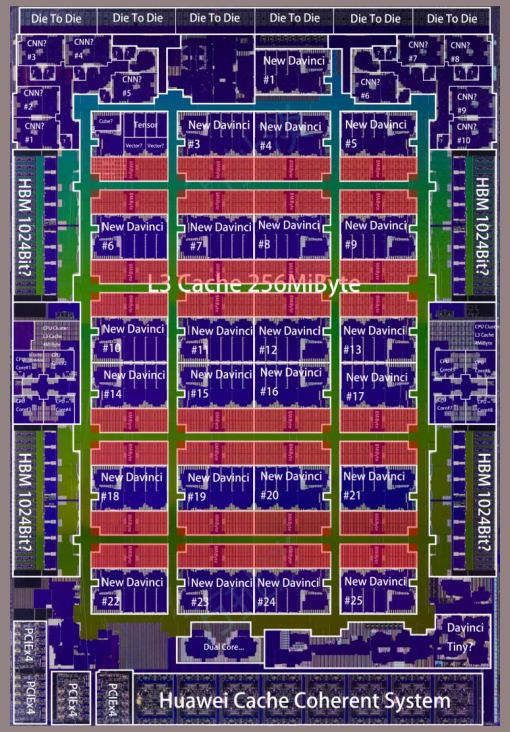


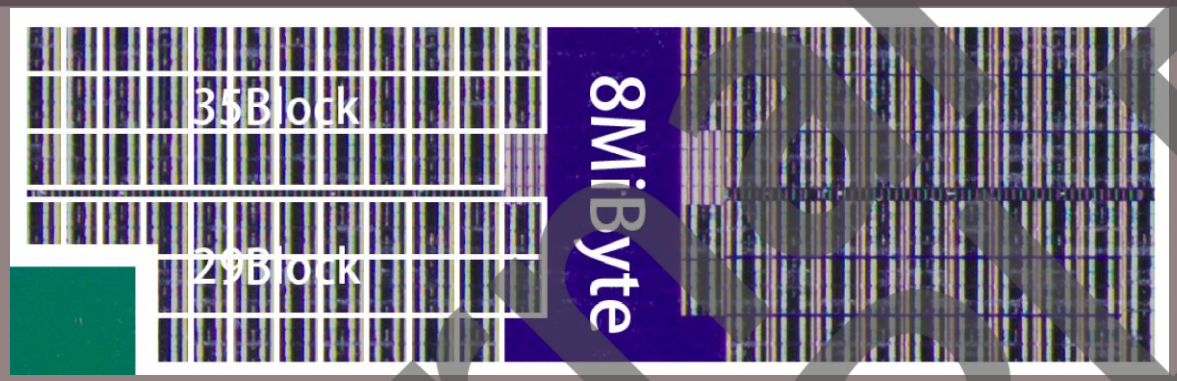
NPU Core number: 32
NPU all size: 165.76mm2
NPU Size per die: 36.33%

The 910C has fewer NPU cores
and the total NPU area remains almost the same
but the NPU occupies less area of the entire die

NPU Core number: 25
NPU all size: 162.75mm2
NPU Size per die: 24.45%

NPU L3





8MiB Cache size： 3.25mm2

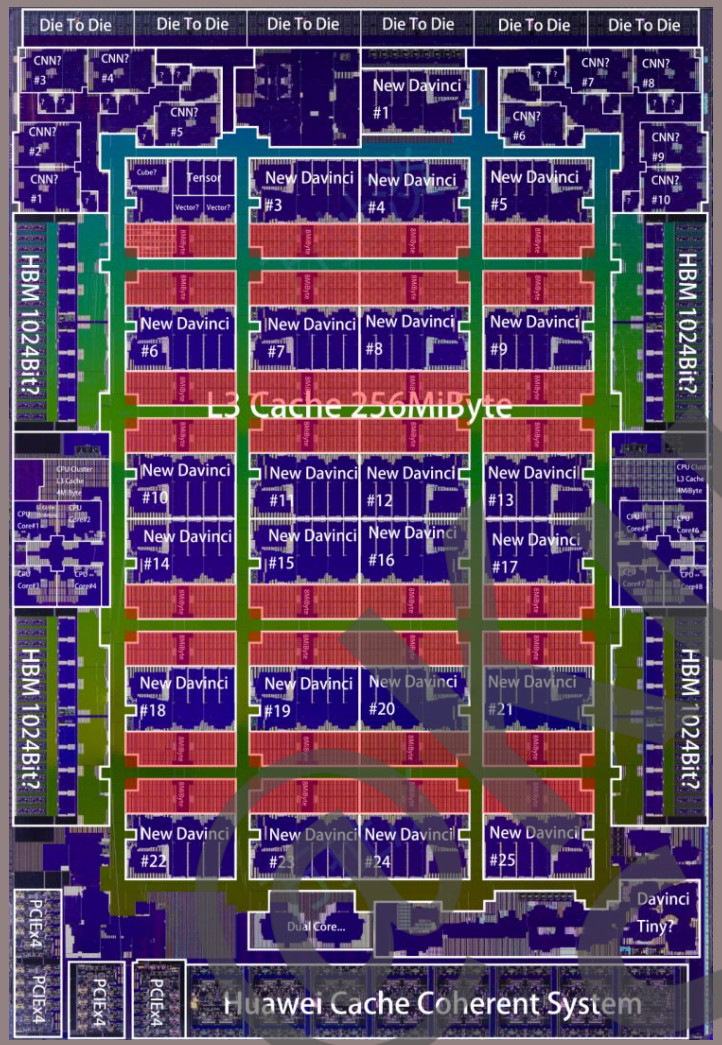
Have 32x8MiB

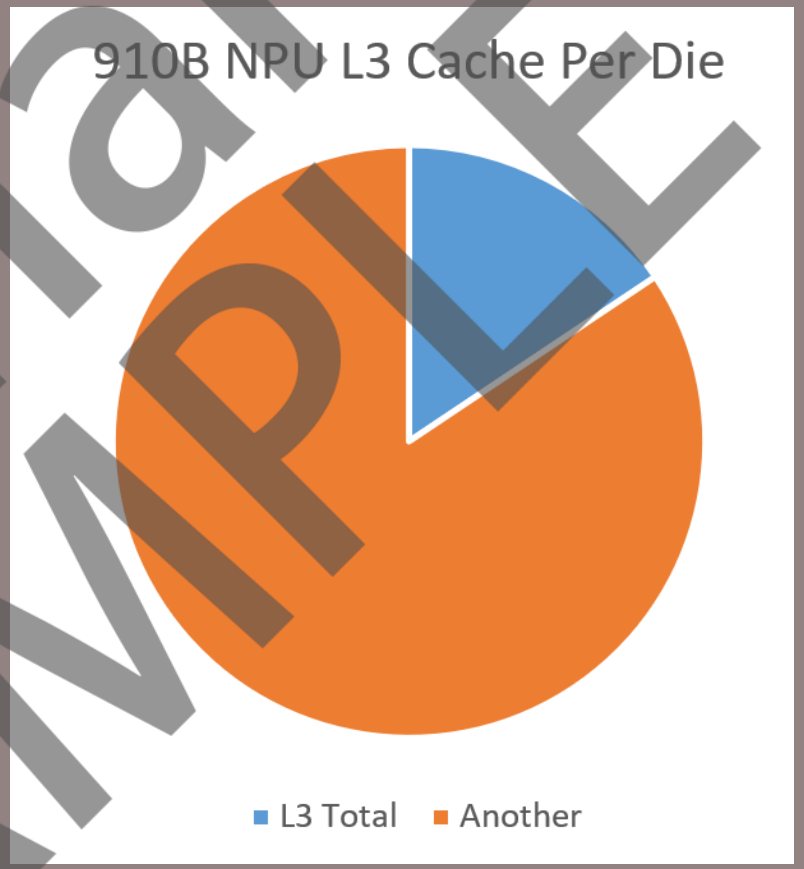
8MiB Cache have 128Block cache

Cache Density： 3200 KiB/mm2
0.32mm2/MiB

1Block(64KiB) cache=0.02mm2

NPU L3



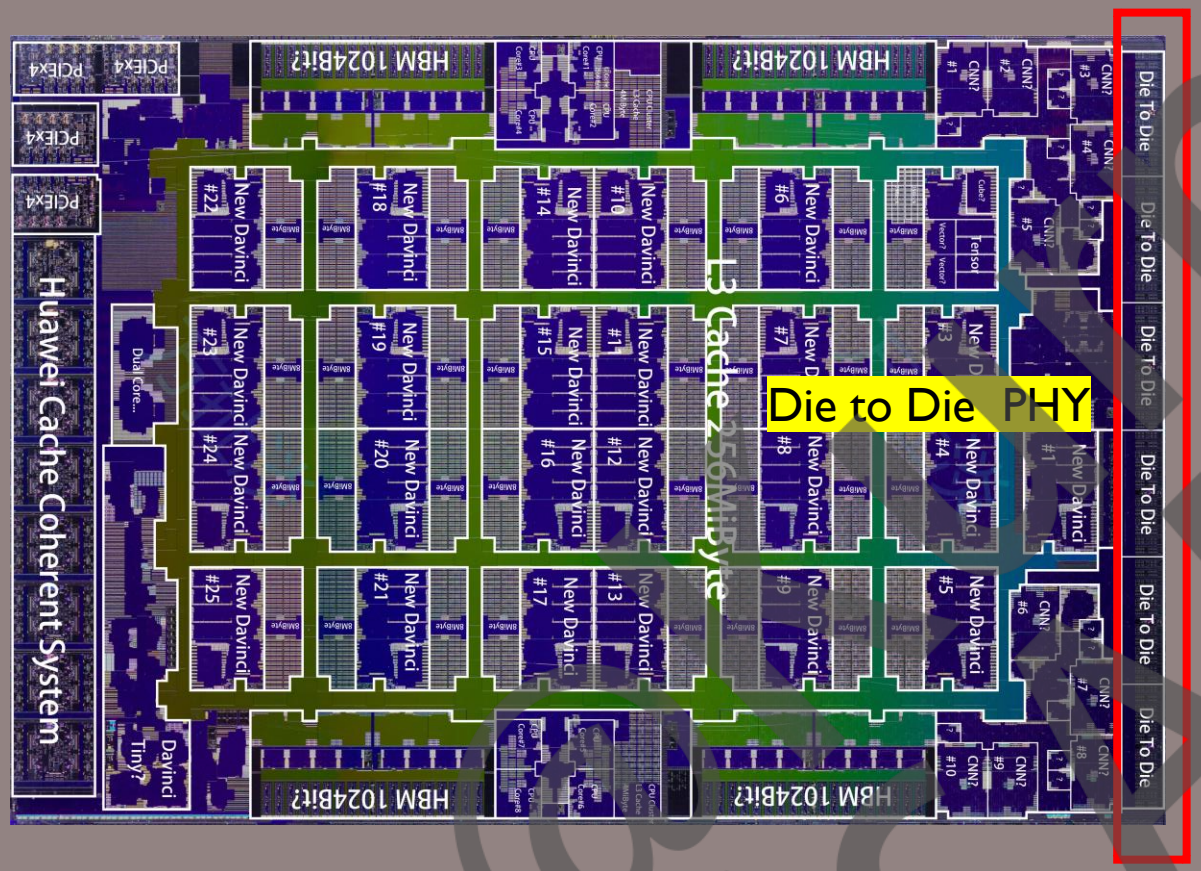


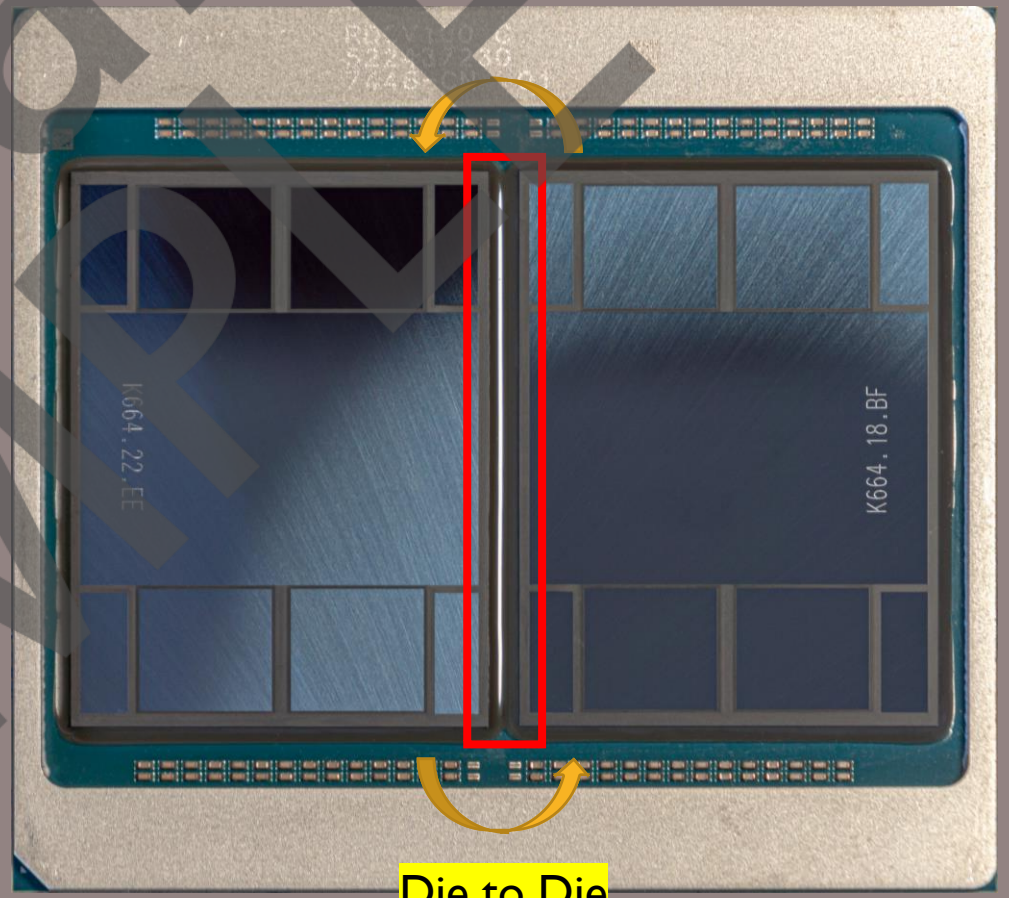
256MiB Cache size	104mm2
256MiB Cache Per Die	15.624%

Die to Die

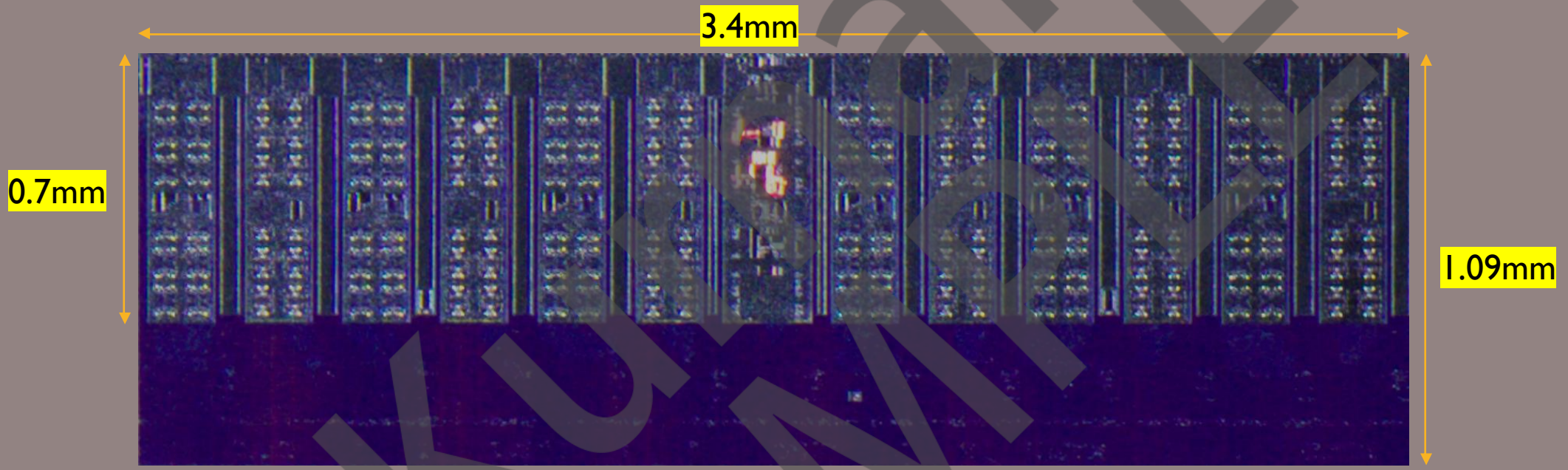
Ascend 910C

Die to Die PHY



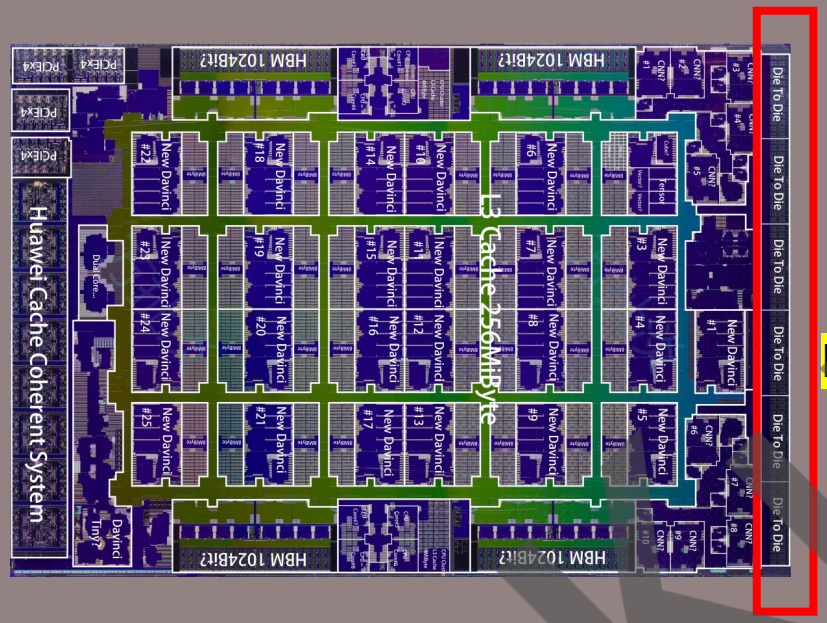


Die to Die PHY



1 Channel D2D PHY size: 3.706mm2

Die to Die PHY

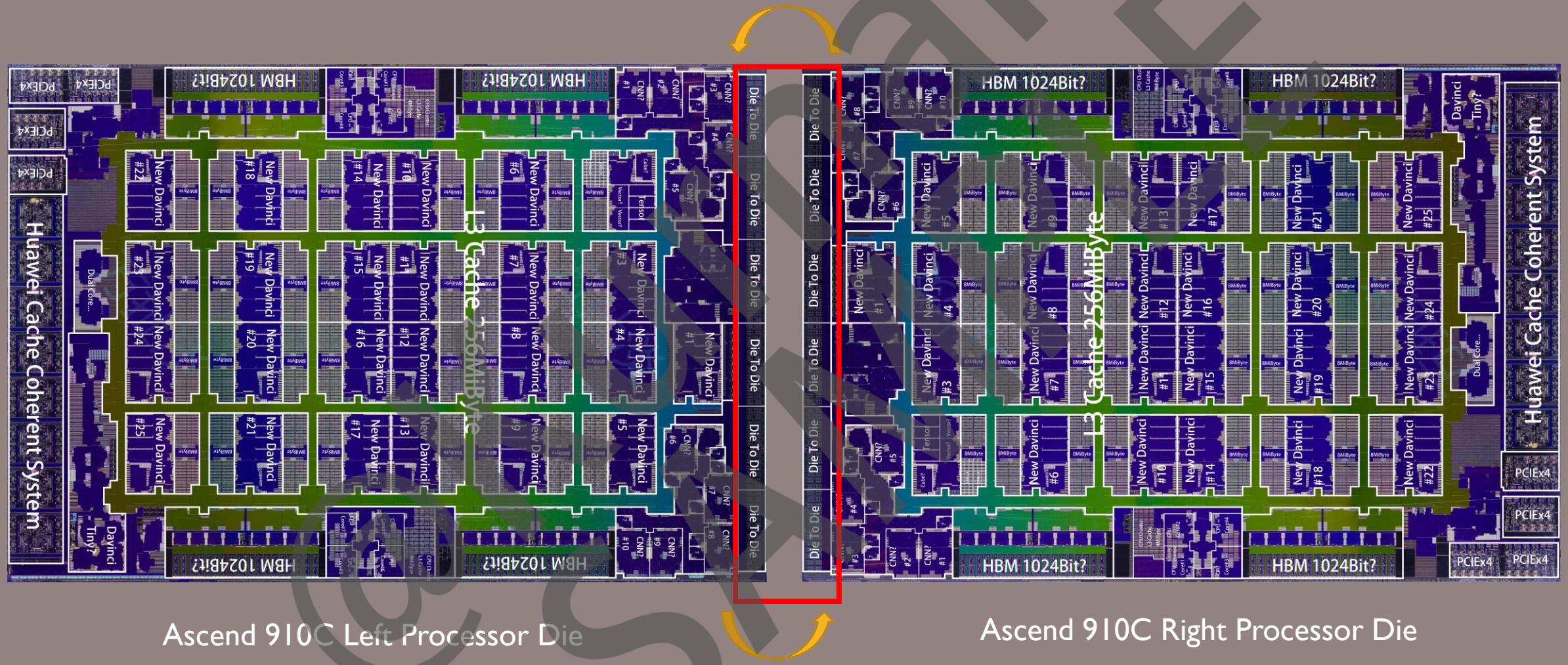


Die to Die PHY

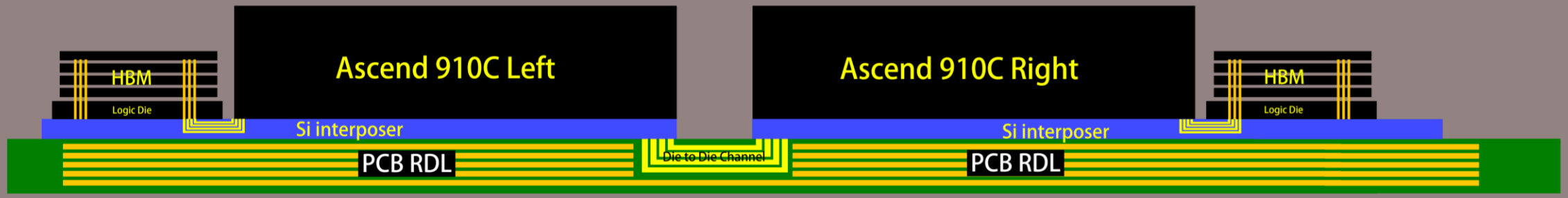
Total Have 6 Channel D2D PHY

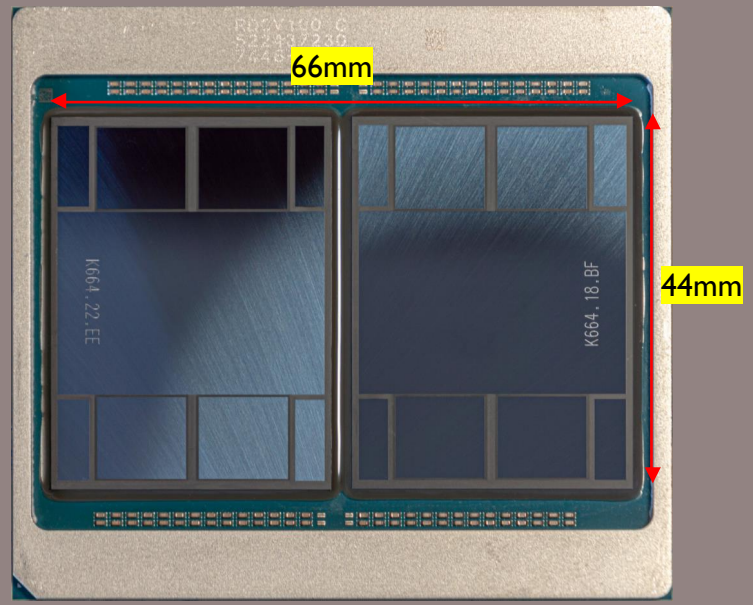
Total D2D PHY size: 22.236mm2

Die to Die PHY



Die to Die PHY



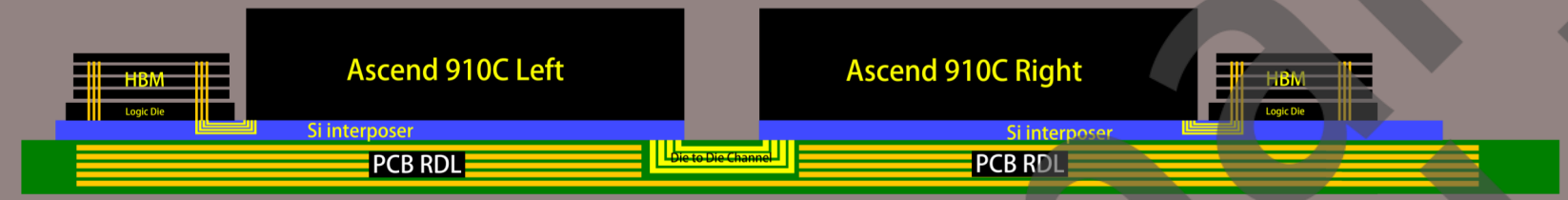


The Die to Die used Sub RDL(like info oS)
But the each chip used the Si interposer to Linked HBM

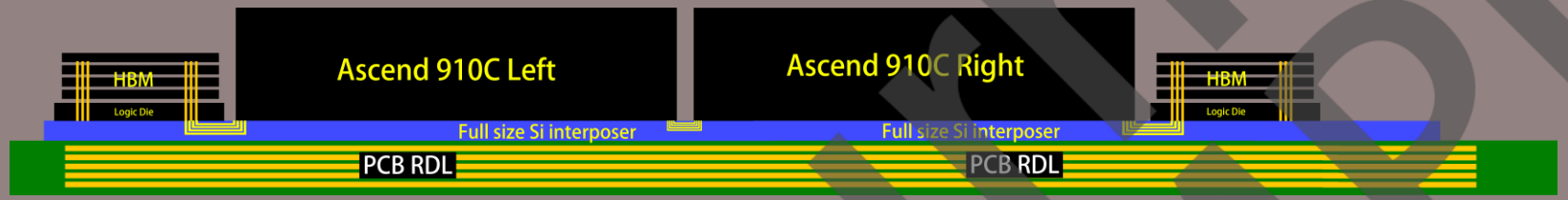
Any way, for I think
Ascend 910C used like CoWoS

And By "Chip Last"

Die to Die PHY



Now(Ascend 910C)



X(New Ascend 910C)

If those used TSV, maybe in the future
New Ascend 910C will used the Local Si Lnterconnect

And 910C/D Will not used the Full size Interposer
If used Full size Si interposer
the interposer size will be 44mm x 66mm
It will need 4x field or 6x Field (Toooo expensive)