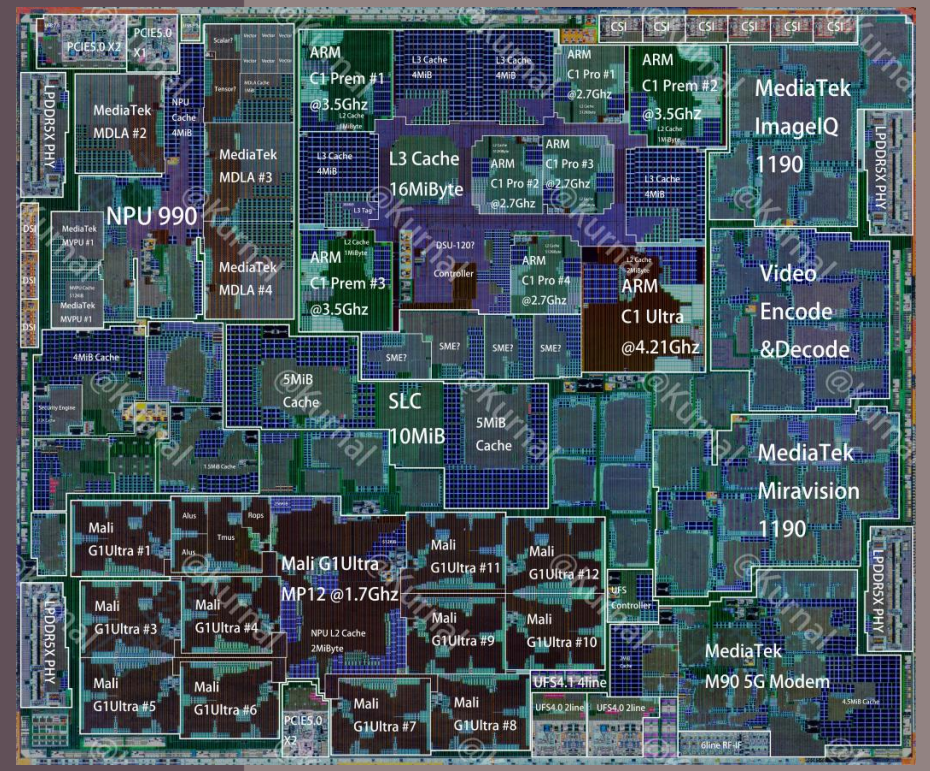
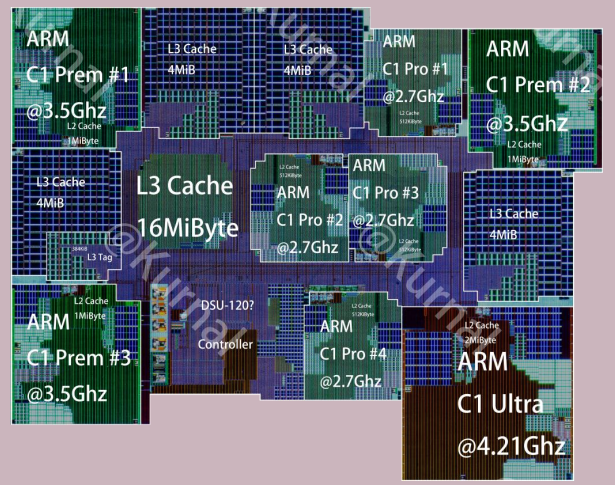
MediaTek Dimensity 9500

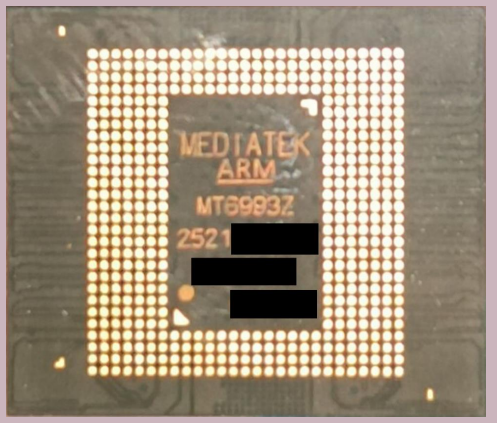
Chip analyze

V1

@Kurnal







Verison of this Report

Version	Date	Updates	Anthor
V0	2025/11/8 16:19	Working	Kurnal
V0.1	2025/11/24 18:32	Finish C1 Ultra	Kurnal
V1	2025/12/1 01:38	Finish all	Kurnal

This Report is made From @Kurnal

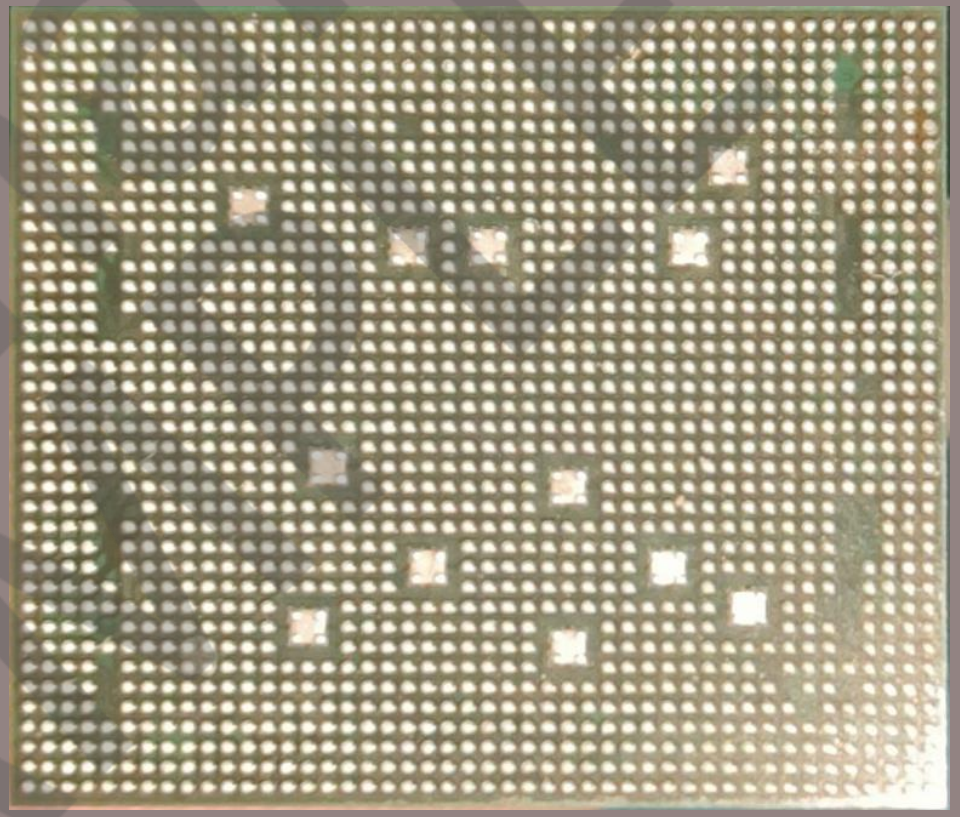
BiliBili: @Kurnal
X: @Kurnalsalts
WeChat: KurnalWeChat

Package analyze

MediaTek Dimensity 9500

Package analyze

Package Frontside



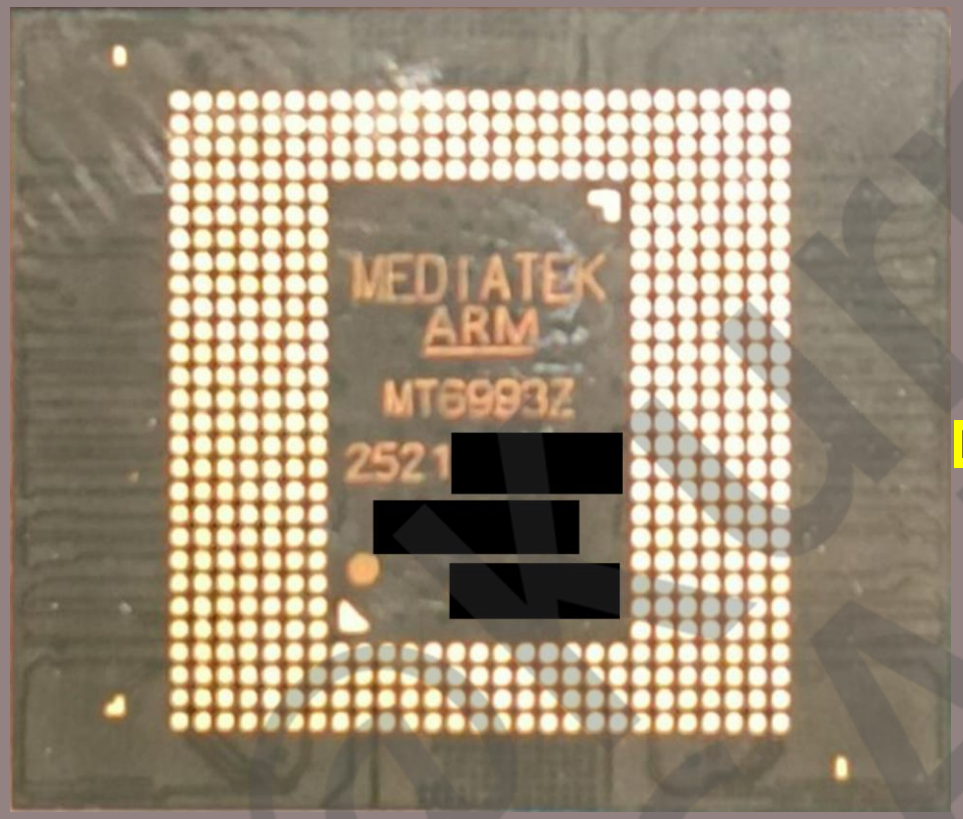
Package Backside

Package Frontside

MEDIATEK
ARM
MT6993Z
2521XXXXXX
XXXXXXX
XXXXXX

Part number
Made/Package in 2025 week 21
Random code
Function code
Trace code

Package analyze



Package Frontside

Package Type:	HB MUFPOP
Package size:	16.40mm x 14.00mm
Package thickness:	0.455mm
Ball Pitch:	0.35mm

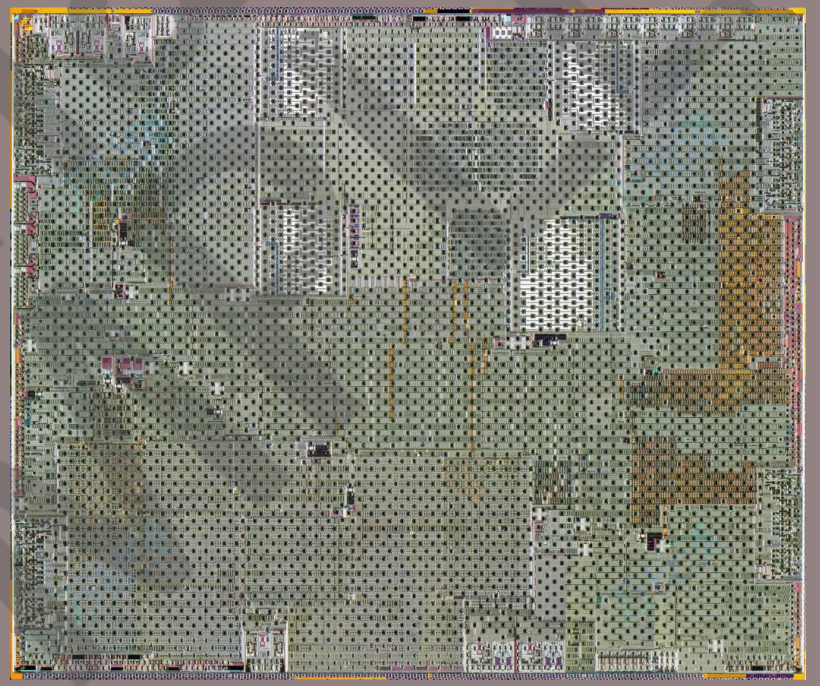
Decaped

MediaTek Dimensity 9500

Chip analyze

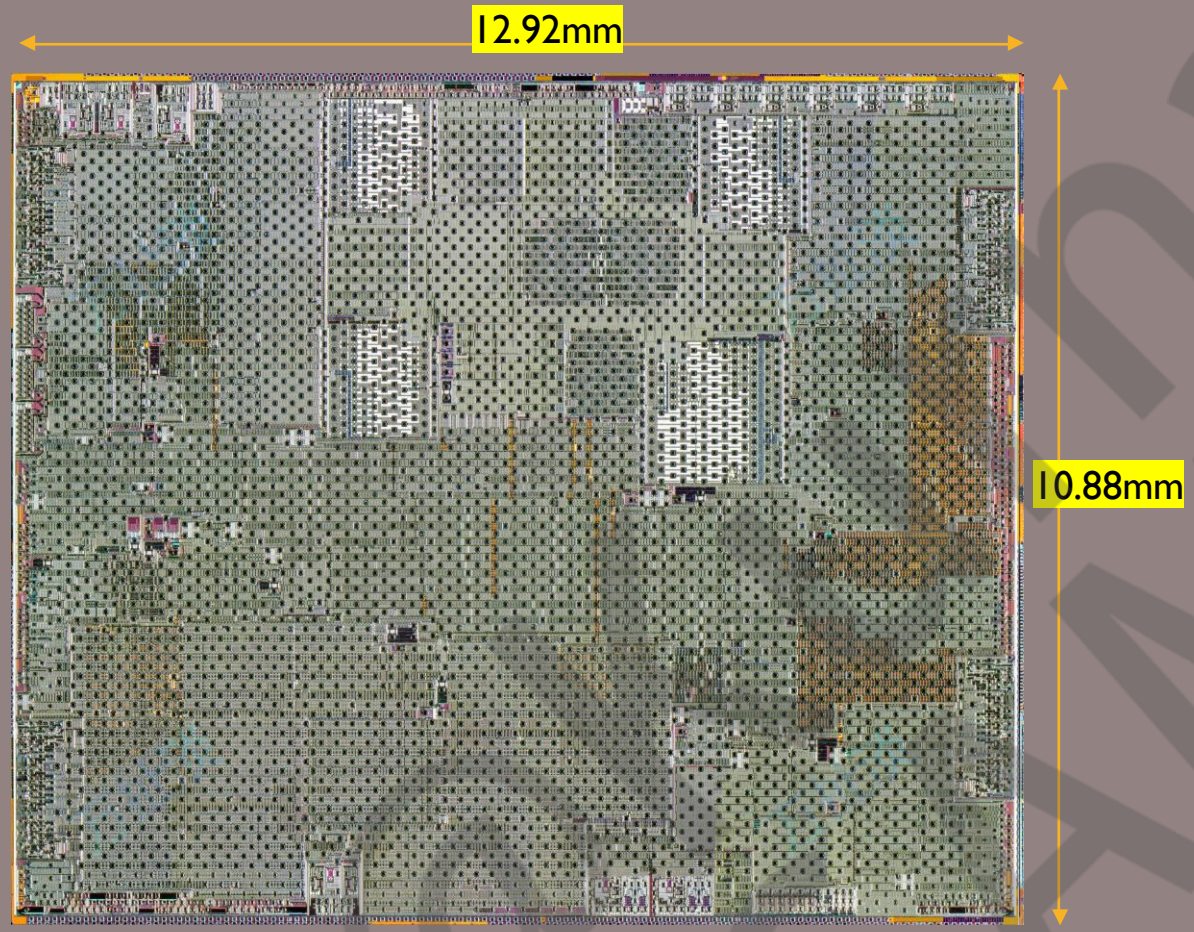
Package Frontside

Decaped



Metal Layers Pics

Chip analyze



Metal Layers Pics

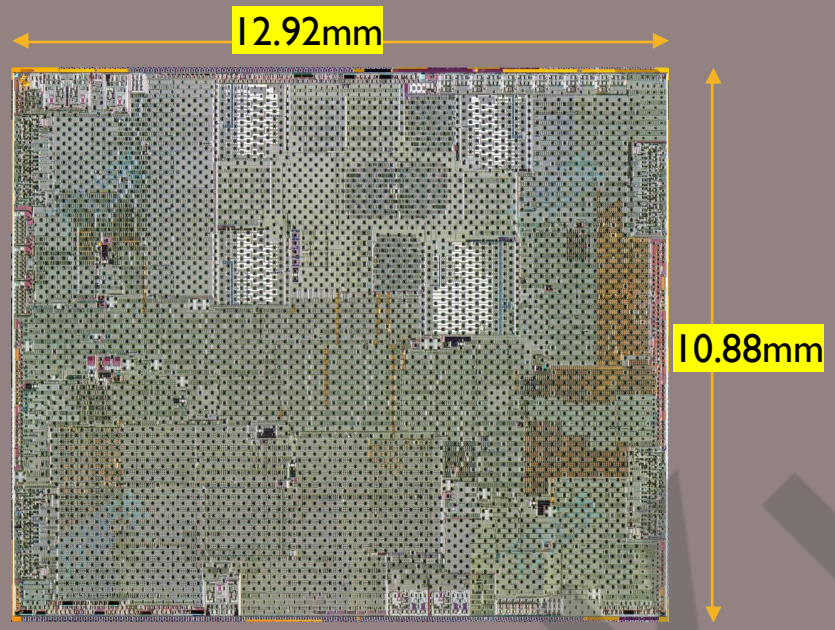
Die size: 140.57mm2
Die Thickness: 200um

Die Mark : 22 FEB 2025 BHJ11471B

Tap Out or Freeze date

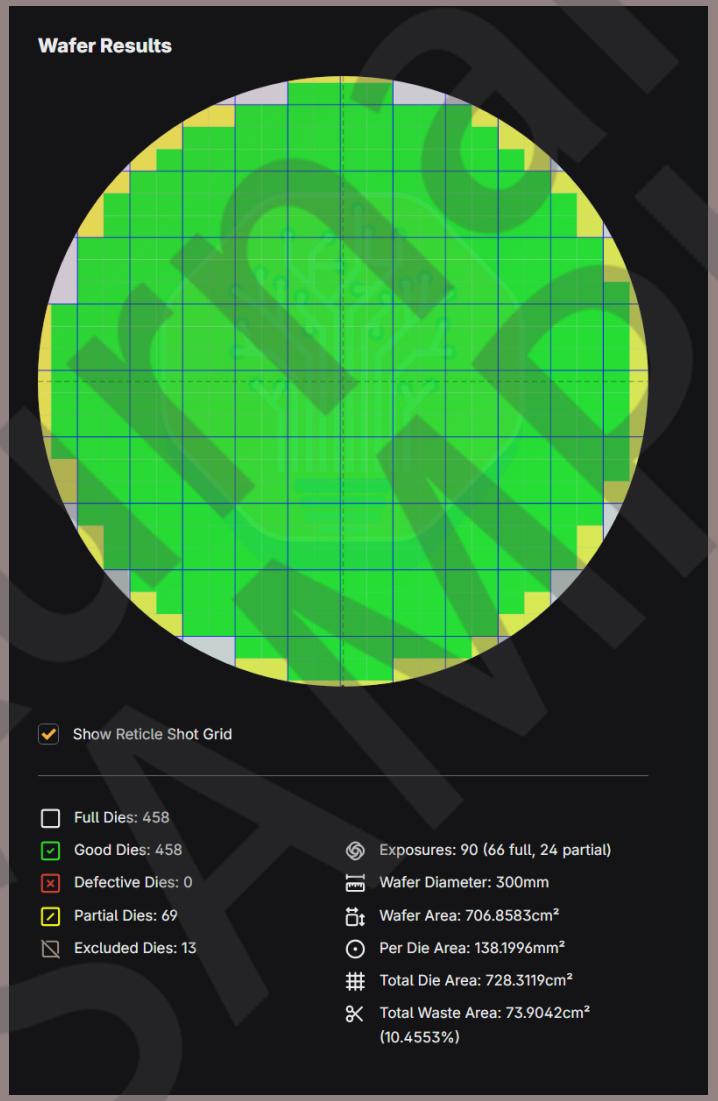
Some Code

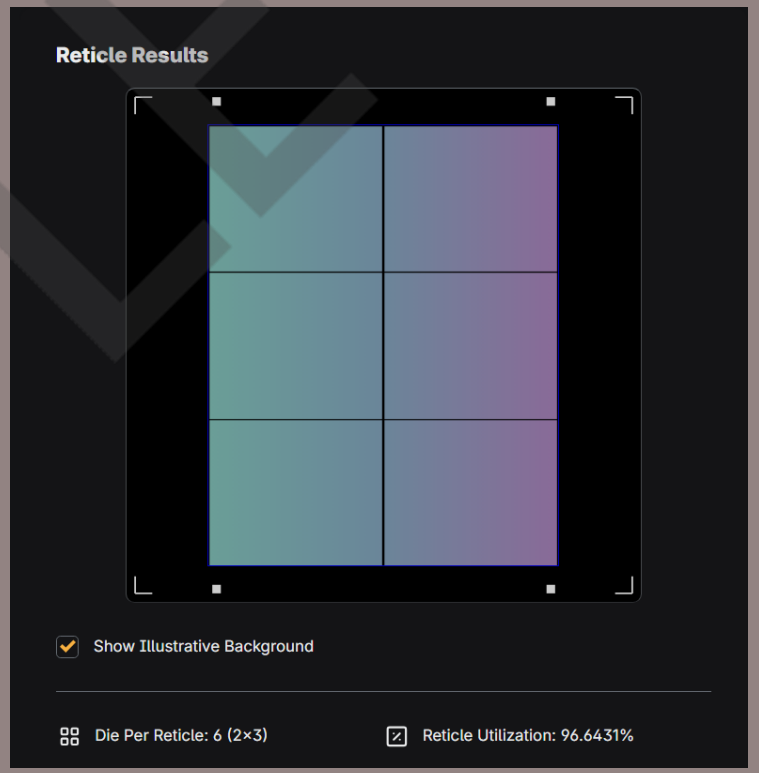
Chip analyze



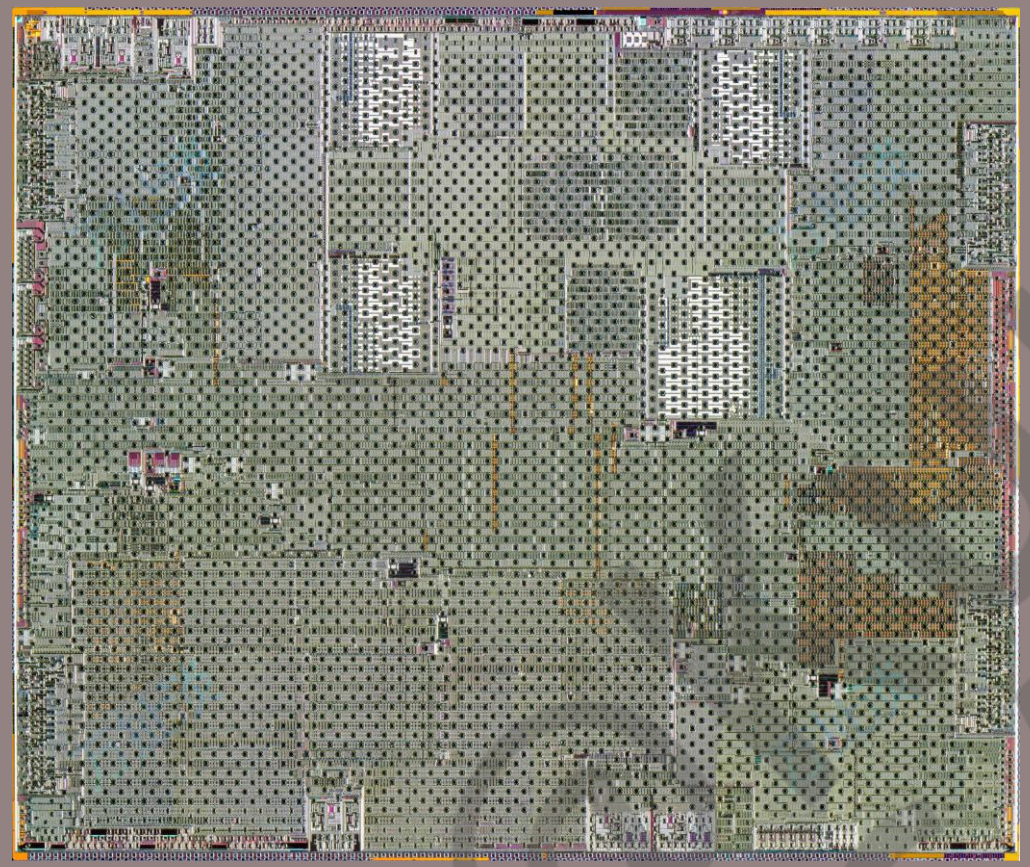
Metal Layers Pics

Die size: 140.57mm2
Die Per Wafer: 458
Die Per Mask: 6:1



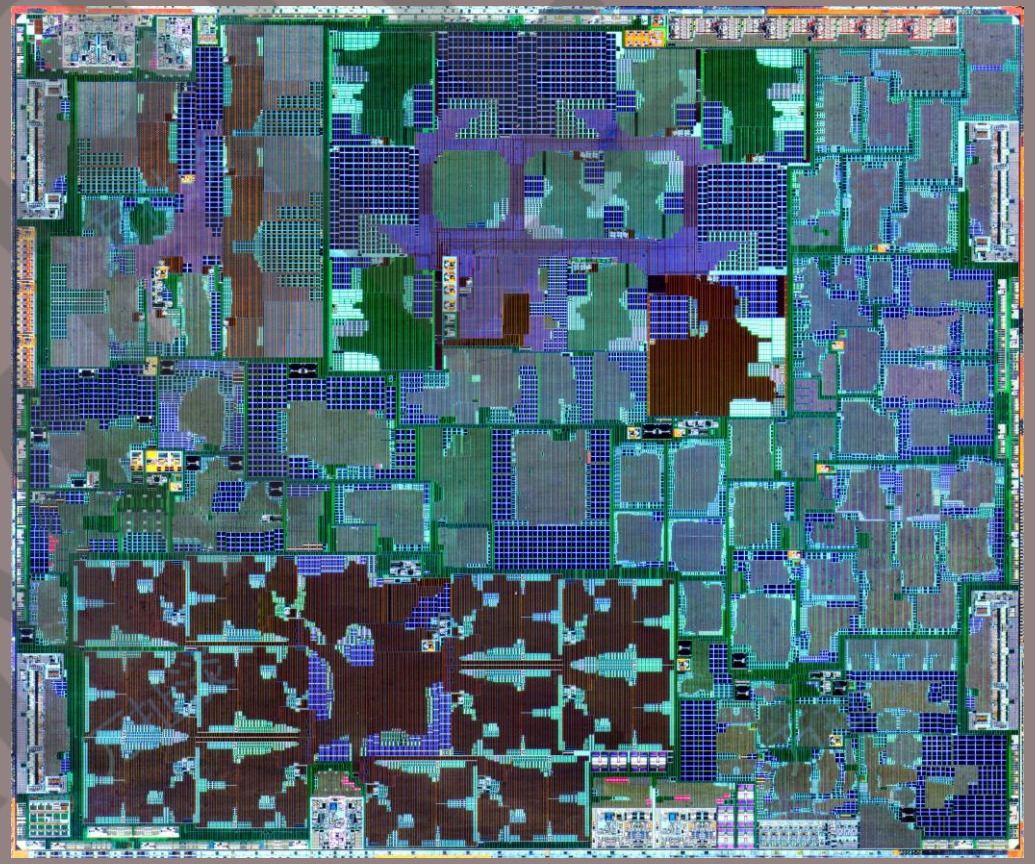


Chip analyze



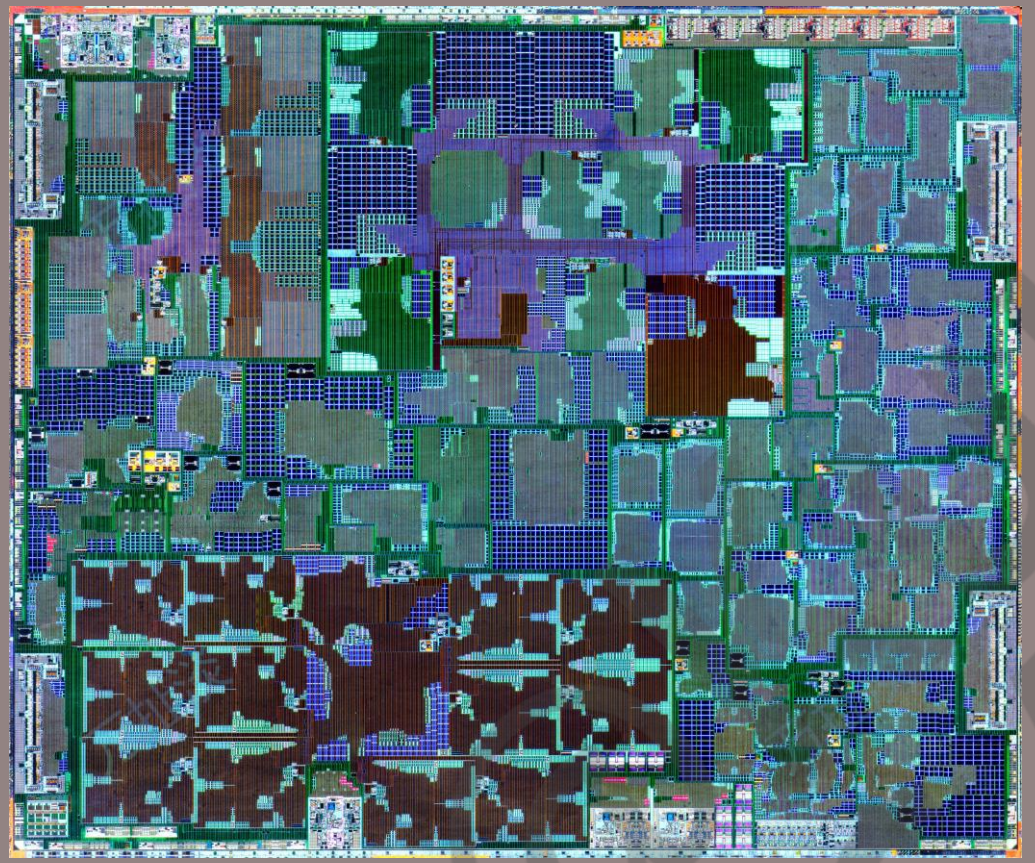
Metal Layers Pics

Delayer



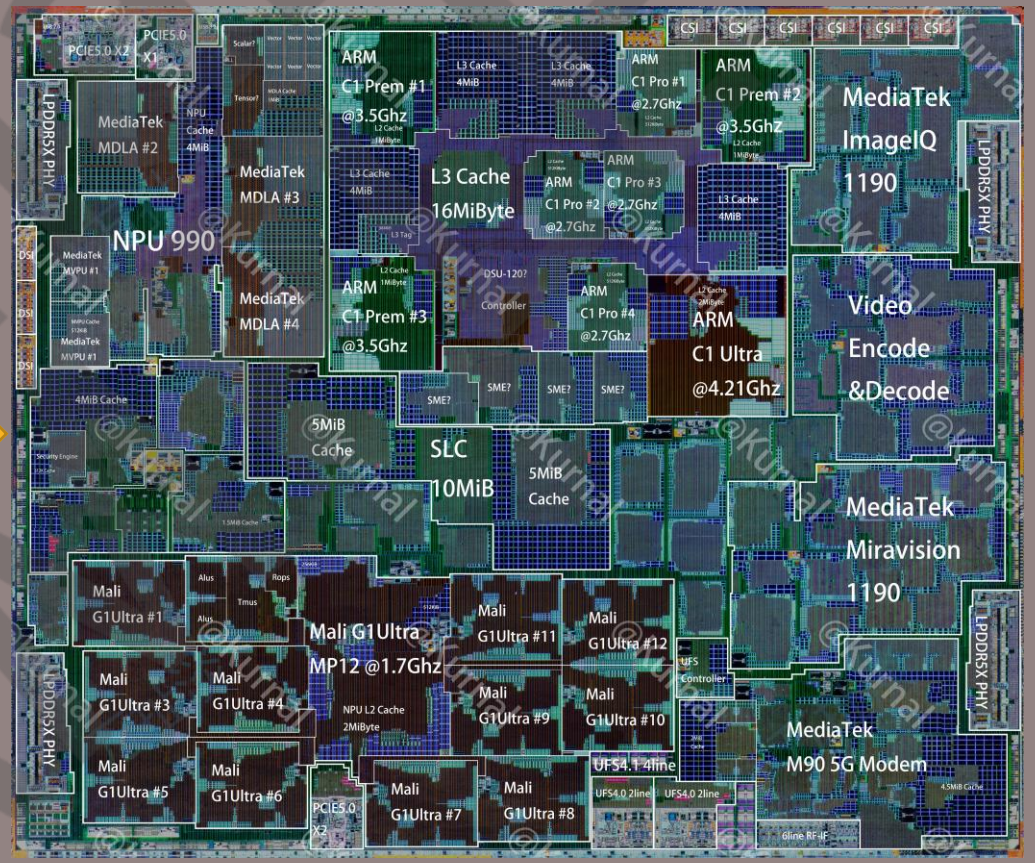
Die Shot

Chip analyze



Die Shot

Layout

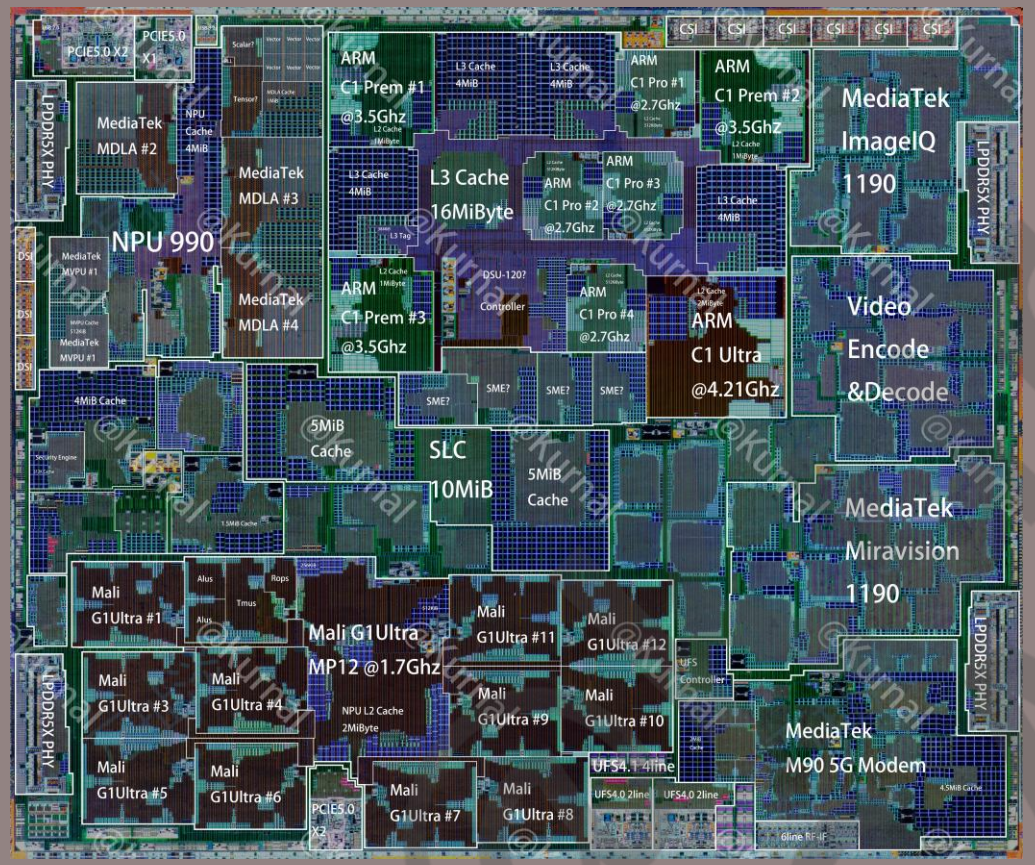


Die Shot

Transister number

MediaTek Dimensity 9500

Transister number

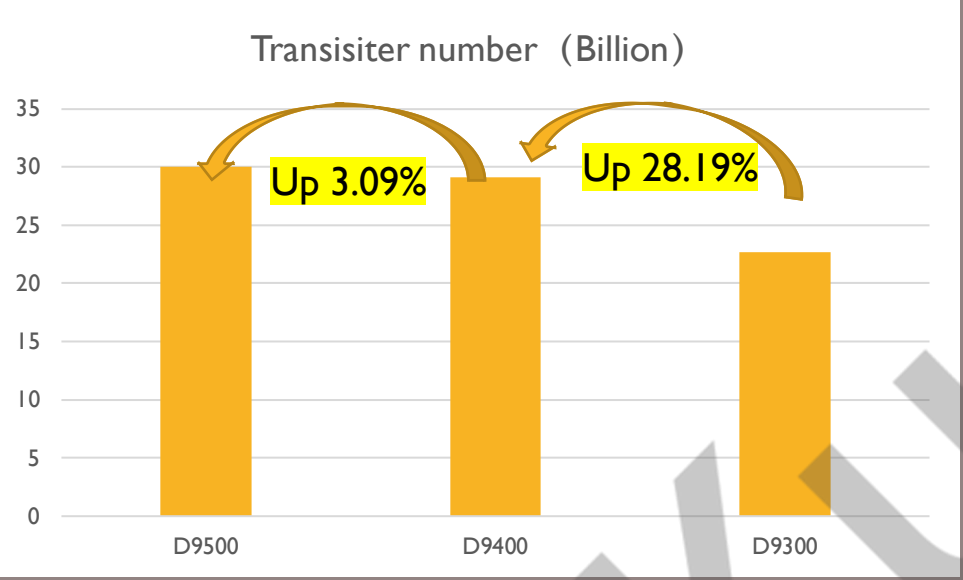


Die Shot

Chip Technology : TSMC N3P

Transister Number : 30Billion ?

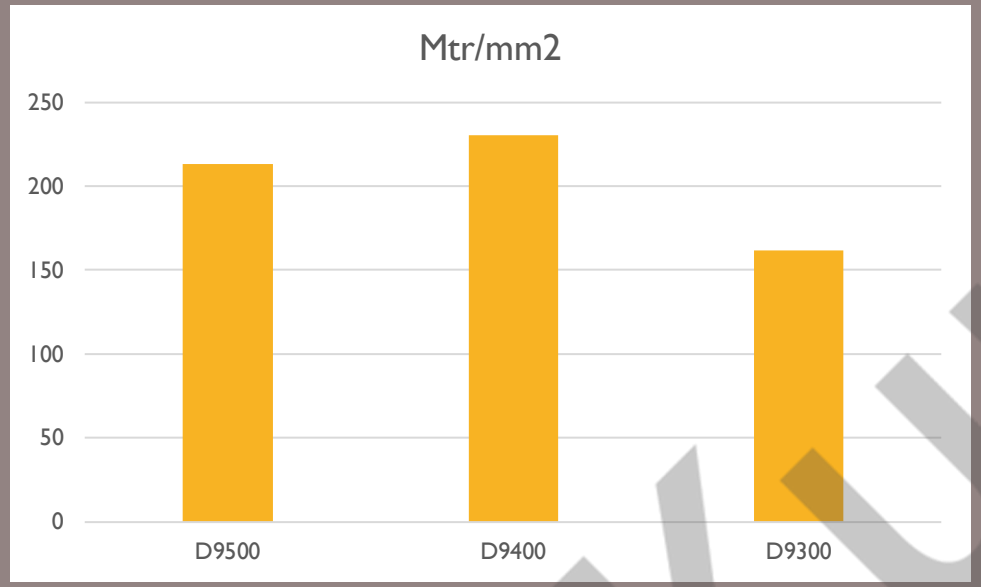
Transister number



	Transisiter number
D9500	30 Billion
D9400	29.1 Billion
D9300	22.7 Billion

The Dimensity 9500 has only 3.09% more transistors than the Dimensity 9400.

Transister number



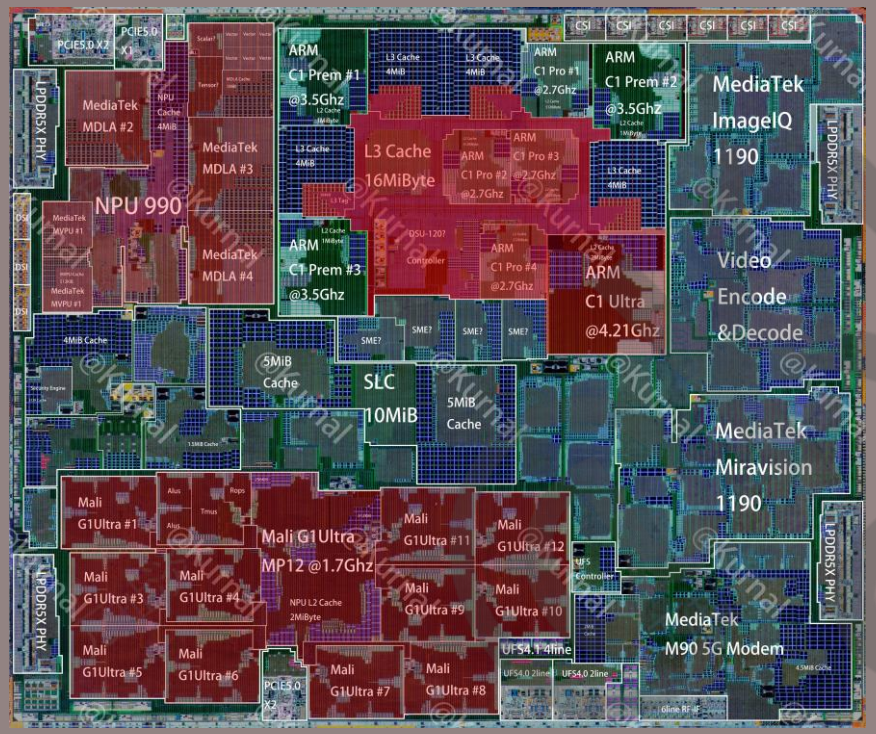
TSMC N3	2-1 Ultra HD lib	2-2 HD lib	3-2 HP lib
Cell H	143	169	195
Gate Pitch	48	48/54	54
Density	214.7	181.67/161.48	157.44

Clearly, the Dimensity 9400's transistor density last year exceeded the highest density of this process (TSMC N3).

	Million Transister /mm2	
D9500	213.41	TSMC N3
D9400	230.47	
D9300	161.73	TSMC N4

Transister number

TSMC N3	2-1 Ultra HD lib	2-2 HD lib	3-2 HP lib	
Density	214.7	181.67/161.48	157.44	
size	78.375mm2	47.385mm2	non	136.1mm2
Trs Number	16,827	10,486.9	non	27.3Billions



Die Shot

3-2: none

2-2: CPU,NPU,GPU, IO

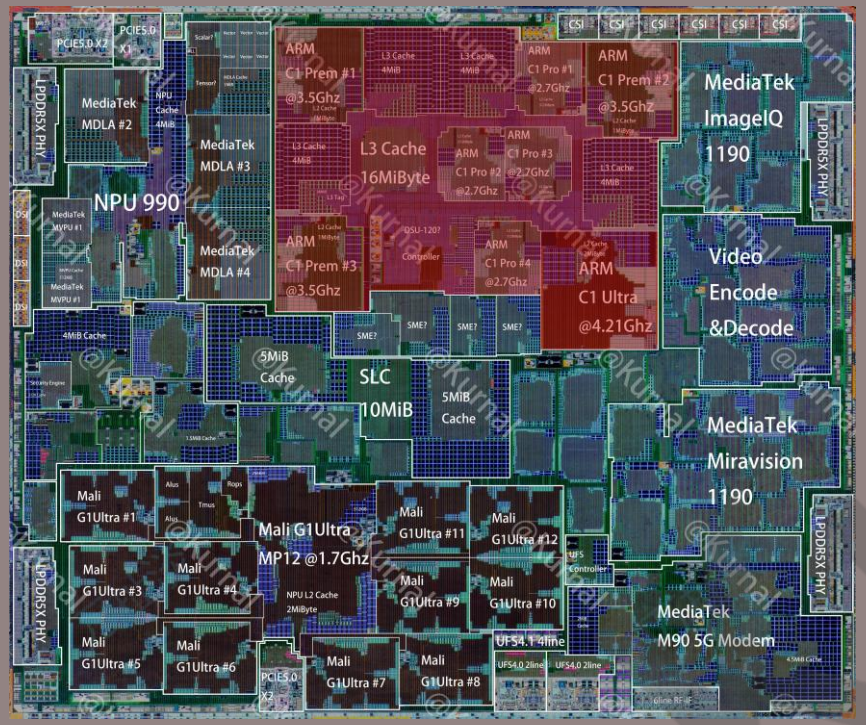
2-1: another side

Calculations suggest that the Dimensity 9500 contains an estimated 27 billion transistors.

On chip analyze-CPU

MediaTek Dimensity 9500

On chip analyze-CPU

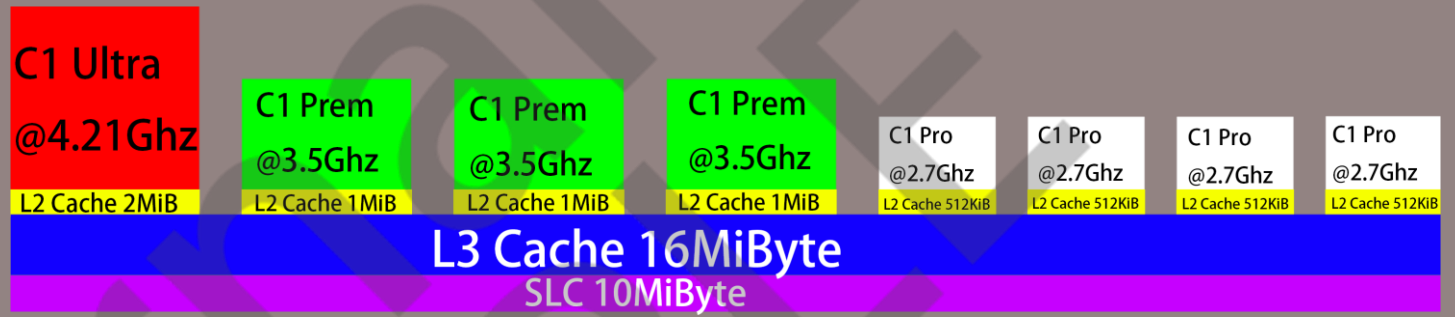


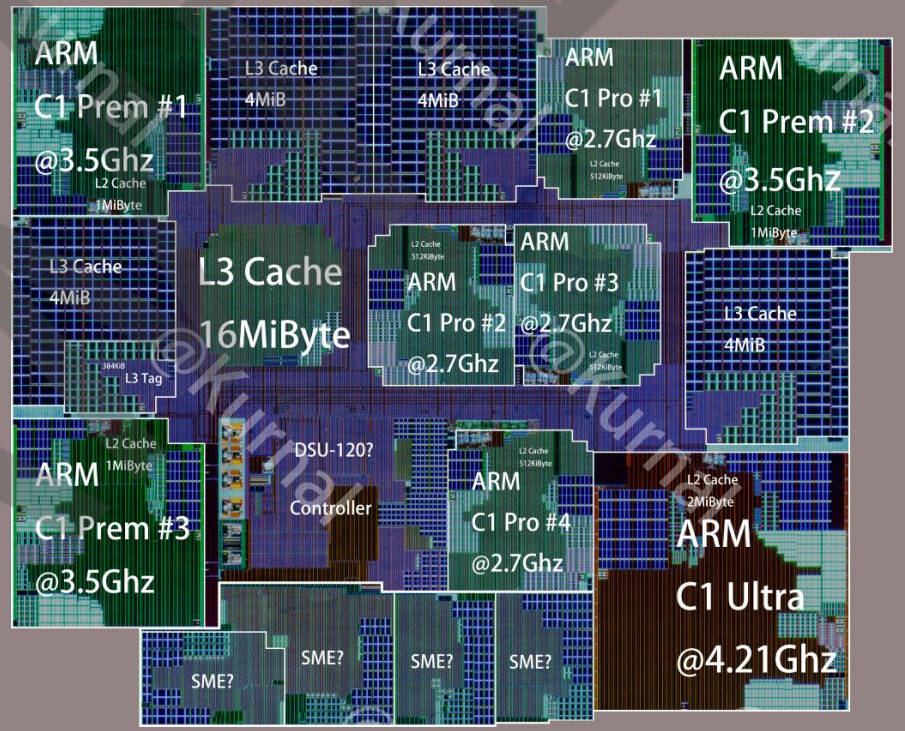
1x C1 Ultra @4.21Ghz L2 2MiB

3x C1 Prem @3.5Ghz L2 1MiB

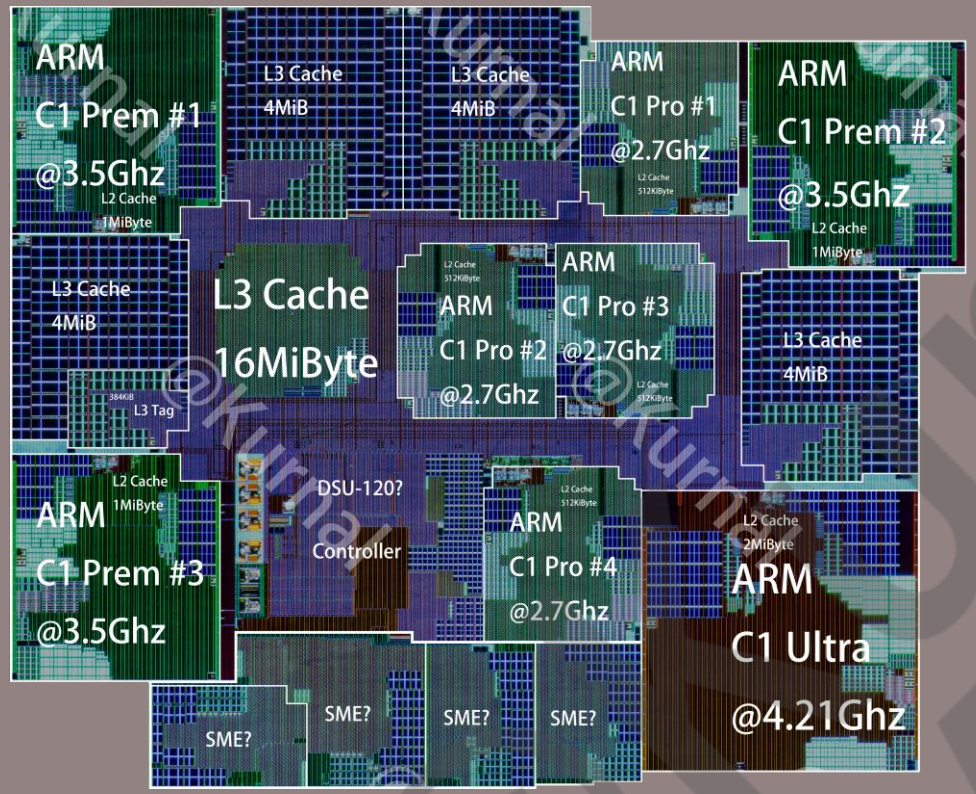
4x C1 Pro @2.7Ghz L2 512KiB

L3 16MiB SLC 10MiB

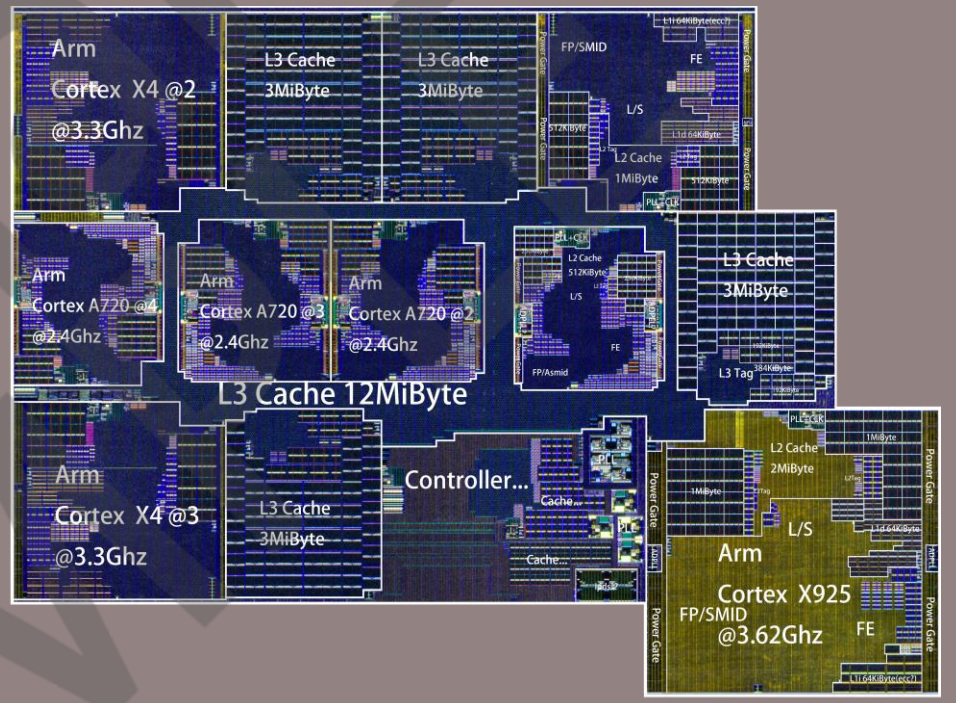




On chip analyze-CPU



D9500 CPU Cluster

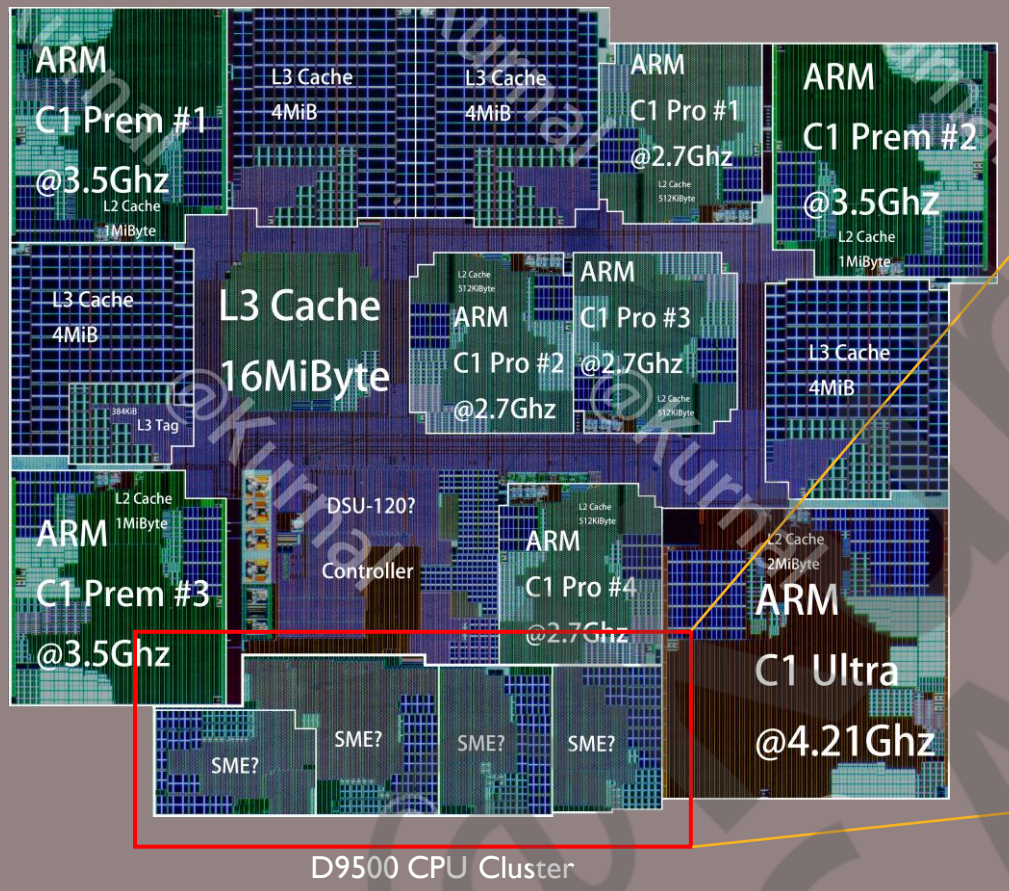


D9400 CPU Cluster

Bigger than 34.22%

CPU Cluster size: 28.75mm2 → CPU Cluster size: 21.42mm2

On chip analyze-CPU



D9500 CPU Cluster

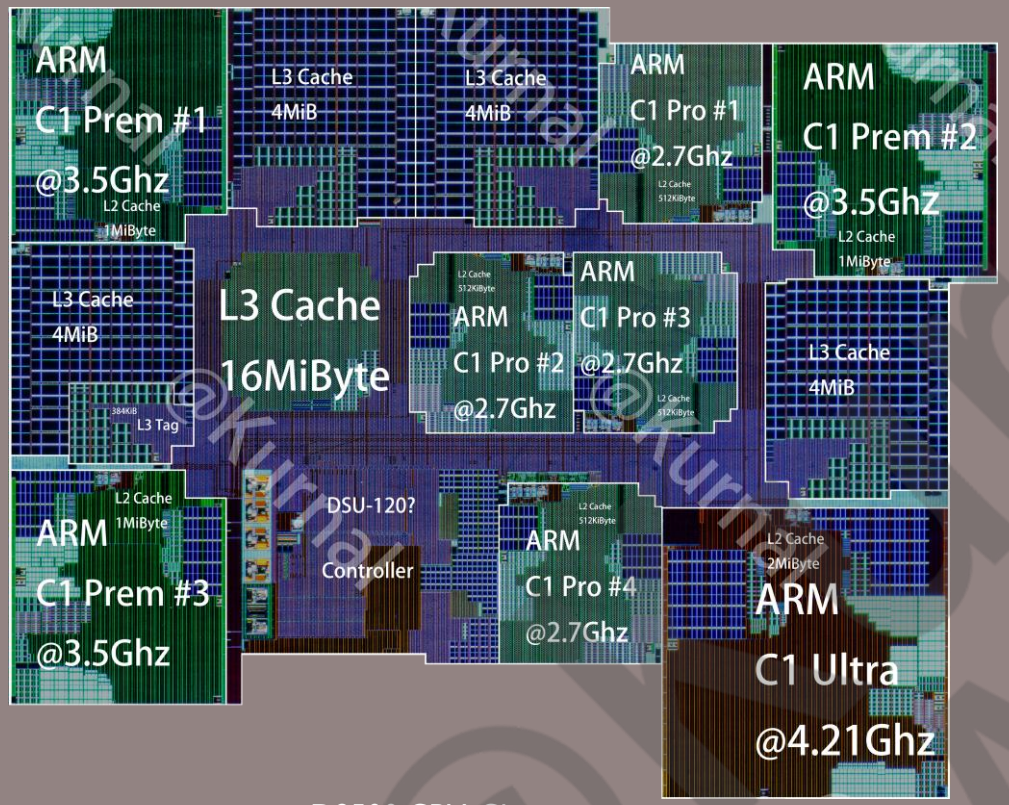
640KiB Cache

4 Core =2.91mm2

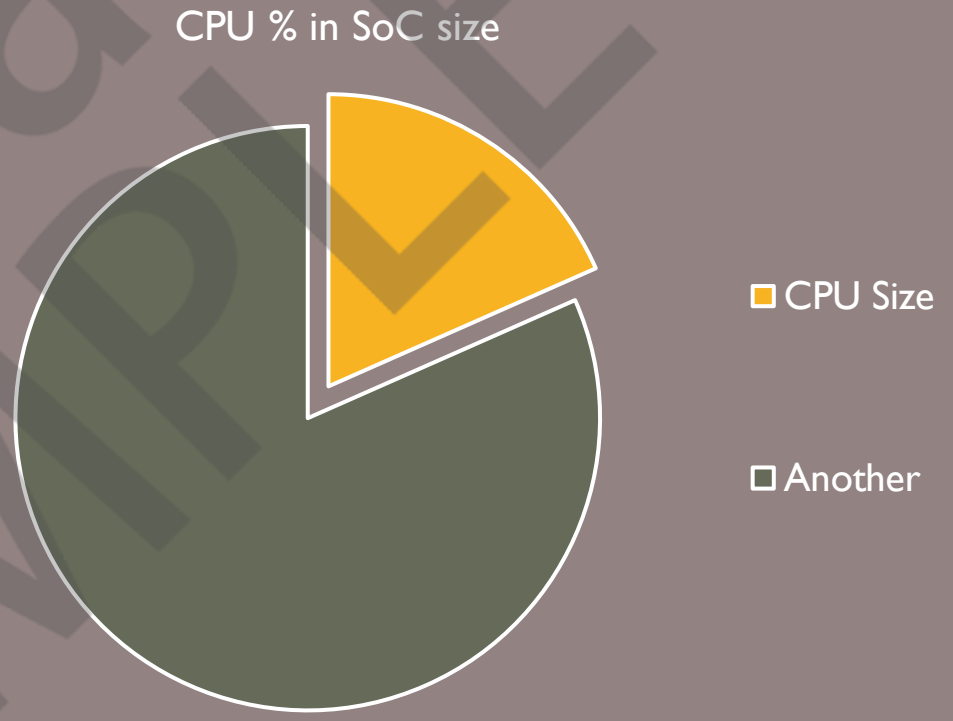
CPU Cluster size: 28.75mm2

Maybe those are SME?

On chip analyze-CPU



D9500 CPU Cluster



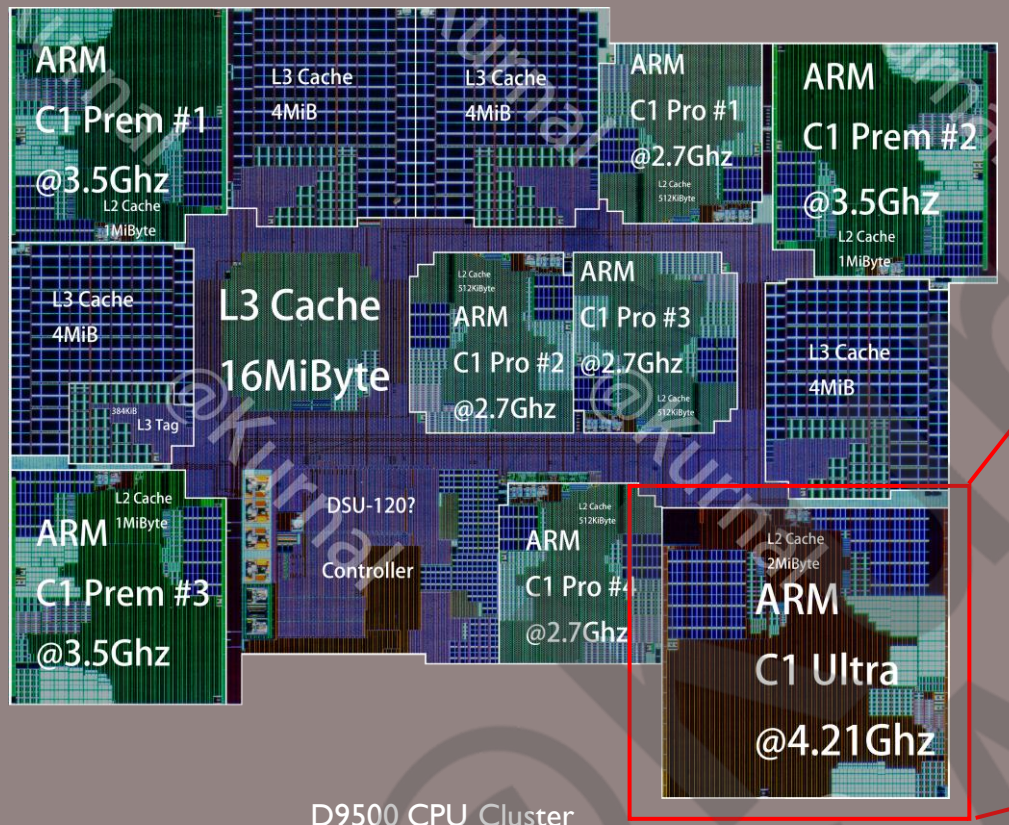
CPU Cluster size: 25.84mm2

CPU Percent in chip: 18.38%

On chip analyze-CPU

C1-Ultra

On chip analyze-CPU

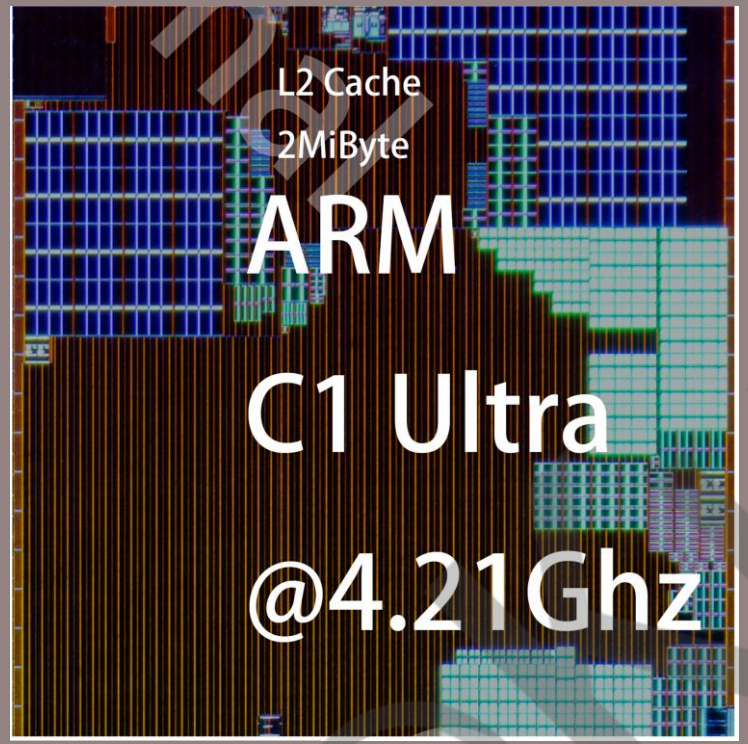


D9500 CPU Cluster

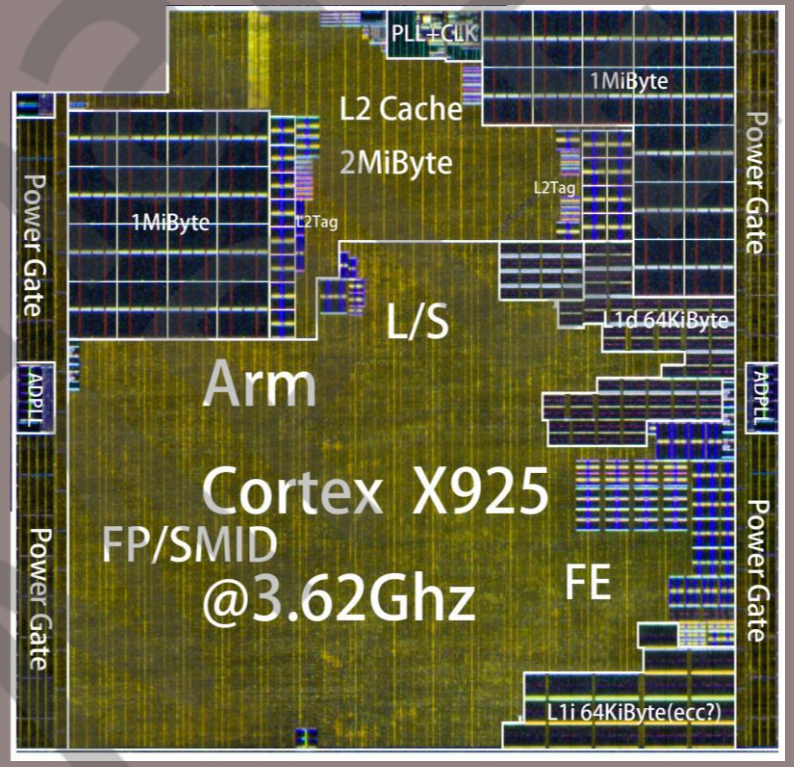
C1 Ultra

Core size:3.259mm2

On chip analyze-CPU



C1 Ultra @D9500



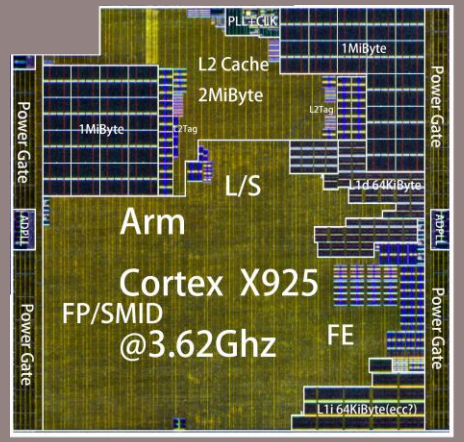
X925 @D9400

Smaller than 2.27%

Core size:3.259mm2

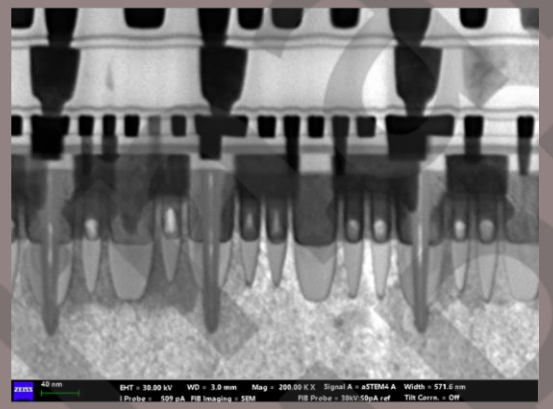
Core size:3.335mm2

On chip analyze-CPU



X925 @D9400

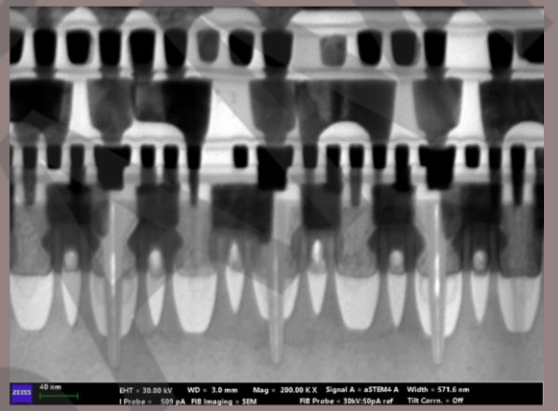
TSMC N3
3-2Fin



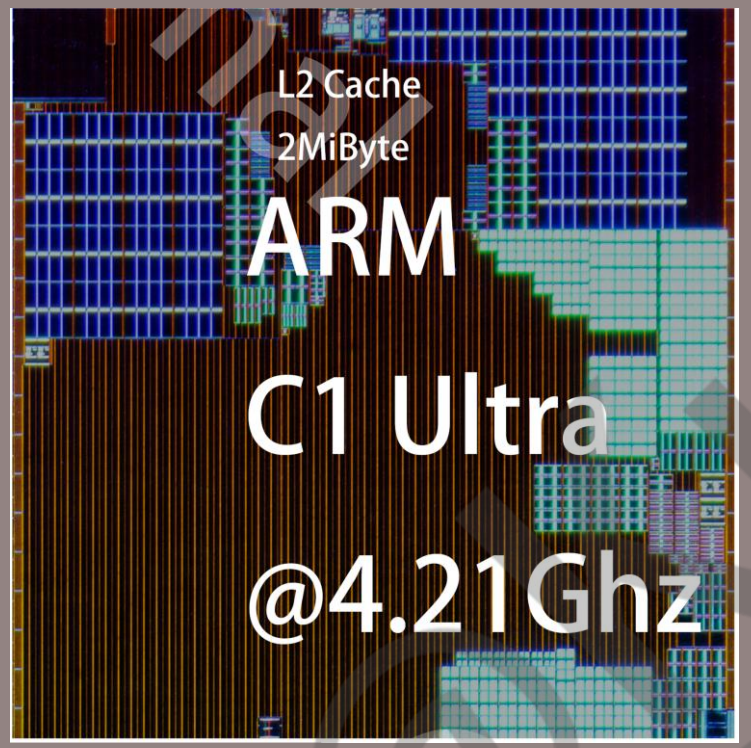
N3E 3-2 Fin
- 0.85X Area
- +33% Speed
- -12% Energy

C1 Ultra @D9500

TSMC N3
2-2Fin



N3E 2-2 Fin
- 0.72X Area
- +23% Speed
- -22% Energy



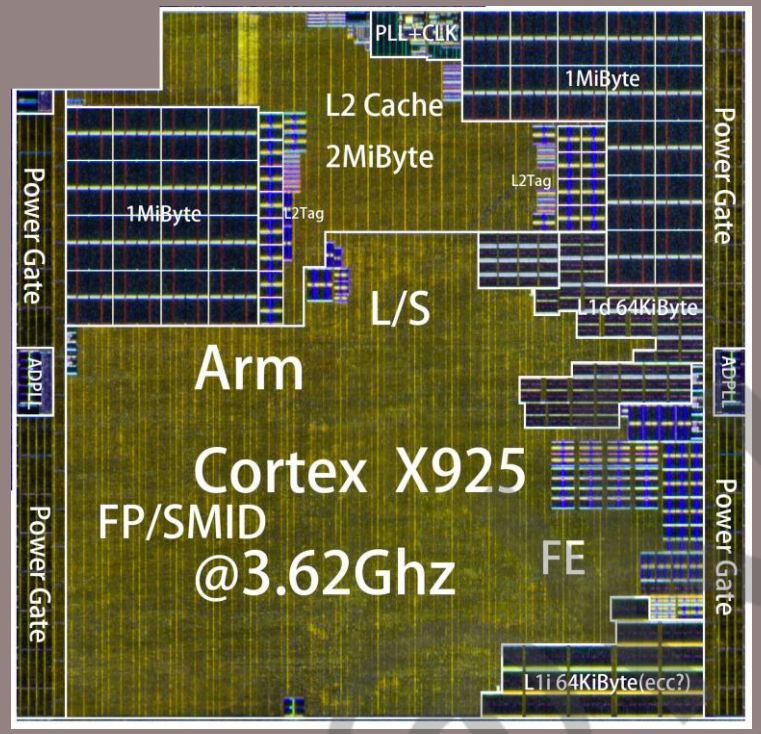
C1 Ultra @D9500

TSMC N3	2-1 Ultra HD lib	2-2 HD lib	3-2 HP lib
Cell H	143	169	195
Gate Pitch	48	48/54	54
Density	214.7	181.67/161.48	157.44

The C1 Ultra is estimated to have 555 million transistors.

N3E 2-2 Fin

- 0.72X Area
- +23% Speed
- -22% Energy



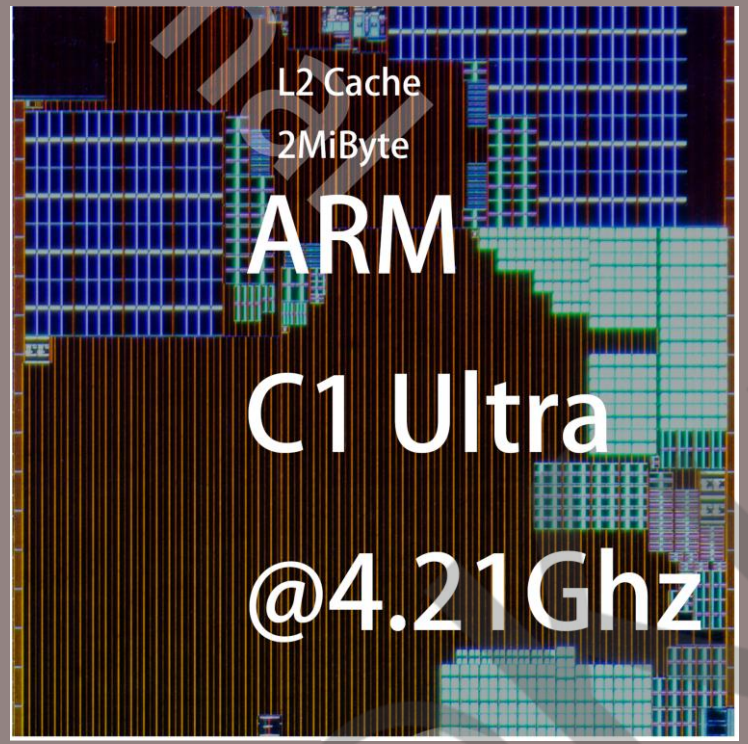
X925 @D9400

TSMC N3	2-1 Ultra HD lib	2-2 HD lib	3-2 HP lib
Cell H	143	169	195
Gate Pitch	48	48/54	54
Density	214.7	181.67/161.48	157.44

The C1 Ultra is estimated to have 464 million transistors.

N3E 2-2 Fin

- 0.72X Area
- +23% Speed
- -22% Energy



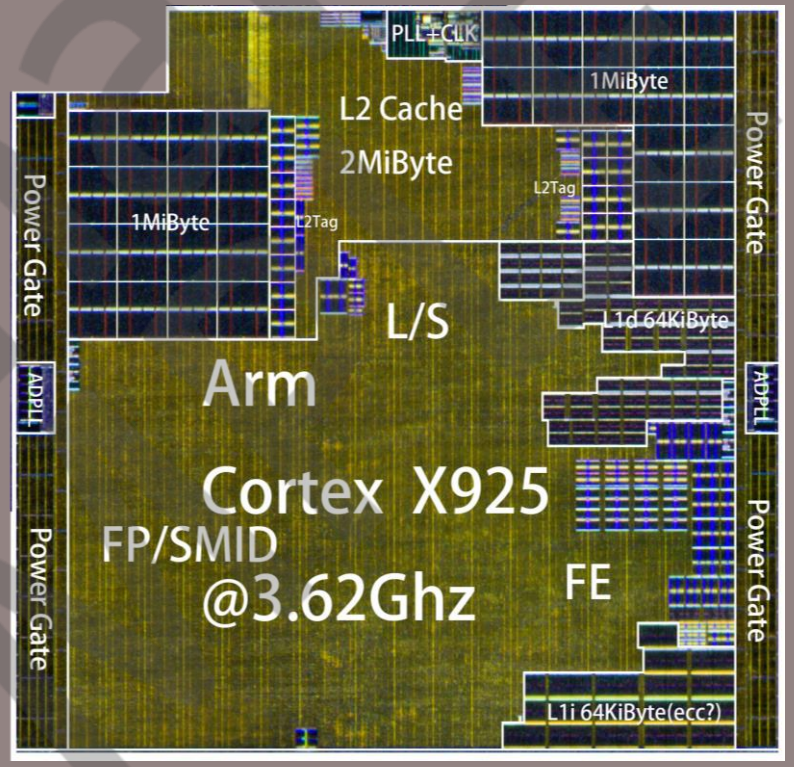
C1 Ultra @D9500

Core size:3.259mm2

Core Trans:555Million

Smaller than 2.27%

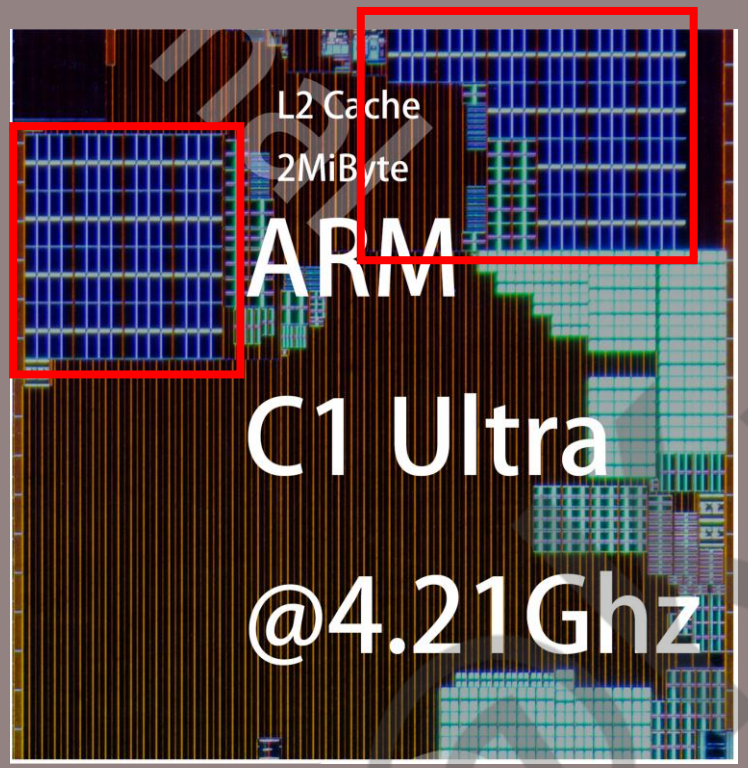
Bigger than 19.61%



X925 @D9400

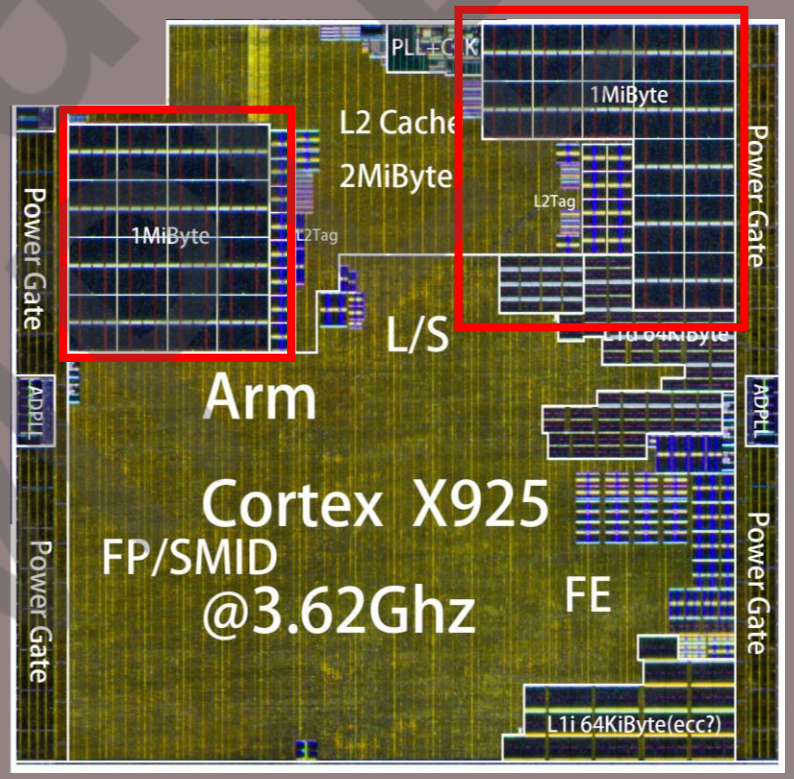
Core size:3.335mm2

Core Trans:464Million



C1 Ultra @D9500

Same 2MiByte L2 Cache



X925 @D9400

On chip analyze-CPU

C1 Ultra @D9500

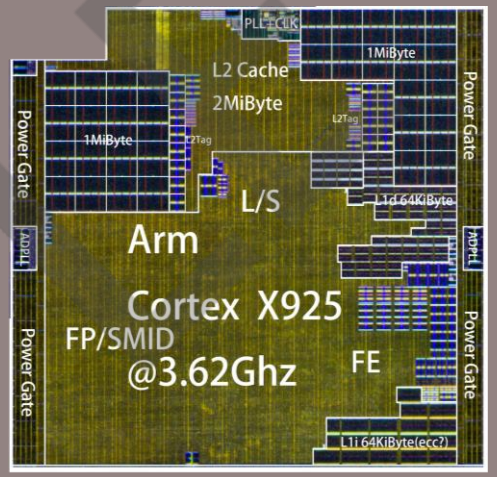
New Power Gate

Smaller

48.58%

0.2mm2

0.389mm2

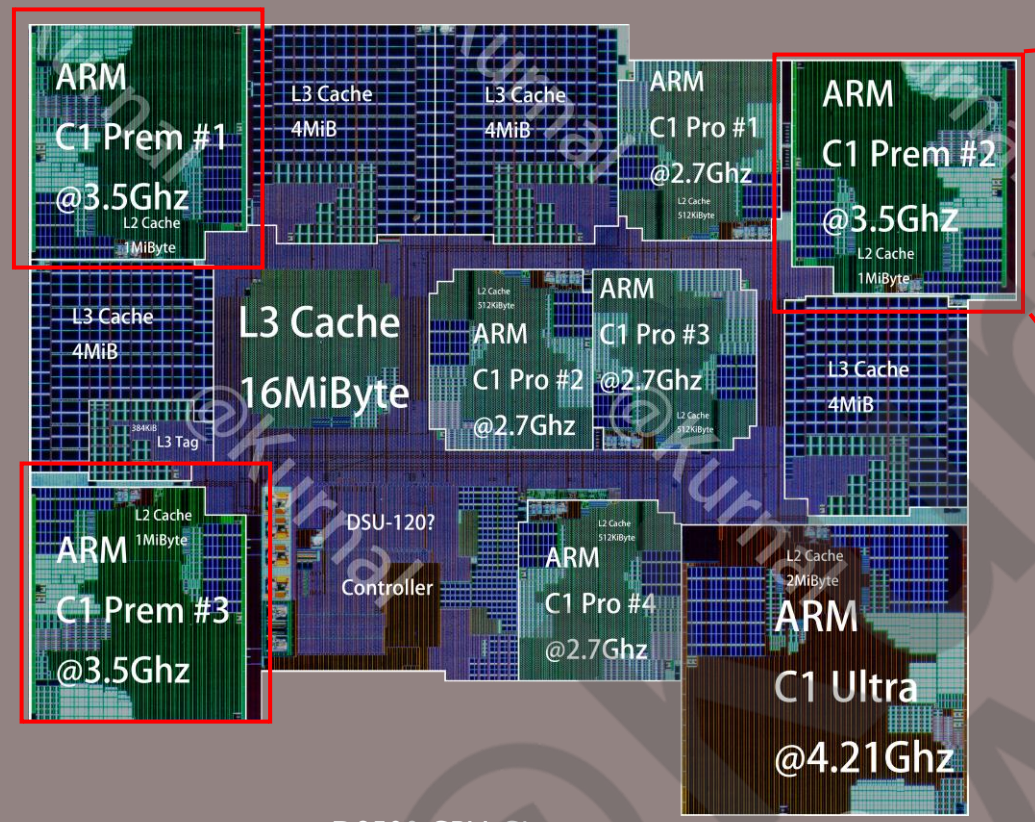


X925 @D9400

On chip analyze-CPU

C1-Prem

On chip analyze-CPU



D9500 CPU Cluster

C1 Prem @D9500

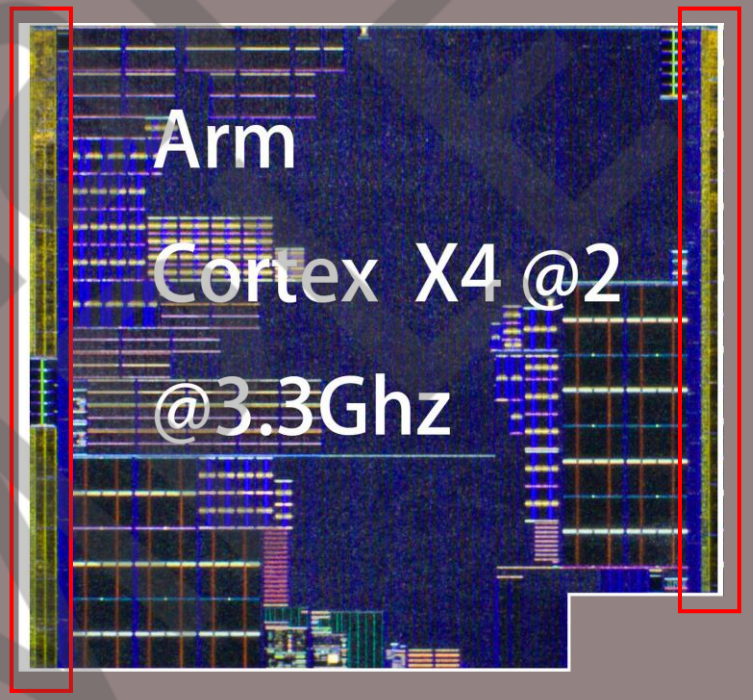
Core size:1.91mm2

C1 Prem @D9500

Core size:1.91mm2

New Power Gate

Same L2 1MiByte

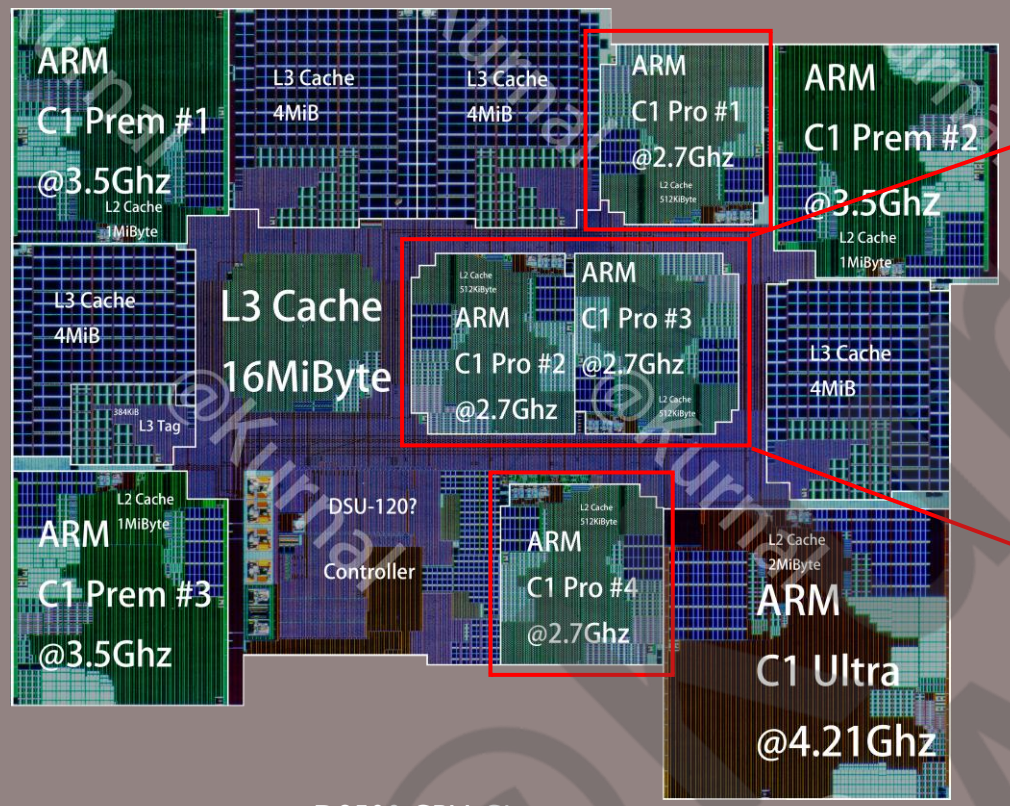


X4m @D9400

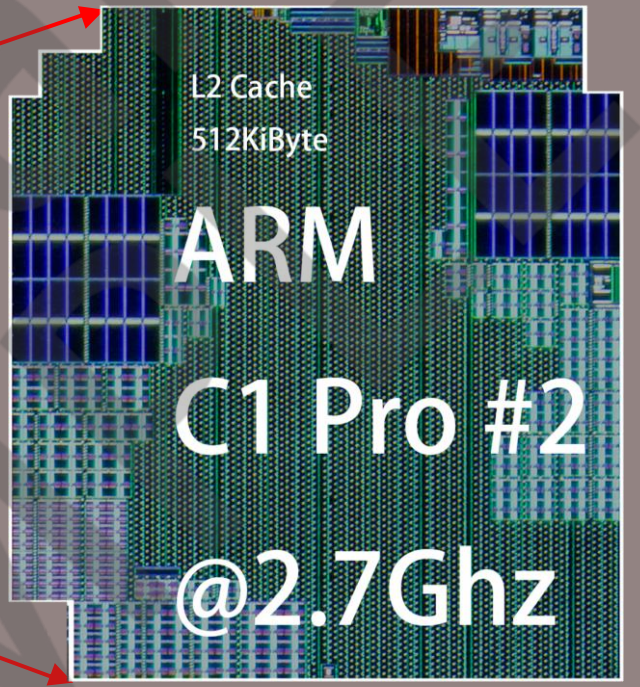
Core size:1.687mm2

On chip analyze-CPU

C1-Pro

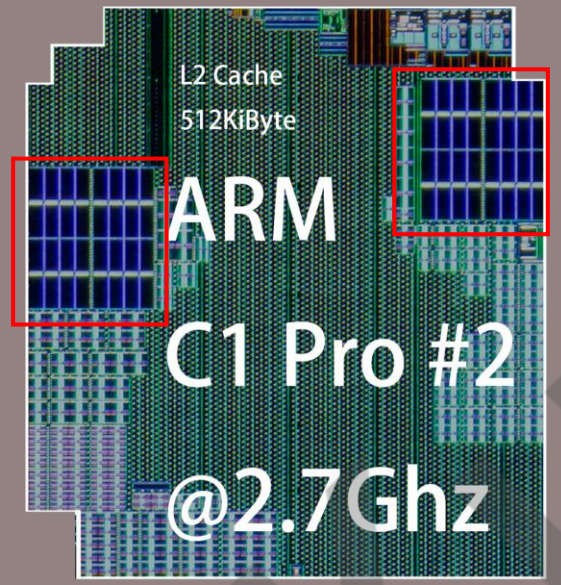


D9500 CPU Cluster



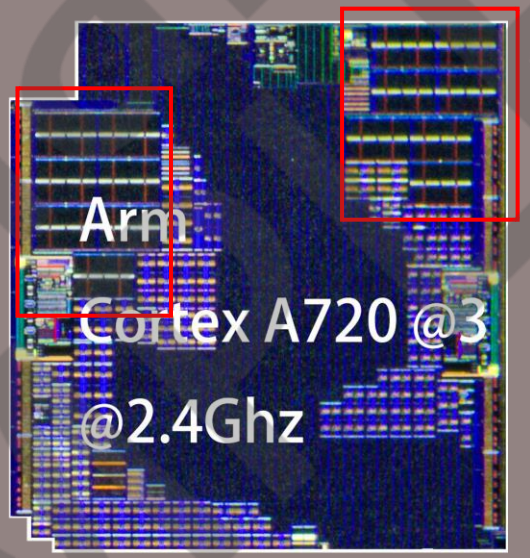
C1 Pro @D9500

Core size:1.131mm2



C1 Pro @D9500

Same L2 512KiB

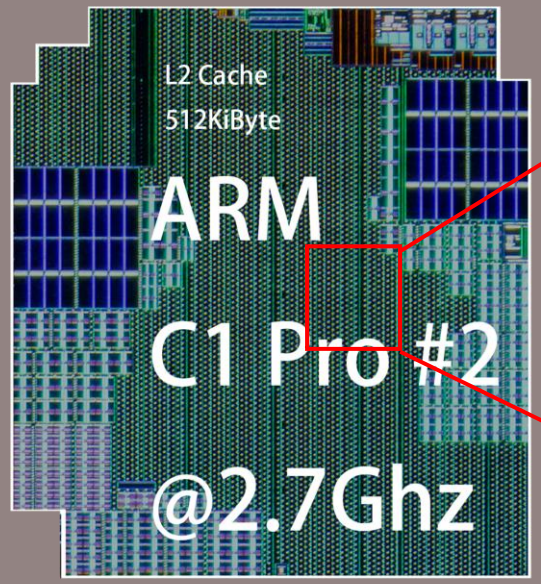


A720 @D9400

Core size:1.131mm2

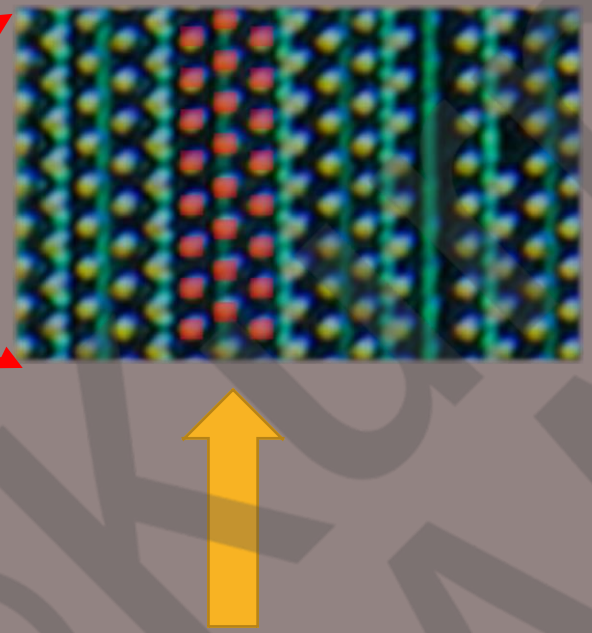
Core size:0.976mm2

Bigger than 15.88%



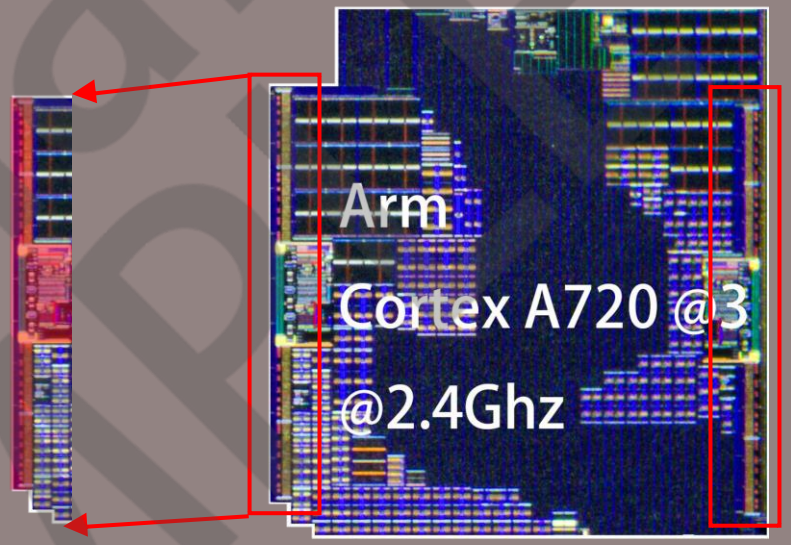
C1 Pro @D9500

Used Perimeter Power Routing



Power Grid

Power edge



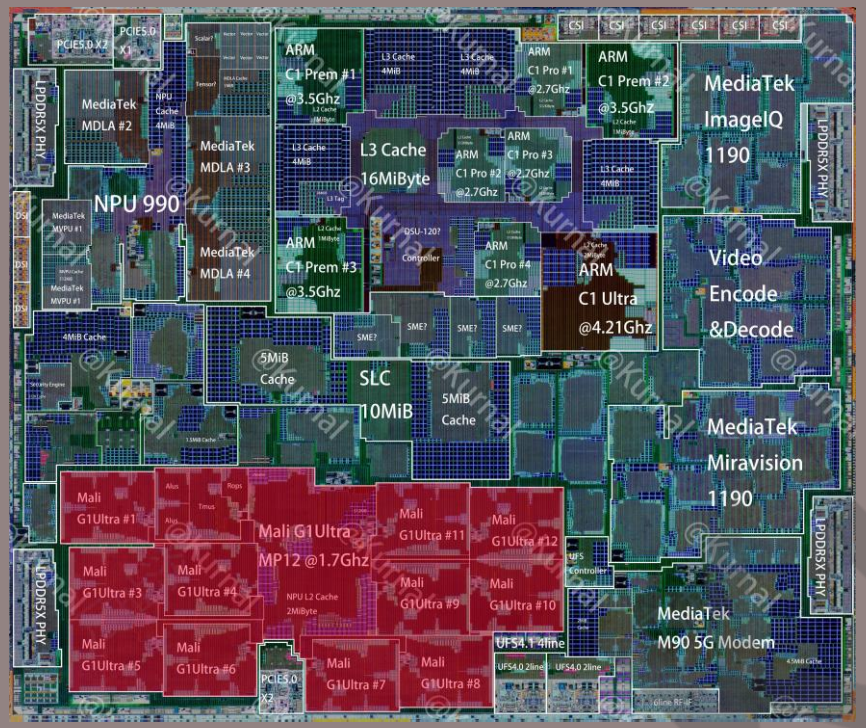
A720 @D9400

Used Power Stripe Distribution

On chip analyze-GPU

G1 Ultra

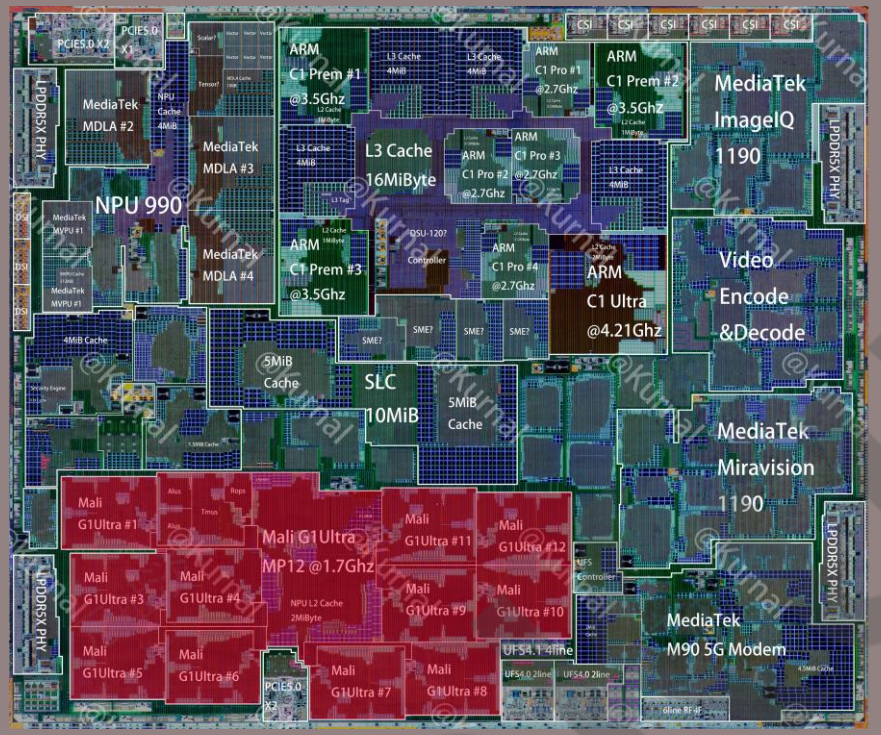
On chip analyze-GPU



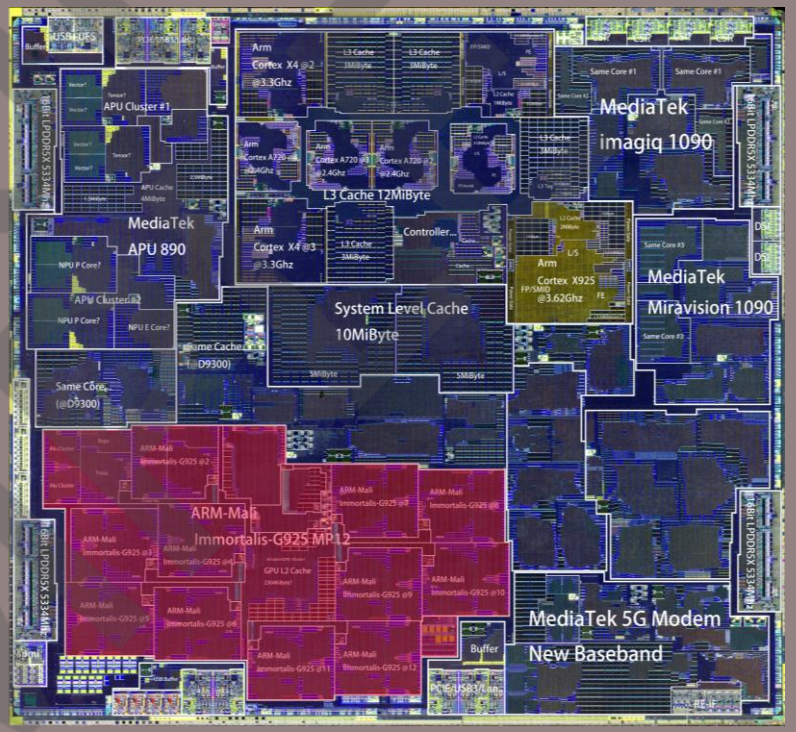
Mali G1-Ultra MP12
@1.7Ghz

GPU size: 24.232mm2
GPU Per Die: 17.24%

On chip analyze-GPU



Mali G1Ultra MP12@D9500

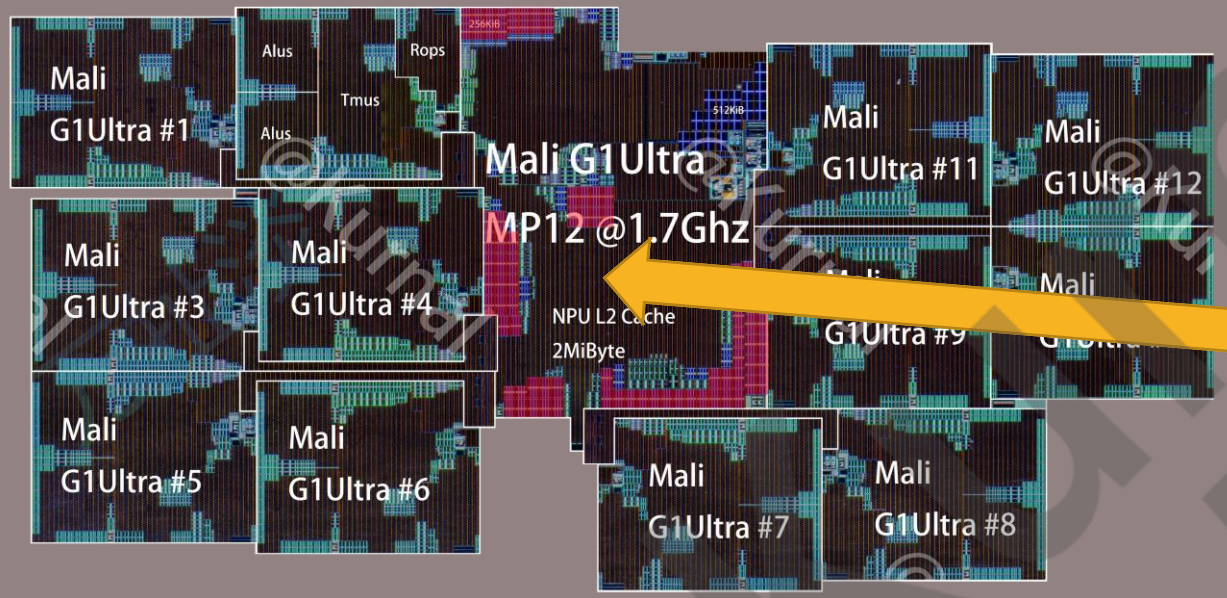


Mali G925 MP12@D9500

Bigger than 10.35%

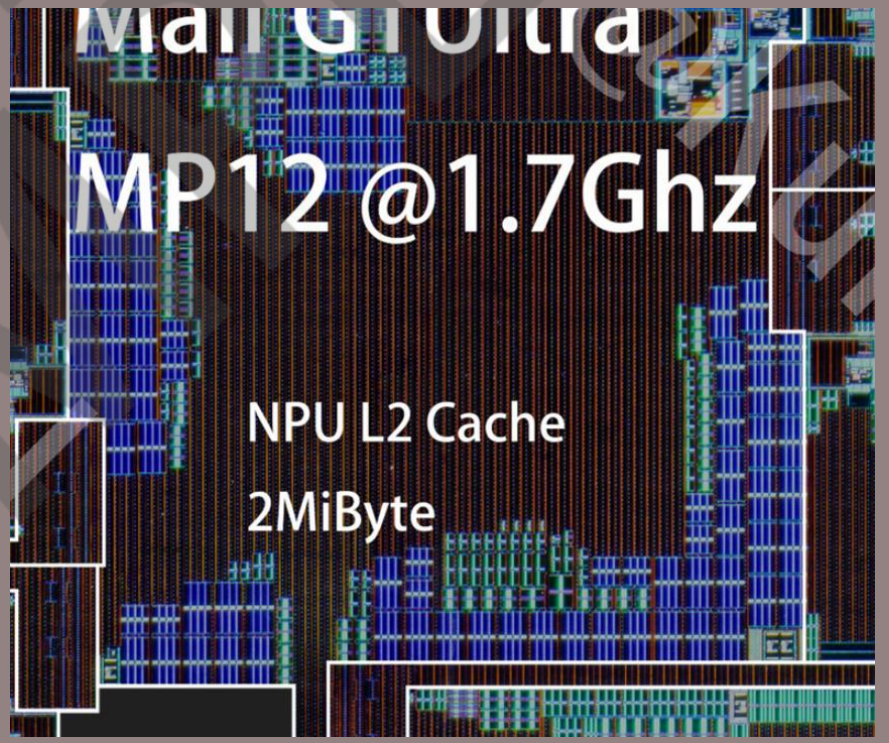
GPU size:	24.232mm2	→	GPU size:	21.959mm2
GPU Per Die :	17.24%	Similar	GPU Per Die:	17.39%

On chip analyze-GPU

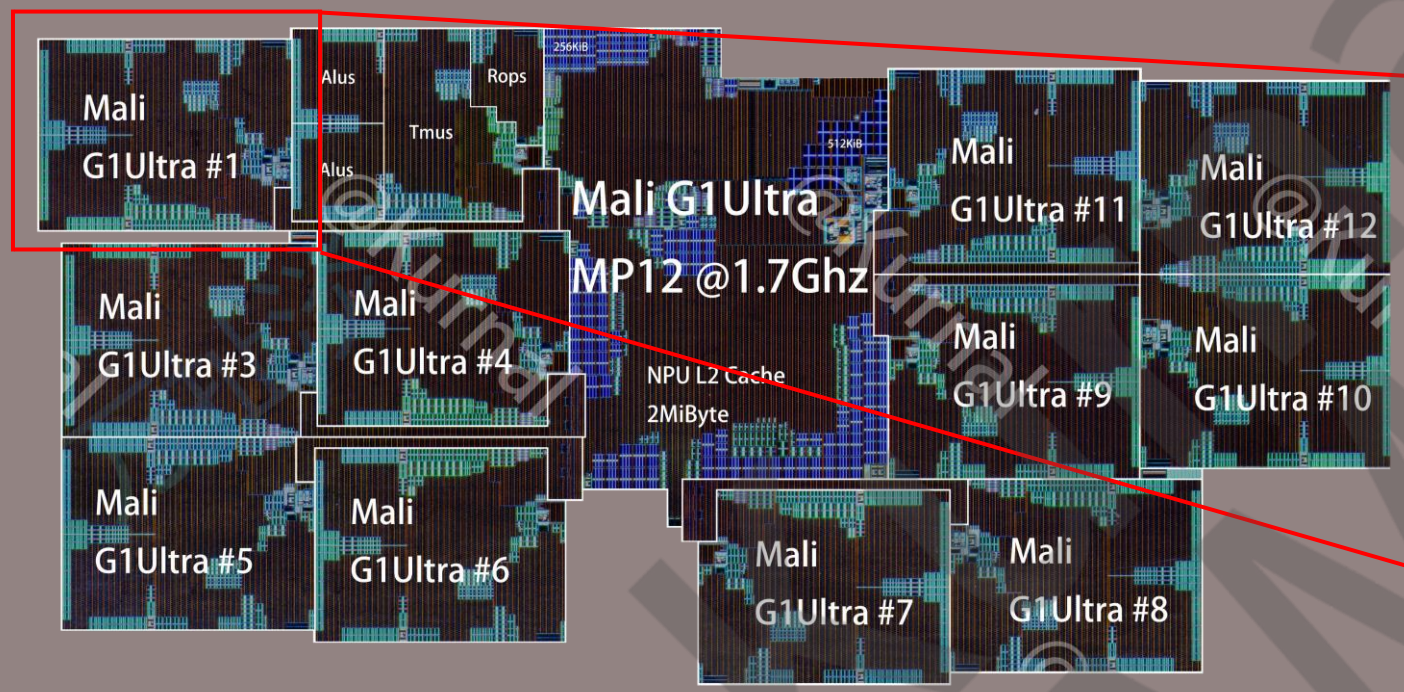


Mali G1Ultra MP12@D9500

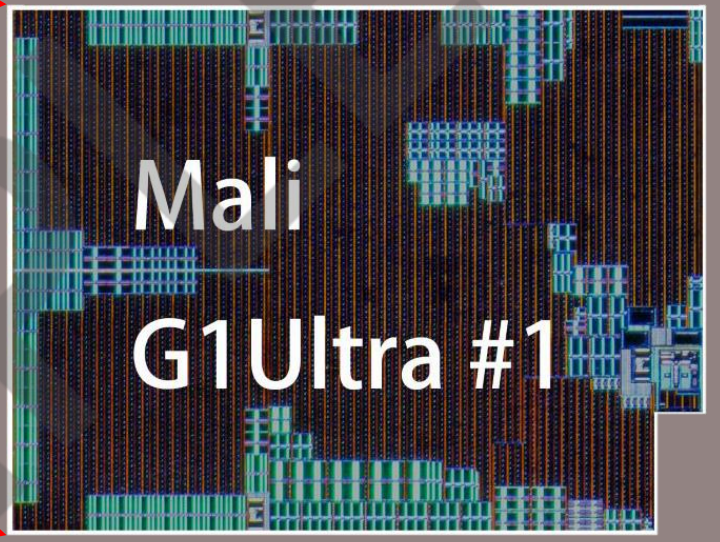
Have 2MiByte L2 Cache



On chip analyze-GPU

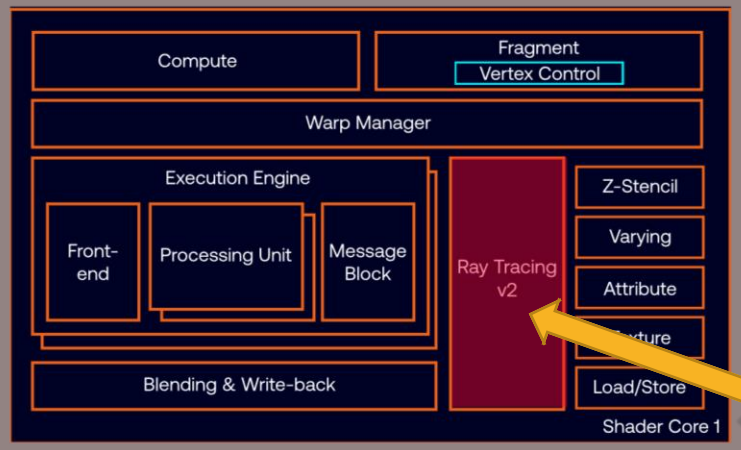


Mali G1Ultra MP12@D9500



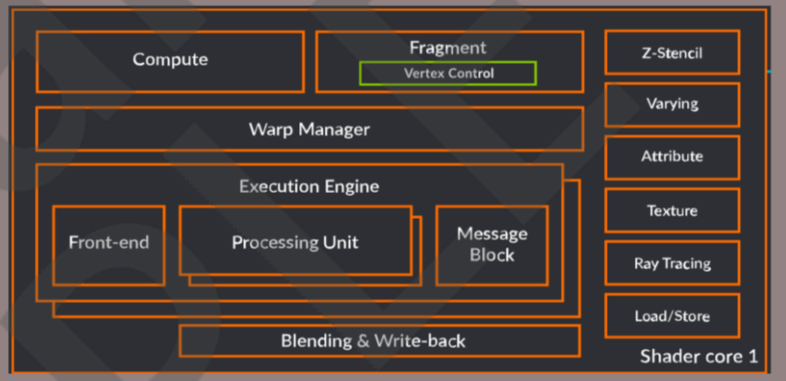
Mali G1Ultra Core @D9500

On chip analyze-GPU

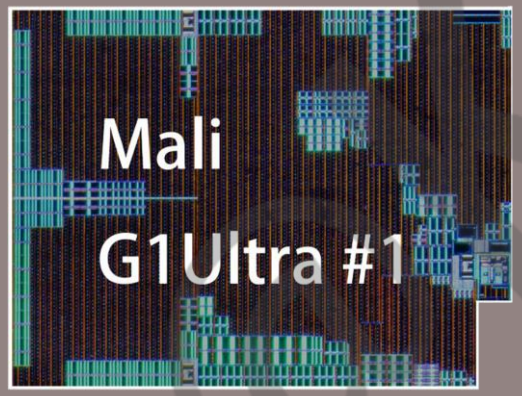


Mali G1Ultra Core @D9500

New Ray Tracing

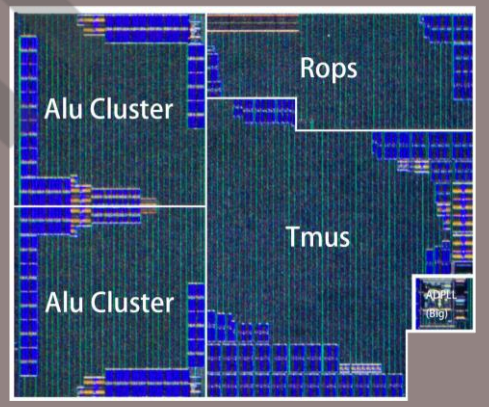


Mali G925 @D9400



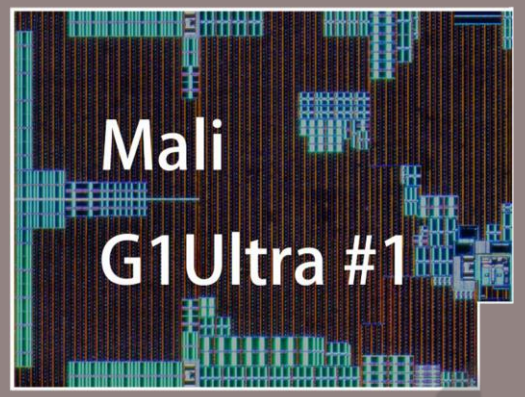
Core size: 1.55mm2

Bigger than 11.91%



Core size: 1.385mm2

Mali G1Ultra Core @D9500



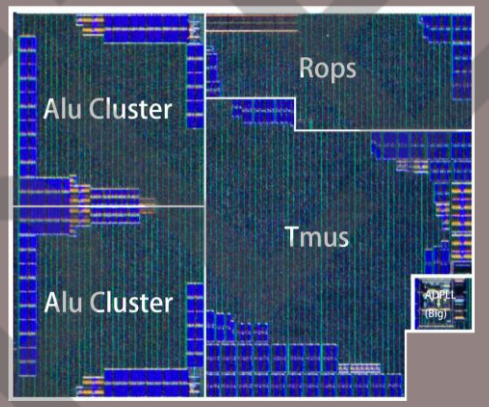
Core size: 1.55mm2

Transister Nb: 282Million

Same TSMC 2-1 Fin

Bigger than 11.91%

Mali G925 @D9400



Core size: 1.385mm2

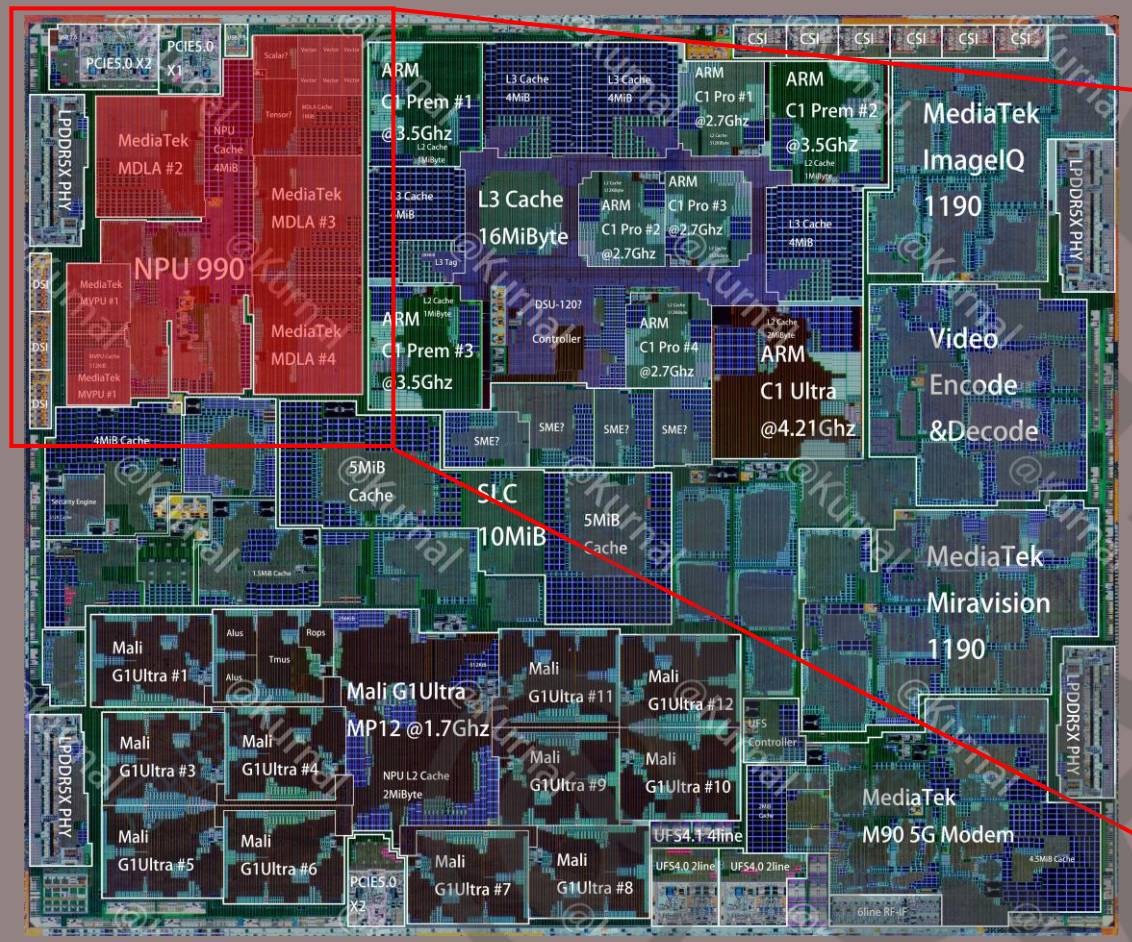
Transister Nb: 252Million

It uses the same TSMC N3 node 2-1 library, so its transistor count and area are increased by 11.91%.

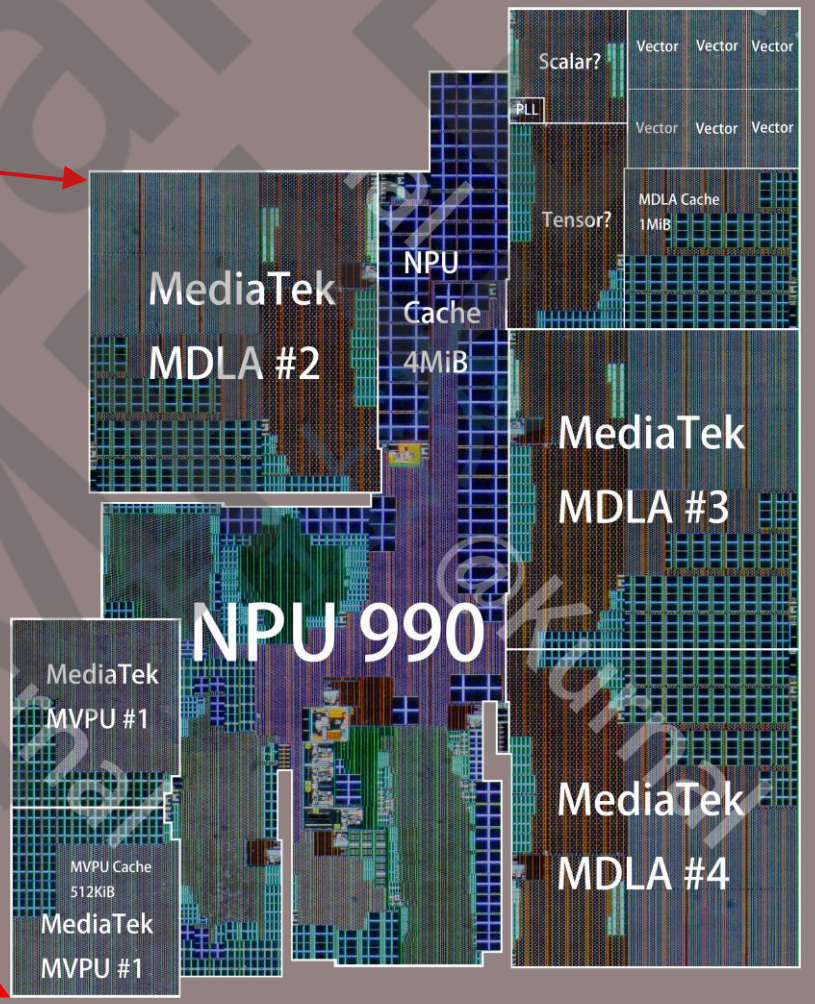
On chip analyze-NPU

NPU 990

On chip analyze-NPU

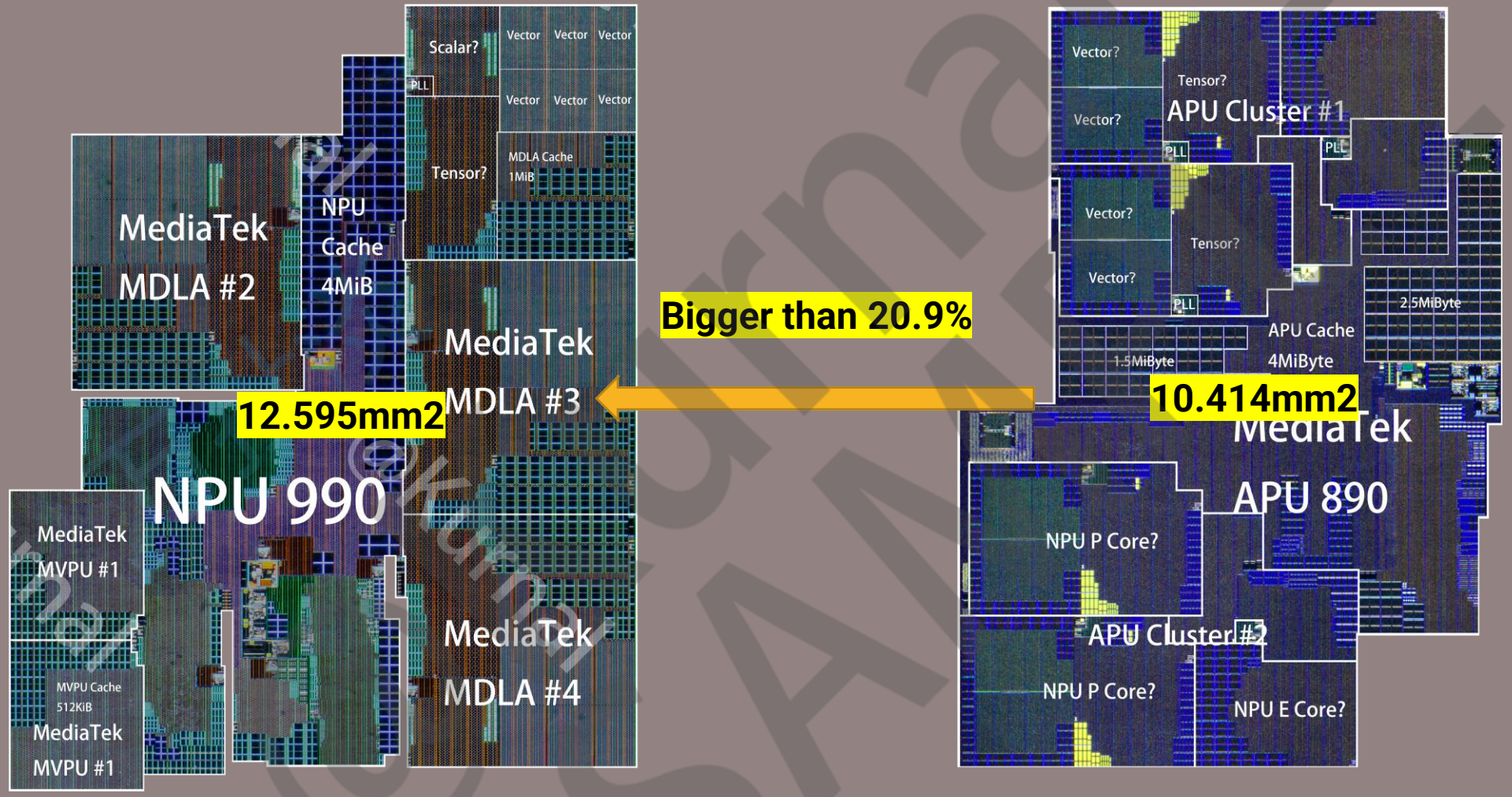


@D9500



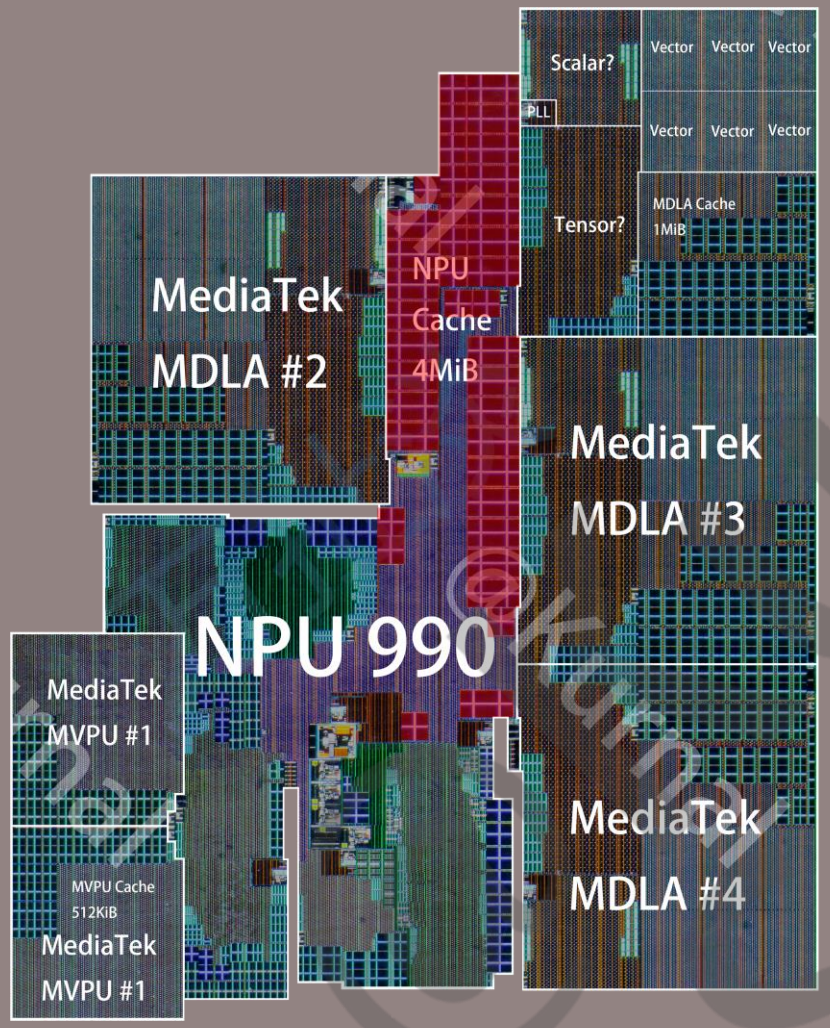
NPU990 @D9500

On chip analyze-NPU



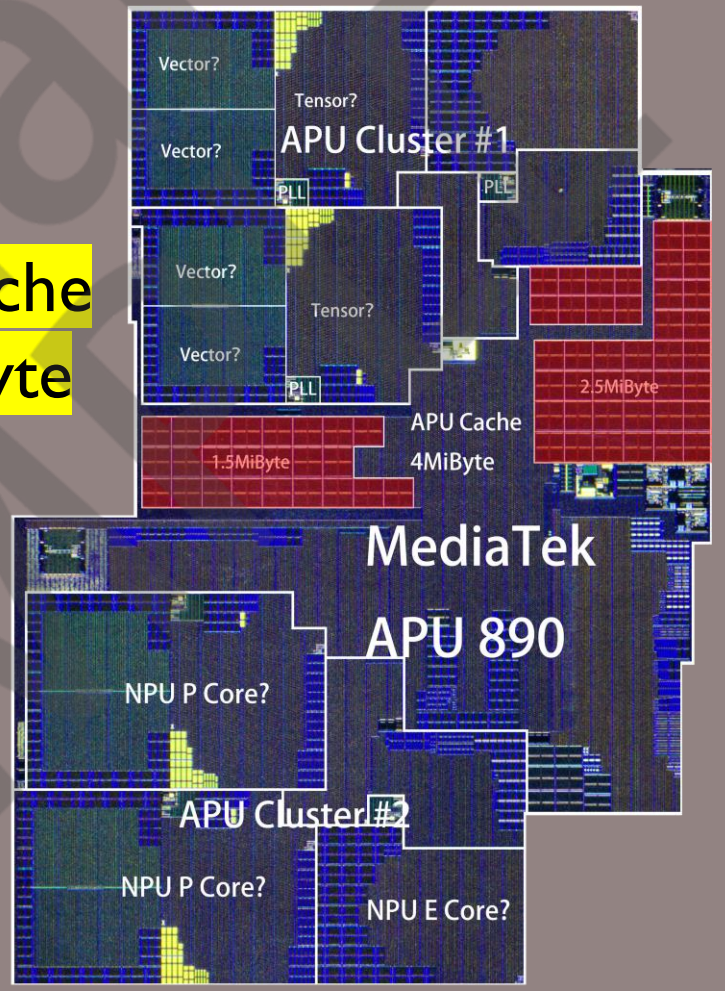
NPU990 @D9500

APU890 @D9400



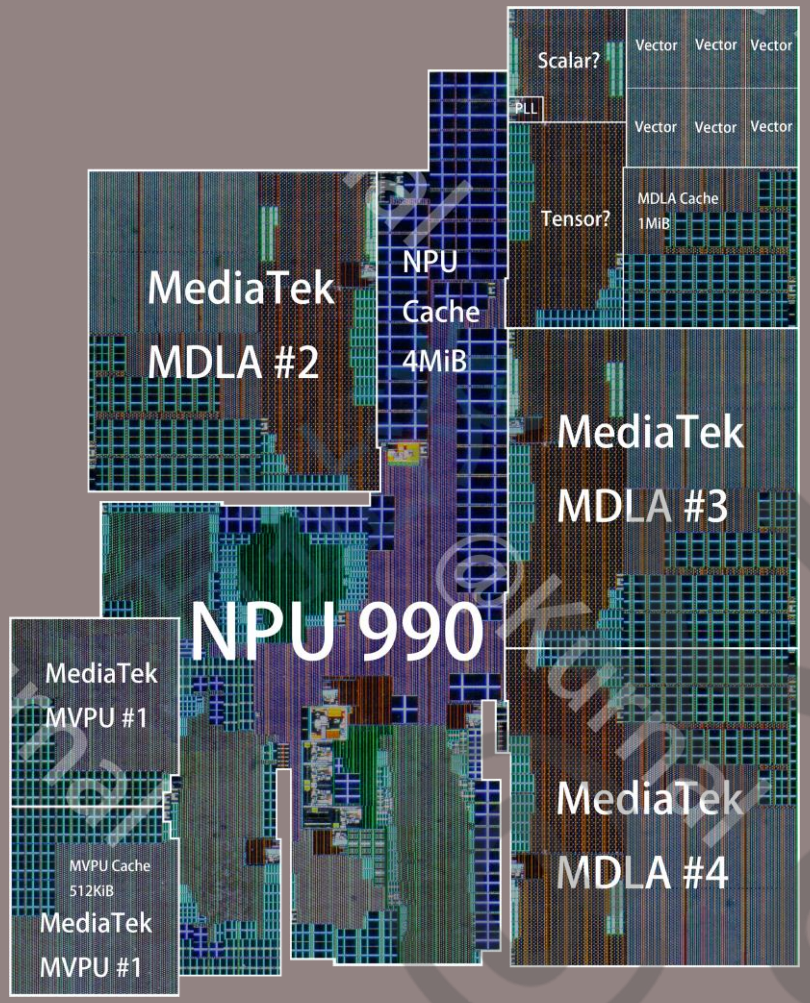
NPU990 @D9500

NPU L2 Cache
Both 4MiByte

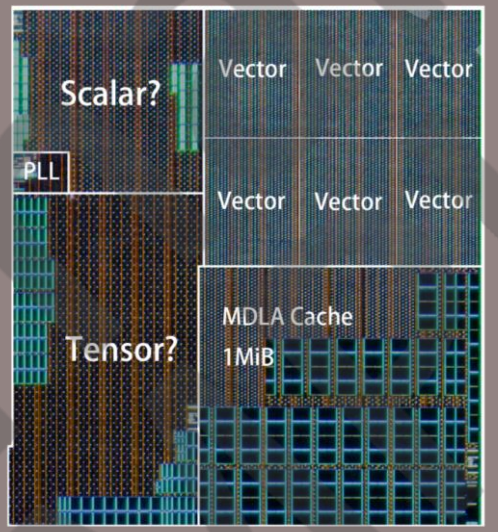


APU890 @D9400

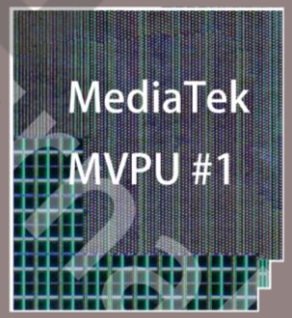
On chip analyze-NPU



NPU990 @D9500

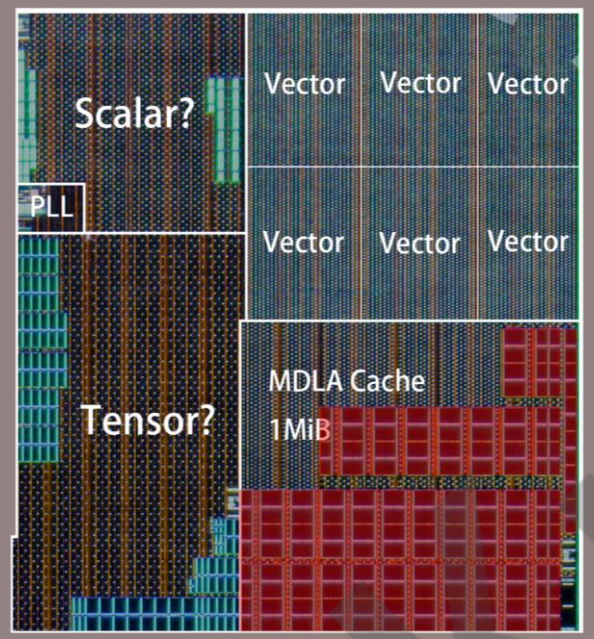


4x MDLA
Mediatek
Deep
Learning
Accelerator



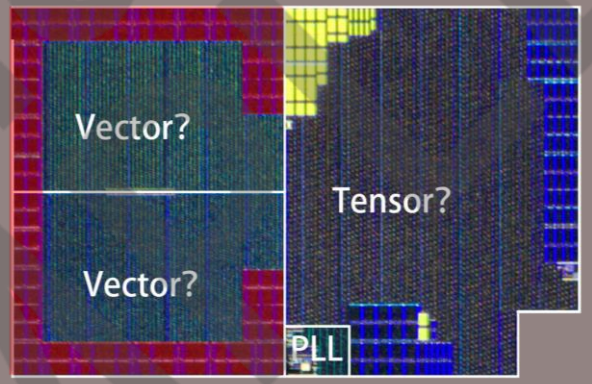
2x MVPU
Mediatek
Vision
Processing
Unit

On chip analyze-NPU



NPU990 MDLA @D9500

MDLA Cache 1MiByte

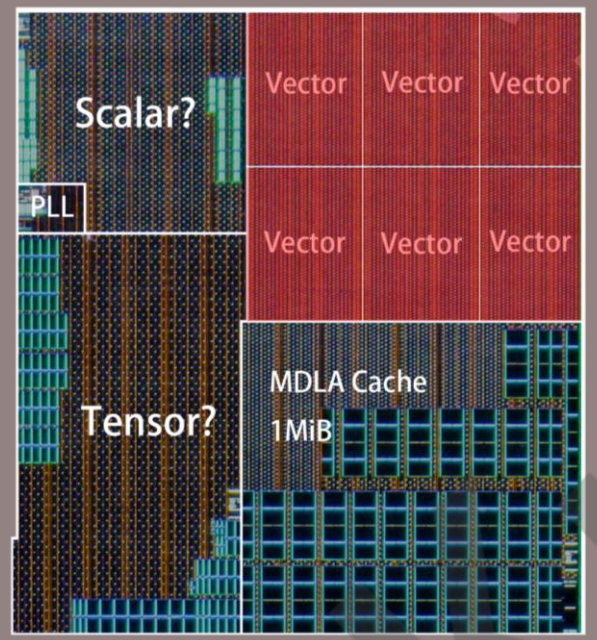


APU890 MDLA @D9400

MDLA Cache 512KiByte?

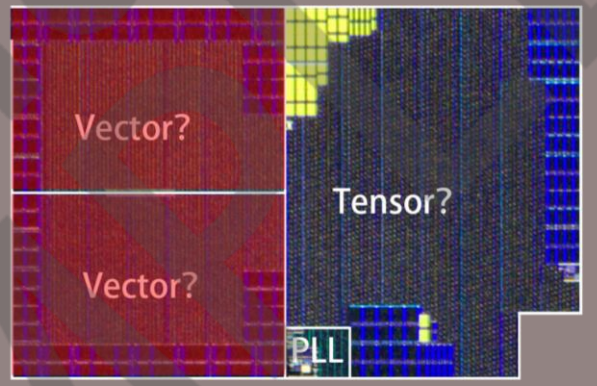
Bigger than 100%

On chip analyze-NPU



NPU990 MDLA @D9500

6Cu Vector
Core size:1.811mm2

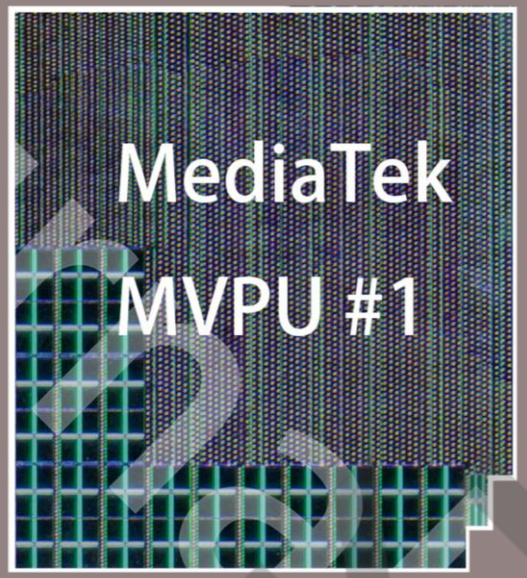


APU890 MDLA @D9400

2Cu Vector
Core size:1.08mm2

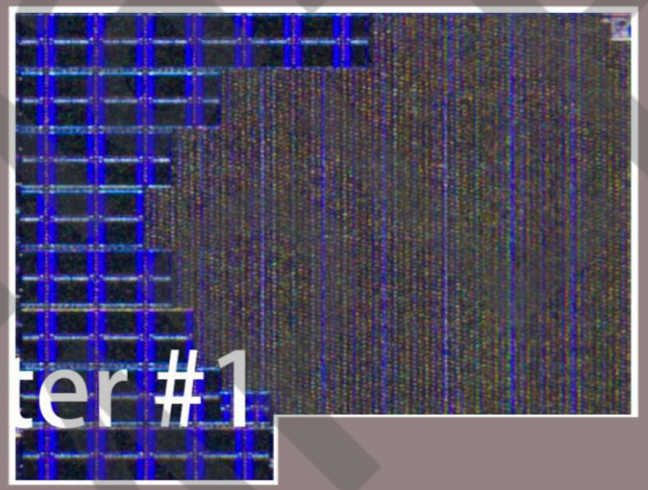
Bigger than 67.68%

On chip analyze-NPU



NPU990 MVPU @D9500

Core size:0.62mm2

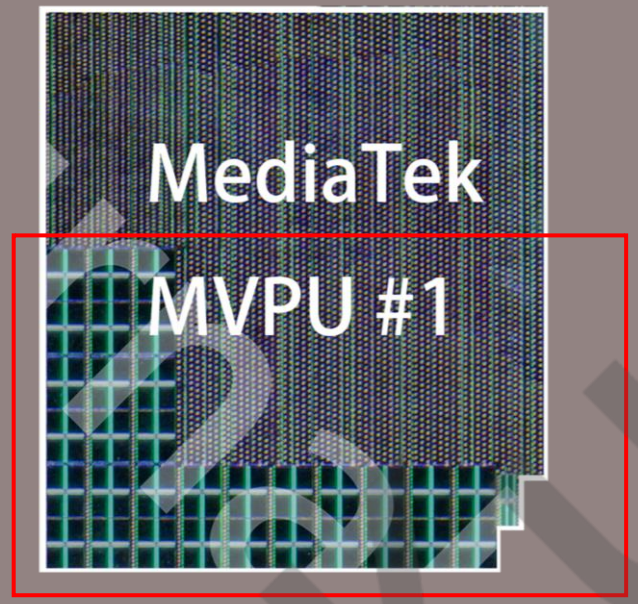


APU890 MVPU @D9400

Core size:0.908mm2

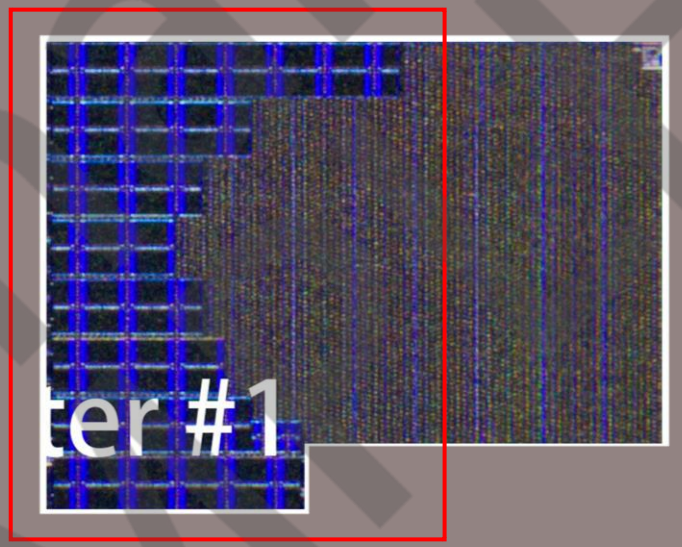
Small than 31.7%

On chip analyze-NPU



NPU990 MVPU @D9500

MVPU Cache 512KiB



APU890 MVPU @D9400

MVPU Cache 512KiB

Same VPU Cache