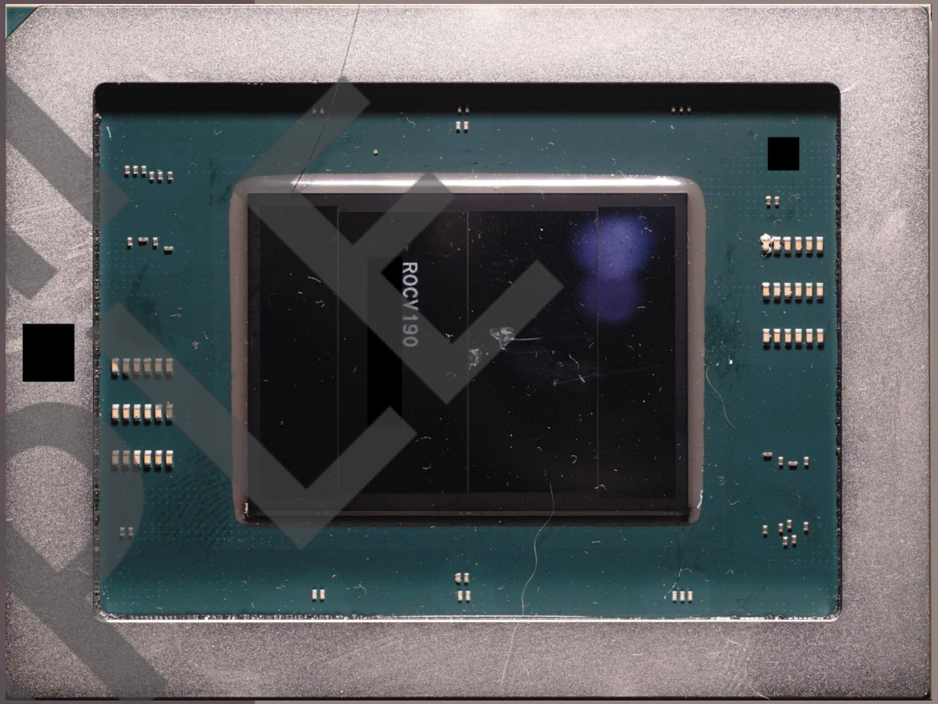
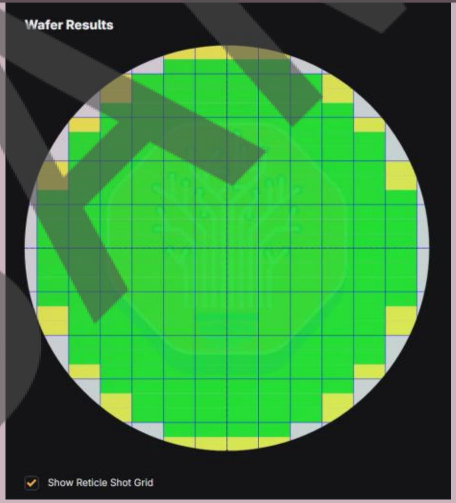
Huawei
Kun Peng 930

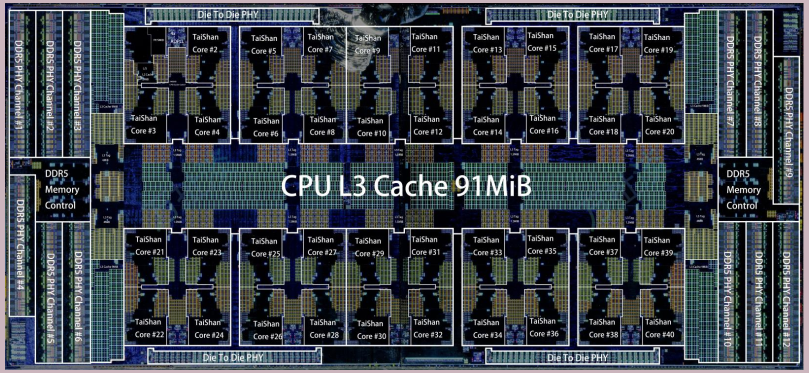
Chip and Semi process analyze

V1.1



@Kurnal





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SAMPLE

Verison of this Report

Version	Date	Updates	Anthor
V0	2025/08/08 16:33	Working	Kurnal
V1	2025/08/22 0:43	Finish	Kurnal
V1.1	2025/08/23 22:32	Cut code	Kurnal
Q2-B站工坊			

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About Authors

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PCB Analyze

Kun Peng 930

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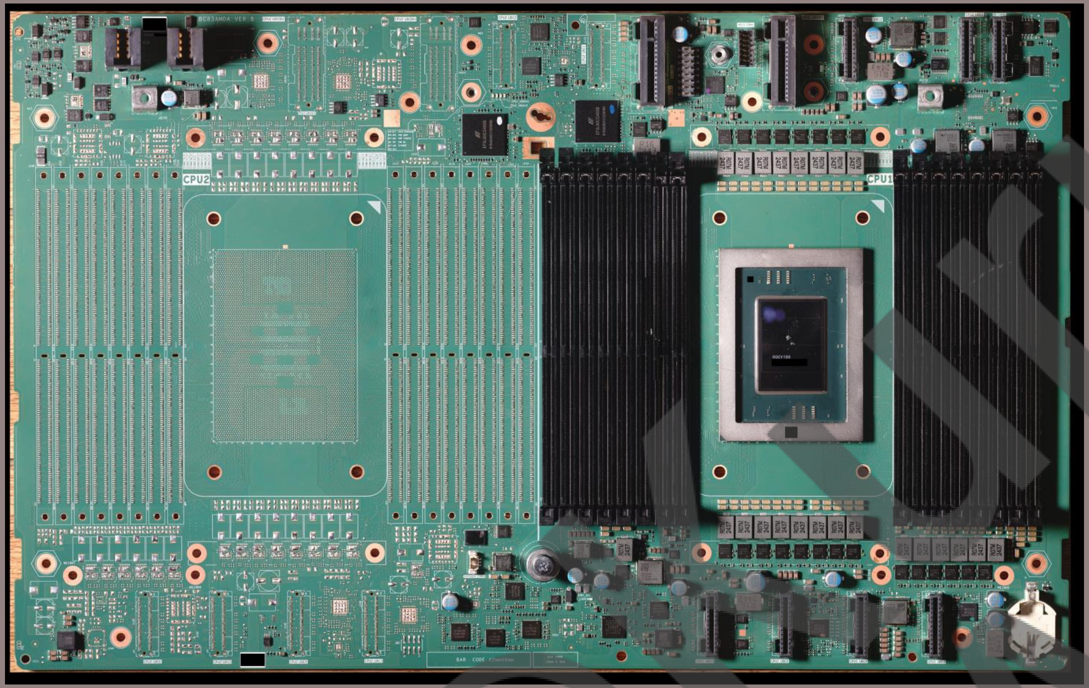
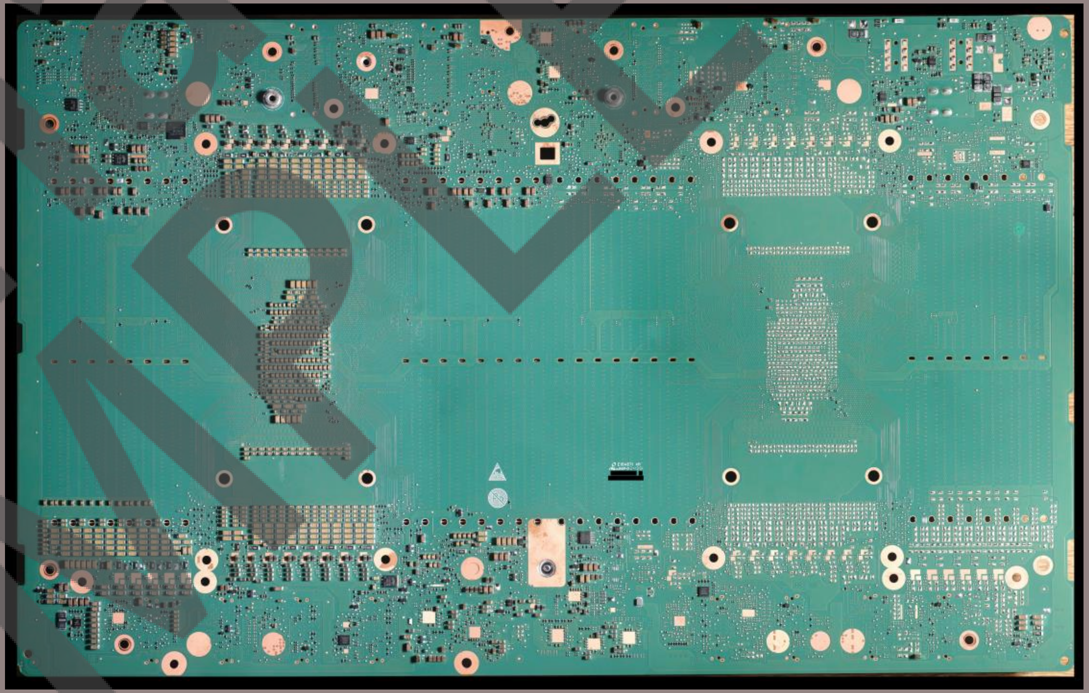
SAMPLE

PCB Analyze



KunPeng930 PCB Topside View



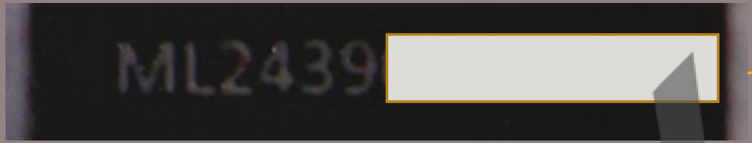
KunPeng930 PCB Backside View

@Kurnal SAMPLE

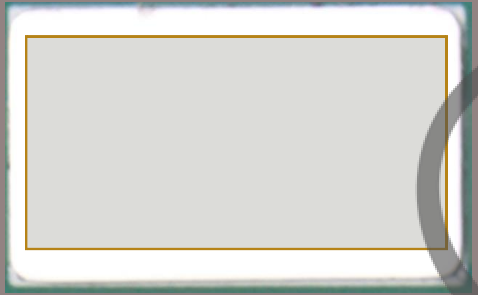
PCB Analyze-PCB Mark


BC83AMDA VER.B

PCB Name： BC83AMDA
VER.B


ML2439[redacted]

PCB SN? ML2439[redacted]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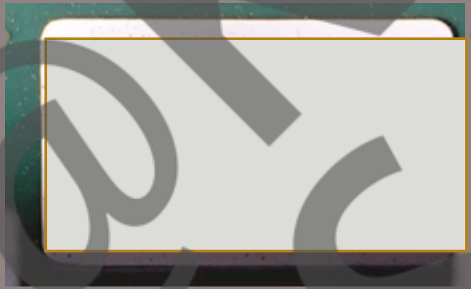
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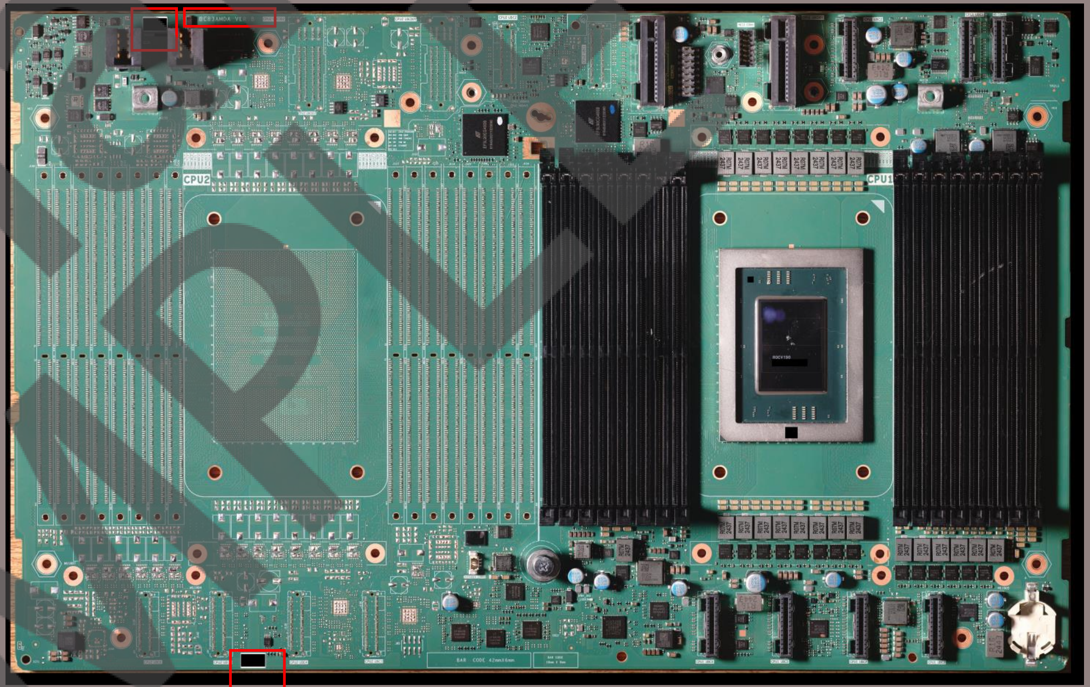
PCB QR Code



KunPeng930 PCB Topside View

PCB made/density? in Year 2024 Week 39

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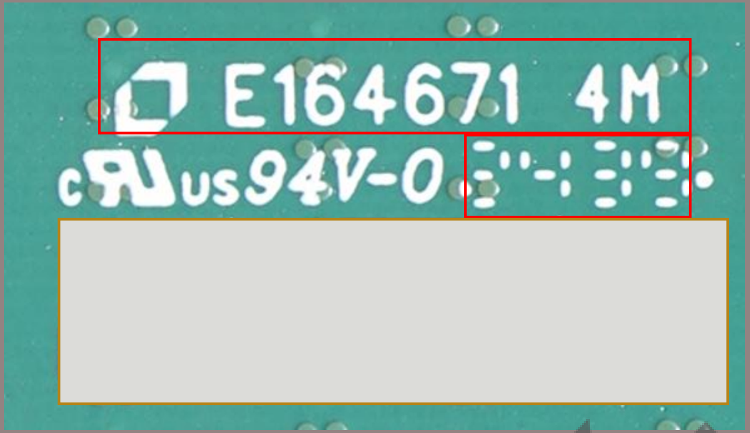
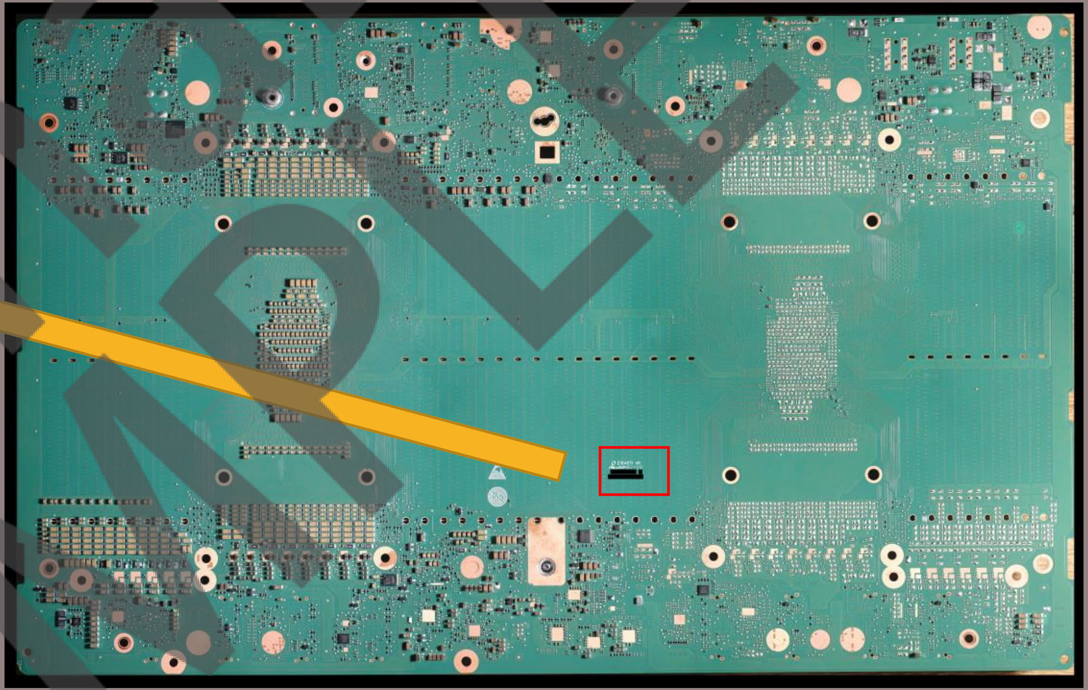
PCB Analyze-PCB Mark



Made on Year 2024 Week 39
PCB No.194



KunPeng930 PCB Backside View

PCB Made By 方正(FounderTech)
E164671 4M： ZhuHai Founder Tech

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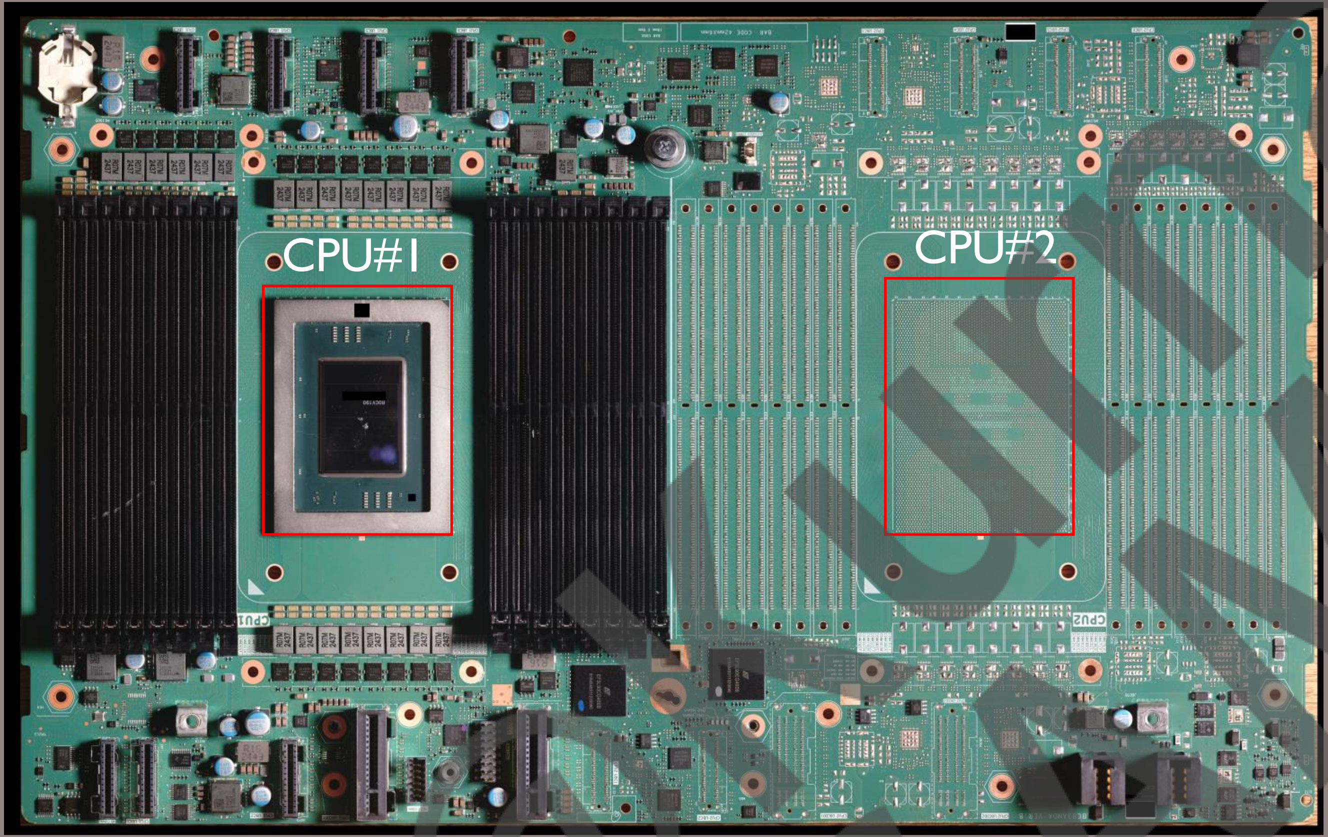
SAMPLE

PCB Analyze

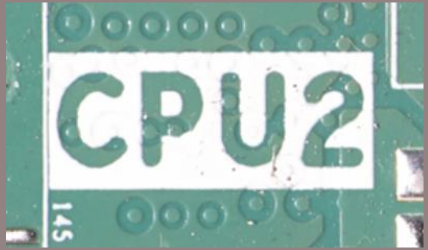


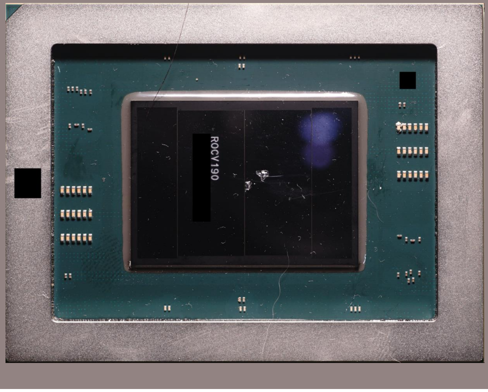
Have SMT

None SMT

This PCB is only half-filled with materials
but it have full Pads
so we can analyze the full socket on the motherboard.

Obviously this is a set of dual-CPU servers





Dual CPUs

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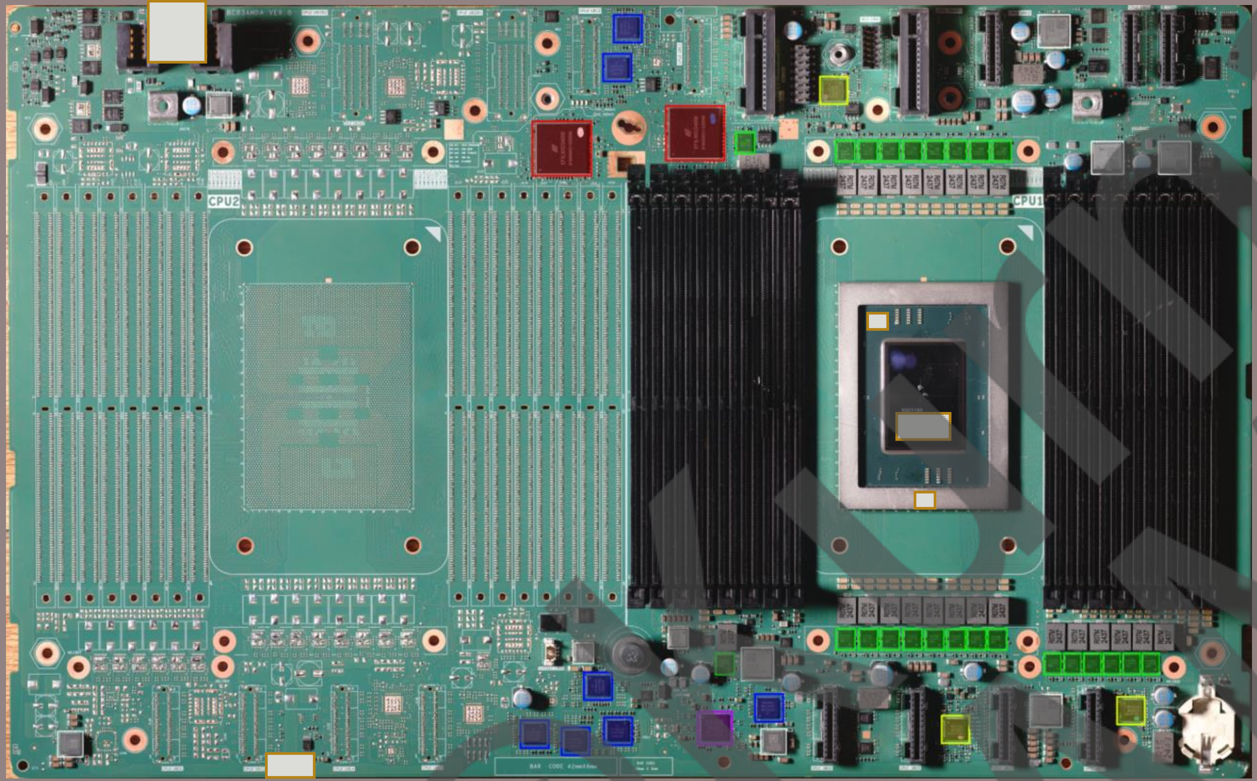
PCB Analyze-Bom

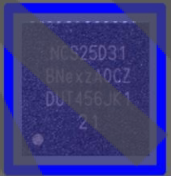


Anlogic EF3L90CG400B
FPGA

安路科技 ANLOGIC

VMQ ES6927 XD5215
DrMOS PMIC

? None data



新港海岸 NCS25D31
PCIE Fan-out Buffer

NewCoSemi 新港海岸 NEWCOSEMI TECHNOLOGY

宁波奥拉半导体 AU5325B
4-Channel JACS

Aurasemi

芯源科技 MP2882A
Multi-Phase Controller

MPS

Huawei NAE12S20
DC-DC Power SiP

Huawei NAM12S06
DC-DC Power SiP

Huawei NAE12S17
DC-DC Power SiP

HUAWEI

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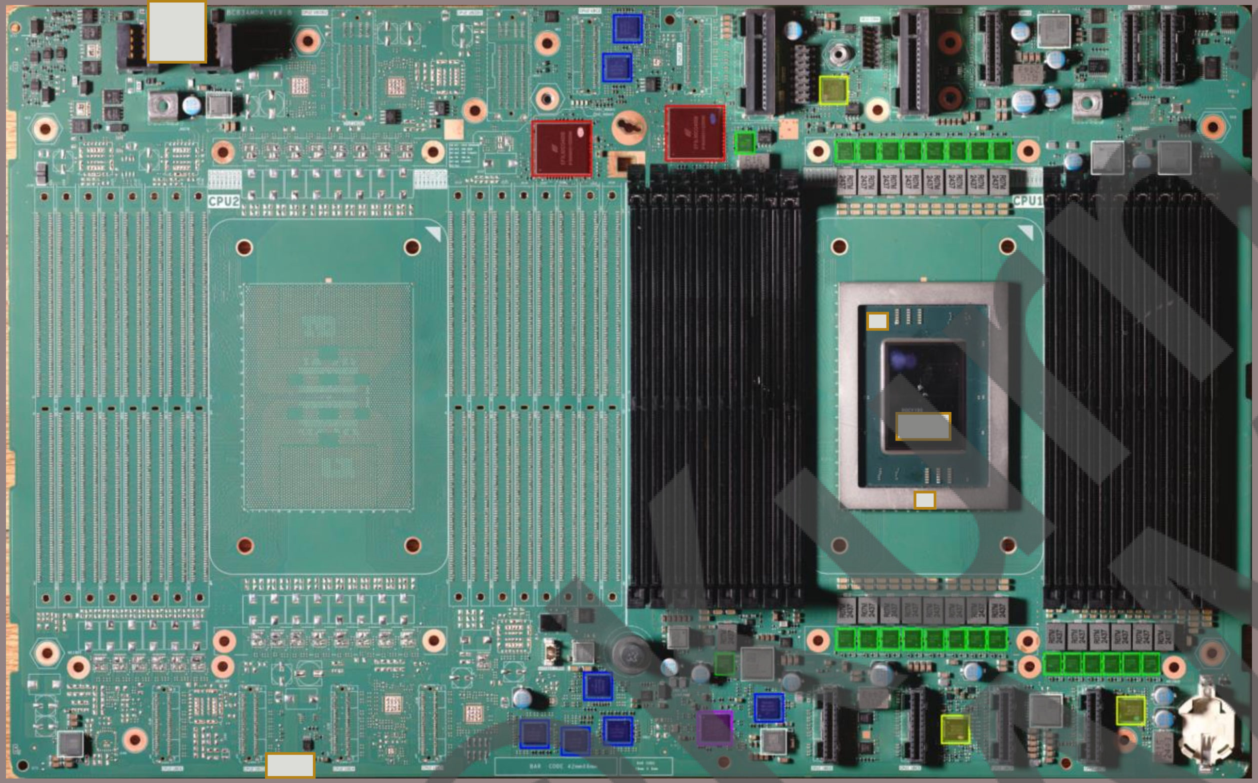
PCB Analyze-Bom



VMQ ES6927 XD5215

DrMOS PMIC

Make analyze and make sure that

Who make those DrMOS chips

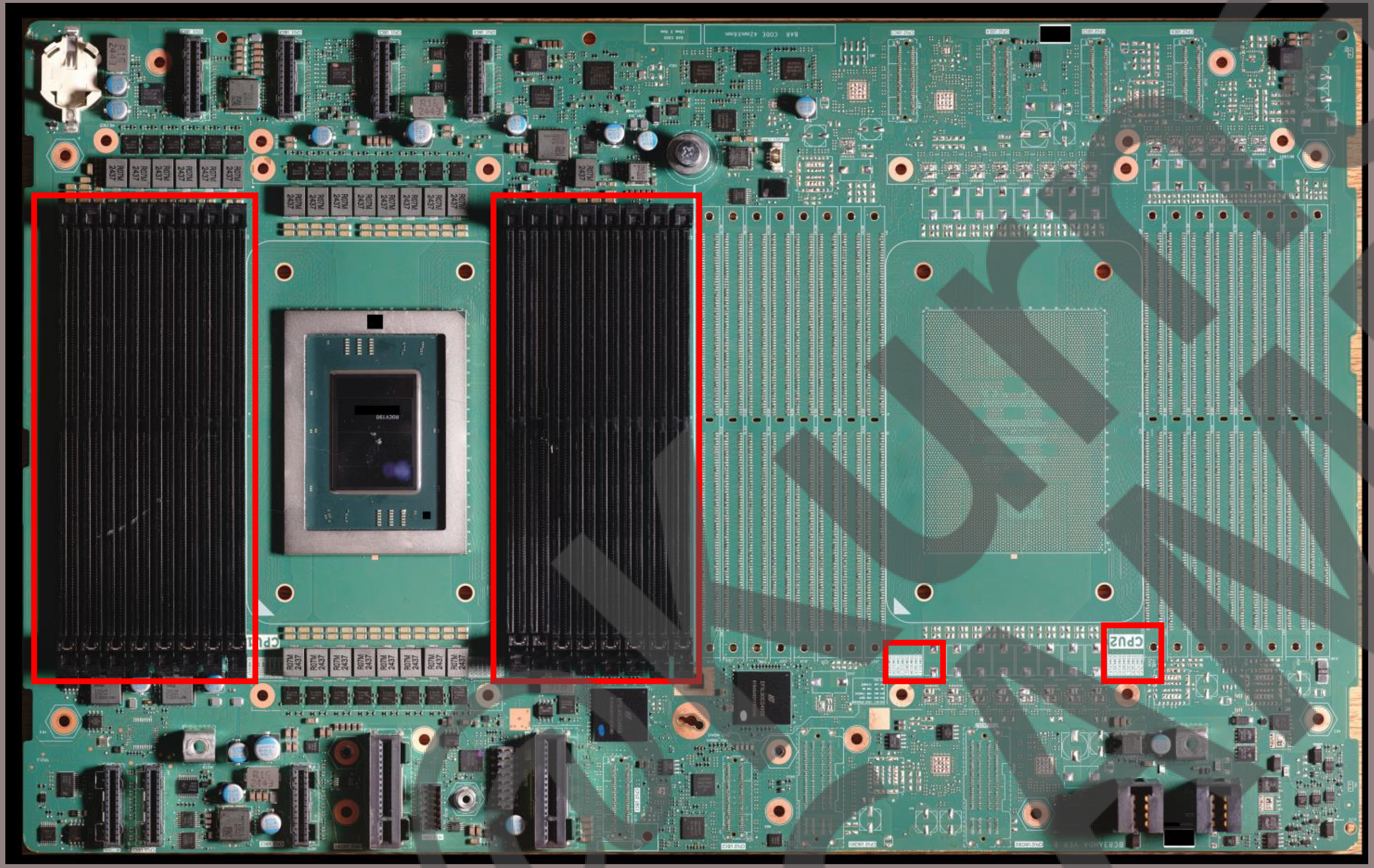
@Kurnal SAMPLE

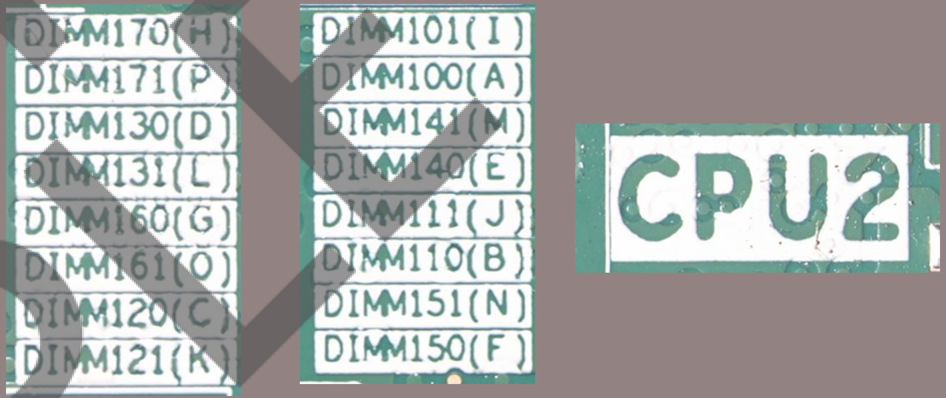
PCB Socket Analyze

Kun Peng 930

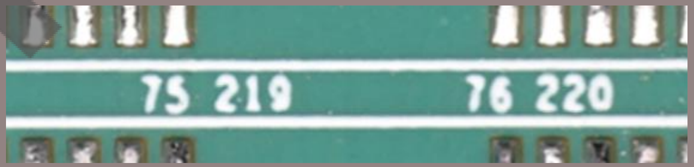
@Kurnal SAMPLE

PCB Socket analyze





Each CPU has 16 DDR5 Socket
with 8 channels



The Socket have 288 pin
cut in 75/76,219/220

And cant used with Consumer DDR5
It is Servers DDR5

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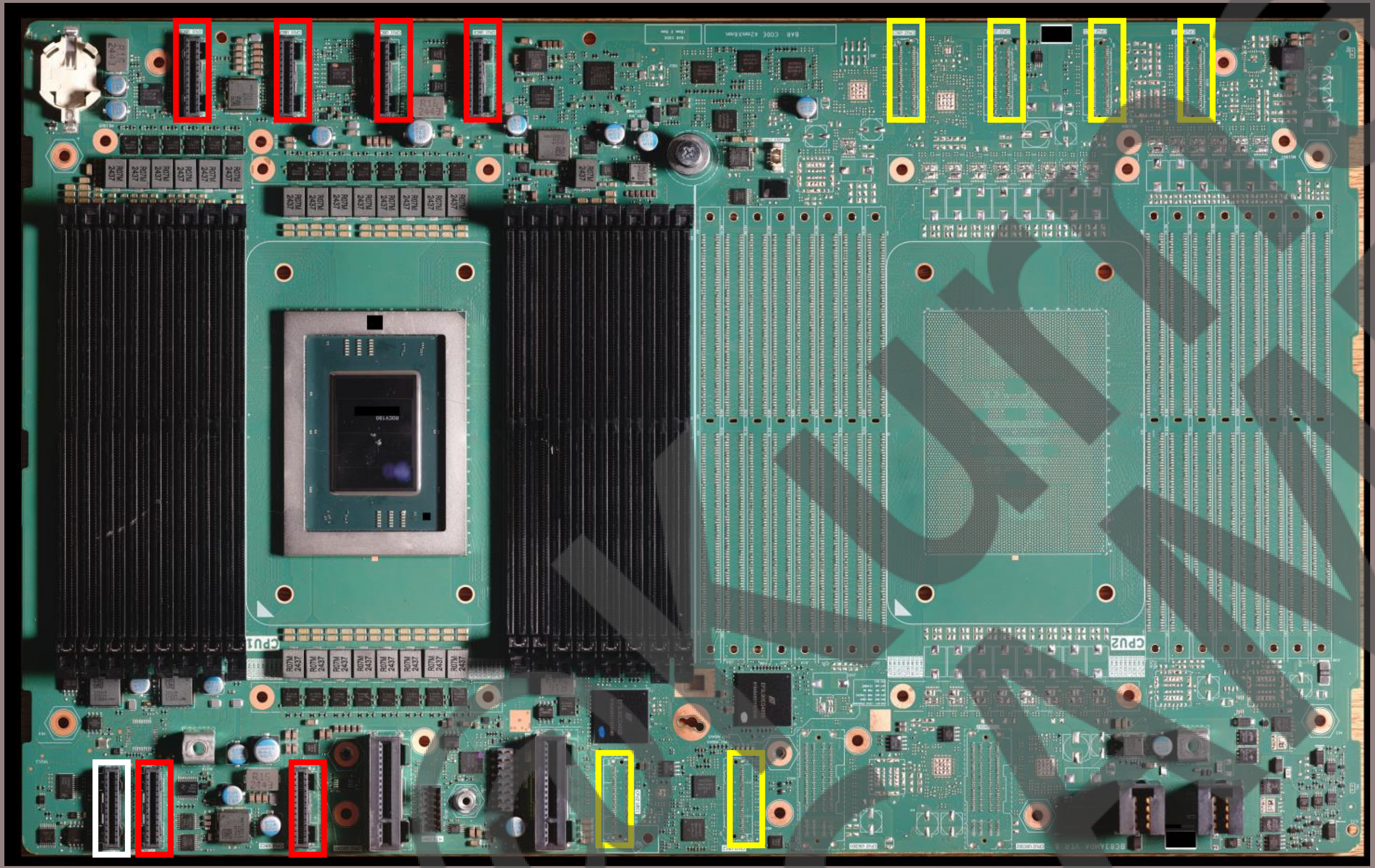
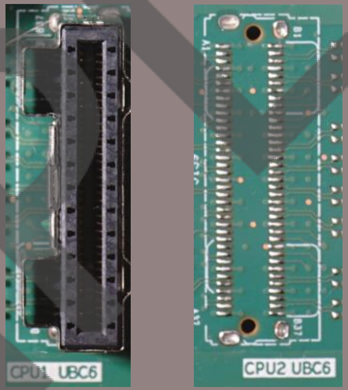
PCB Socket analyze

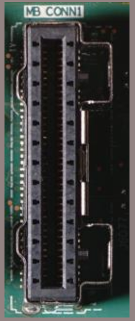


Each CPU have 6 Channel UBC

UBC=Union Bus Connector



UBC x1 =PCIE x8

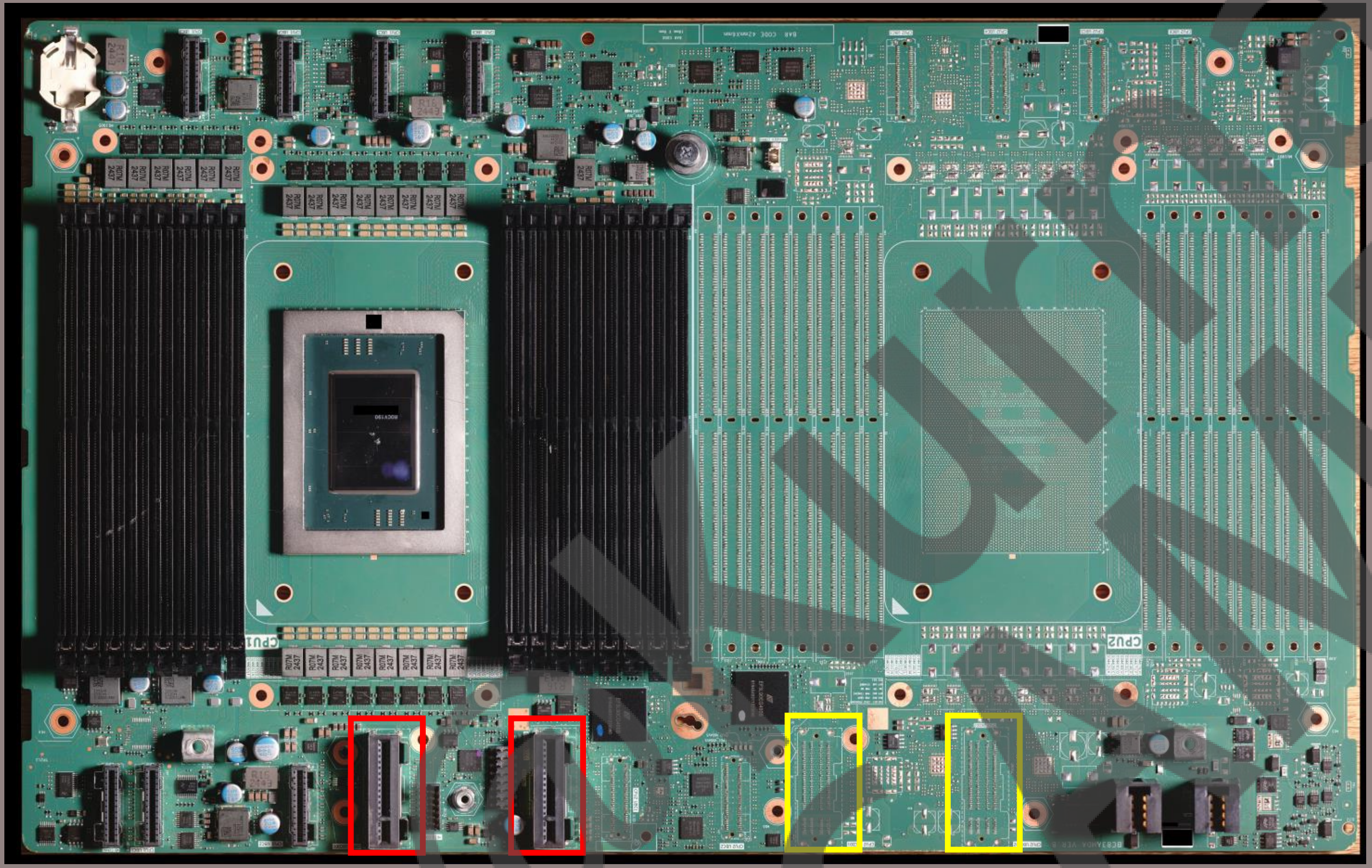


Inter-board management interface between base board and expansion board

UBC Socket

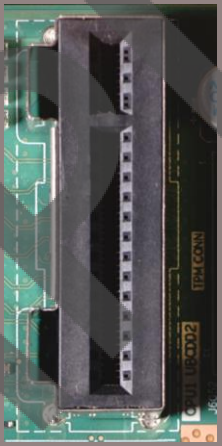
@Kurnal SAMPLE

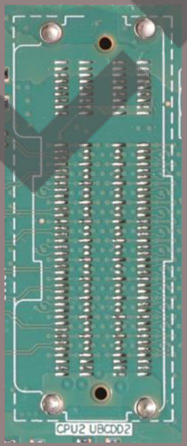
PCB Socket analyze



Each CPU have 2 Channel UBCDD

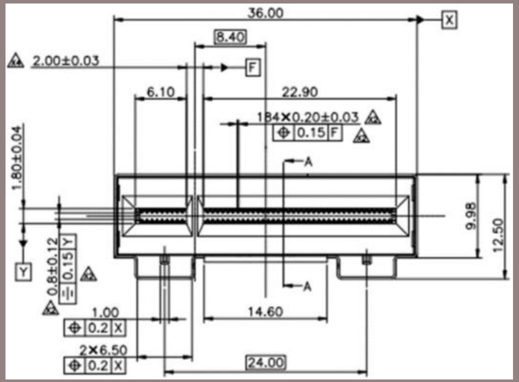
UBCDD=Union Bus Connector Double Density





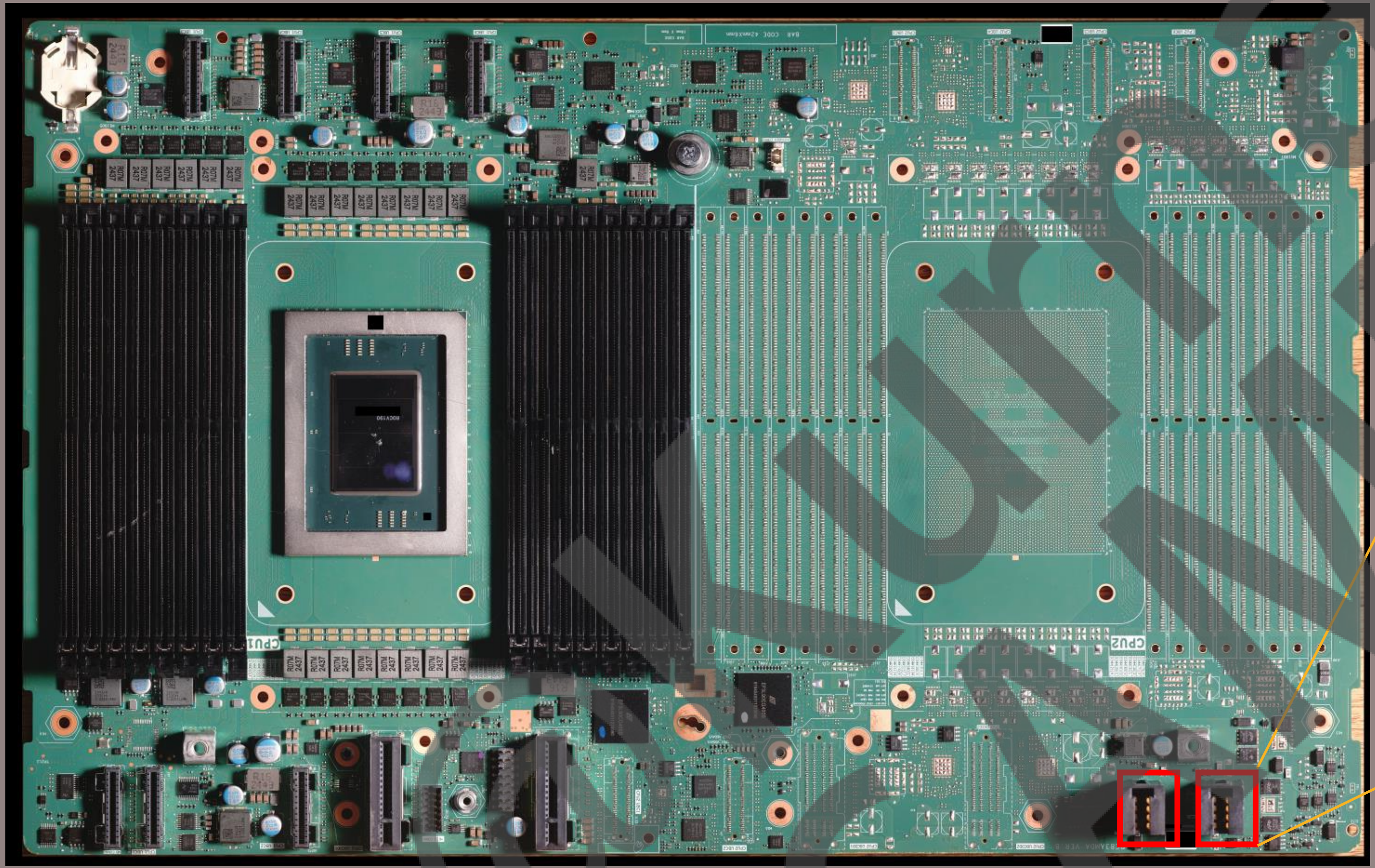
1 UBCDD=PCIE X16

xFusion
CN116107943A

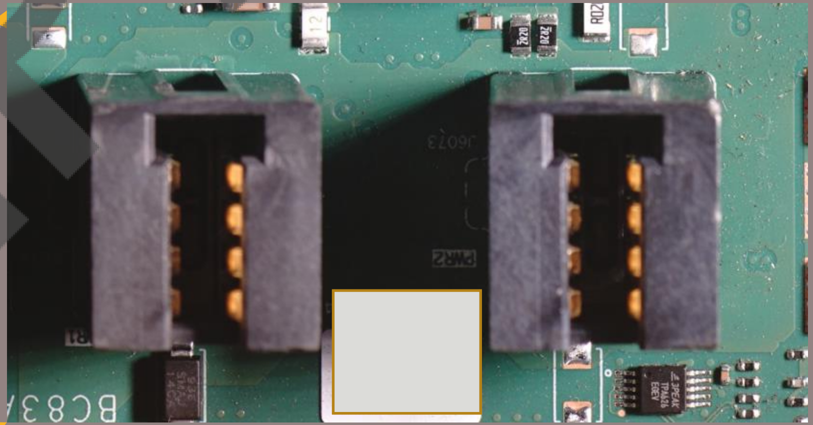


@Kurnal SAMPLE

PCB Socket analyze



The Mother Board have 2 Power Socket



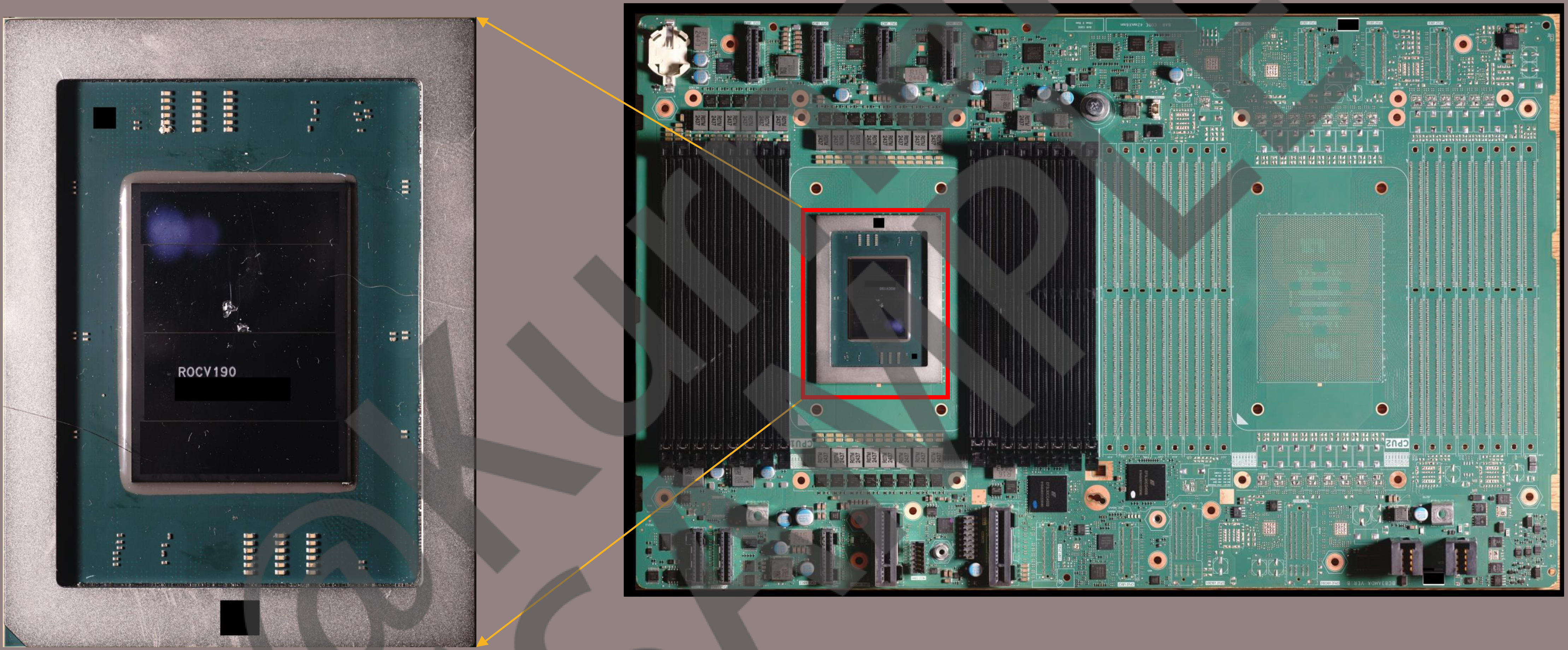
@Kurnal SAMPLE

Chip Package Analyze

Kun Peng 930

@Kurnal SAMPLE

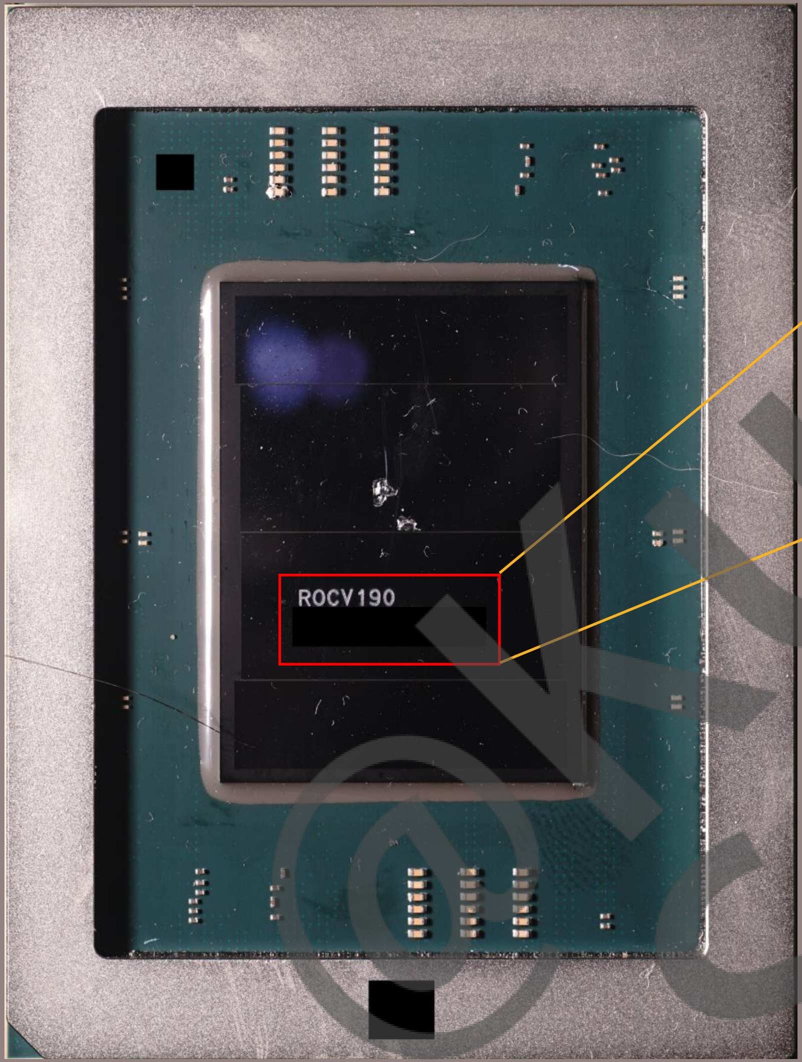
Chip Package Analyze



[redacted]

@Kurnal SAMPLE

Chip Package Analyze



[redacted]

[redacted]

KunPeng 930 Diemark

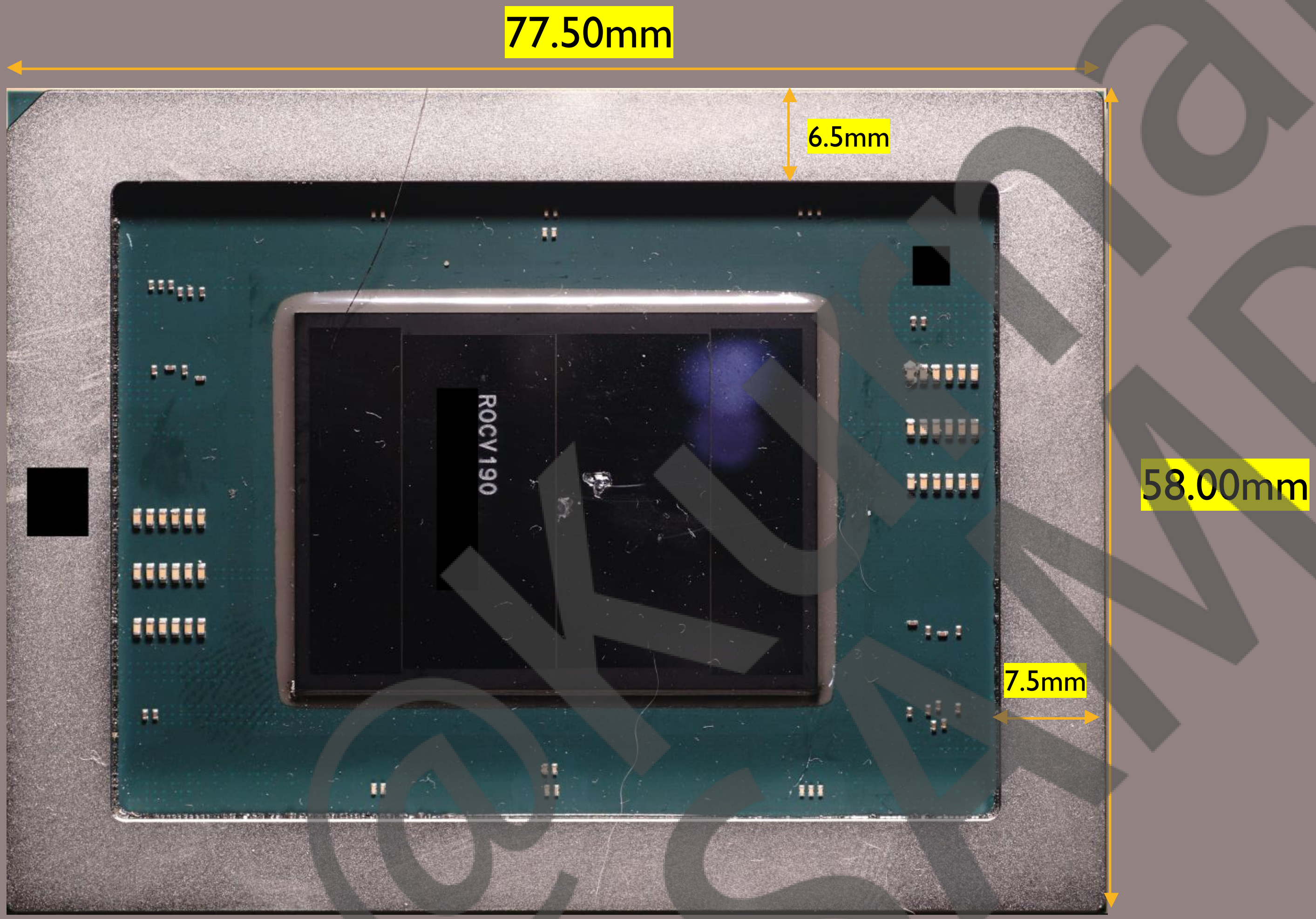
ROCV190 → Chip version number?

[redacted] → Traceability code?

This is an Engineering Sample (ES),so Diemark cannot decode it.

@Kurnal SAMPLE

Chip Package Analyze

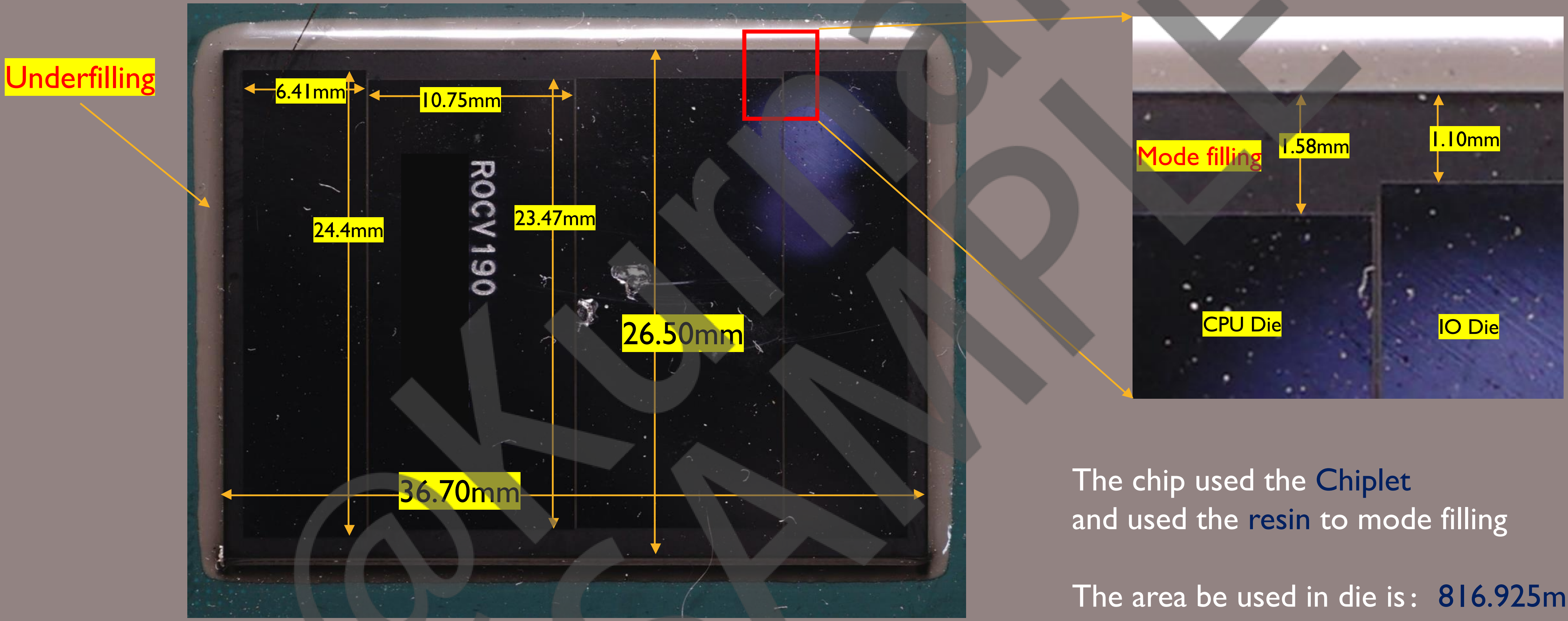


The Package area is 4,495mm2

Have an HIS on the package surface and the area is 1,682.5mm2

@Kurnal SAMPLE

Chip Package Analyze

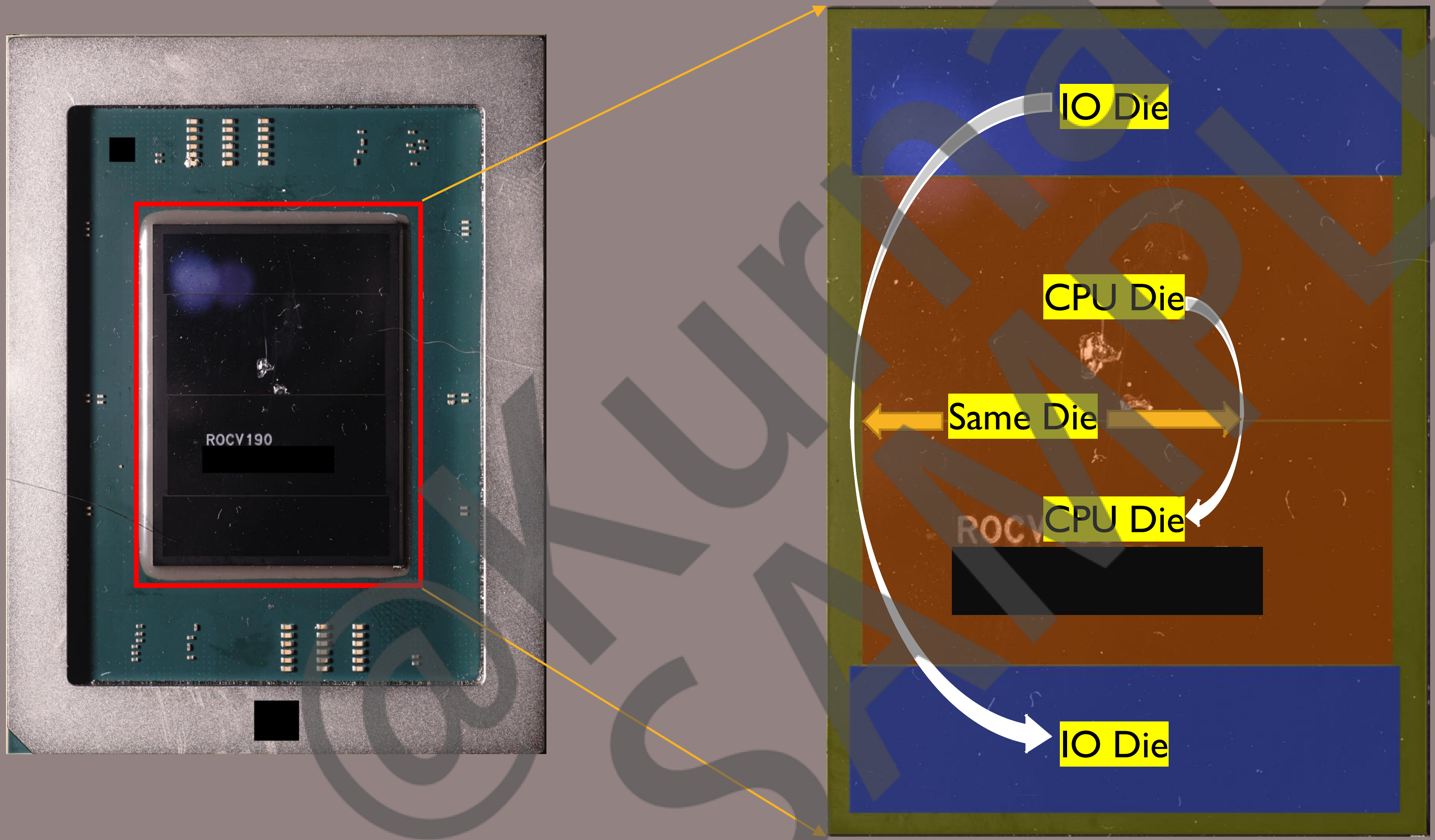


The chip used the Chiplet
and used the resin to mode filling

The area be used in die is： 816.925mm2

@Kurnal SAMPLE

Chip Package Analyze



[redacted]

[redacted]

[redacted]

[redacted]

KP930 have 2 type of die

2 IO Die on both sides
and 2 CPU Die in the middle

@Kurnal SAMPLE

Chip Package Analyze-Decaped

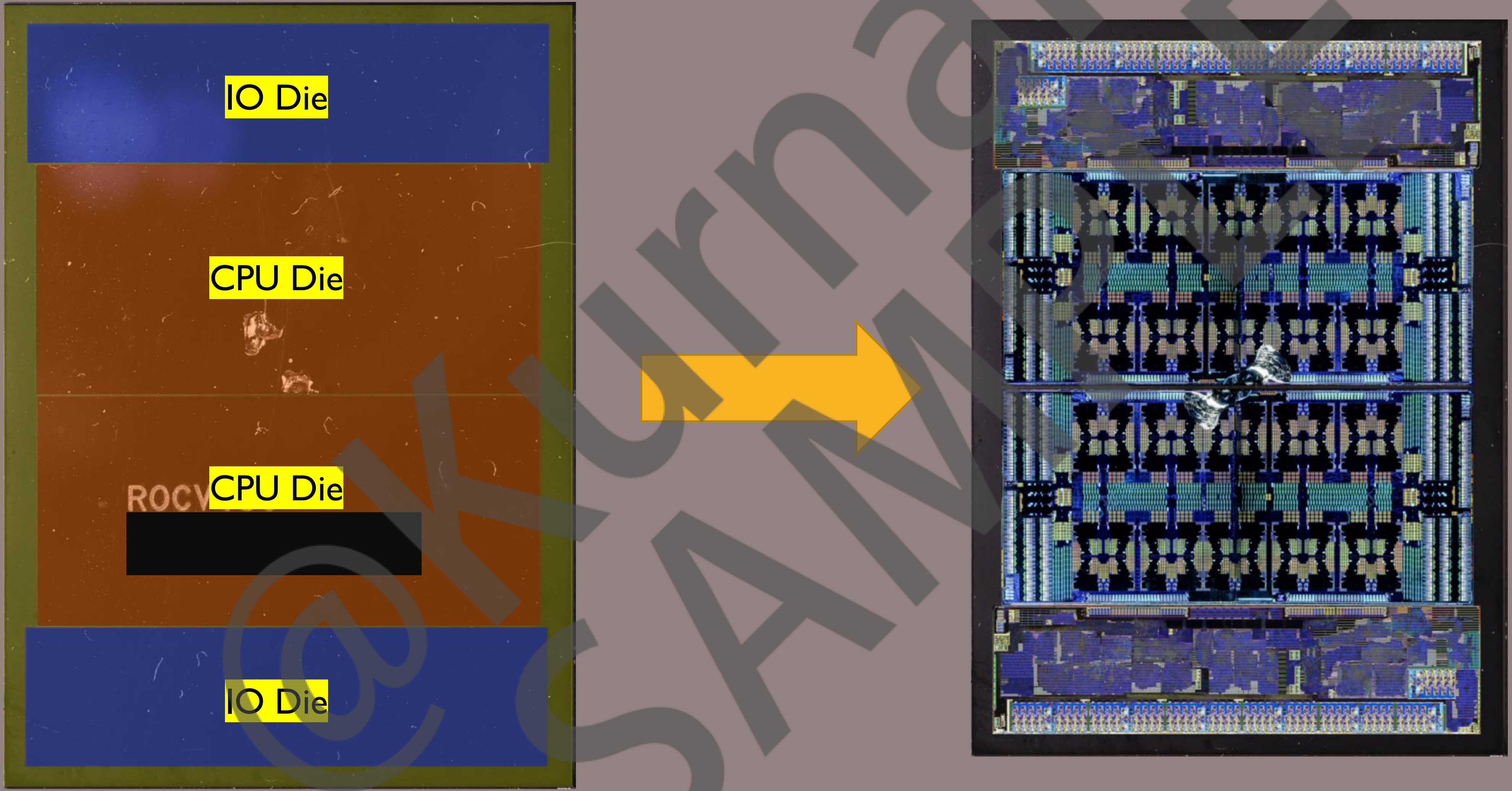
[redacted]

[redacted]

[redacted]

@Kurnal SAMPLE

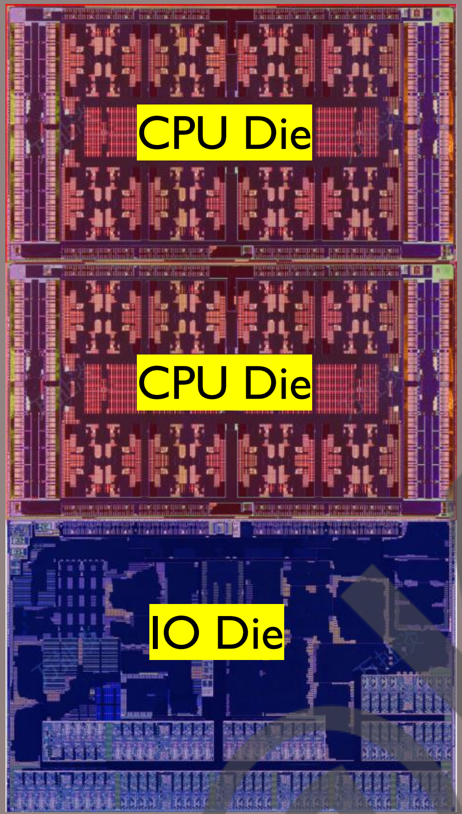
Chip Package Analyze



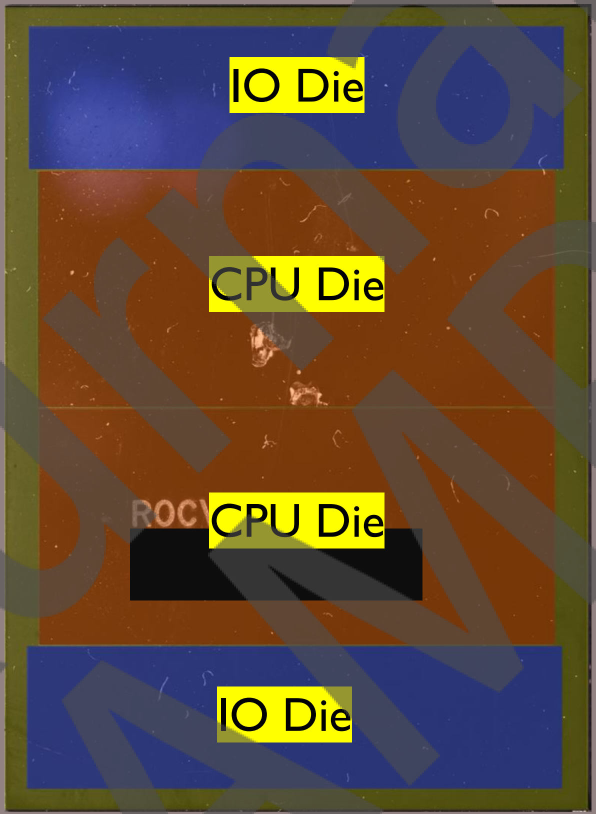
[redacted]

@Kurnal SAMPLE

Chip Package Analyze



KunPeng 920



[redacted]

KunPeng 930

Next Gen

KunPeng 920 have 2 type of die
2 CPU Dies and 1 io Die

KunPeng 930 have 2 type of die
2 CPU Dies and 2 io Dies

KP930 more than KP920 1 io Dies

And the KP930 both die were be new chip

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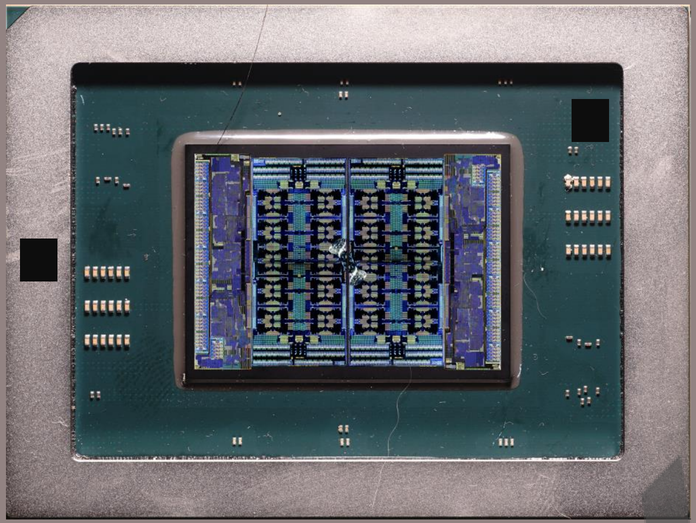
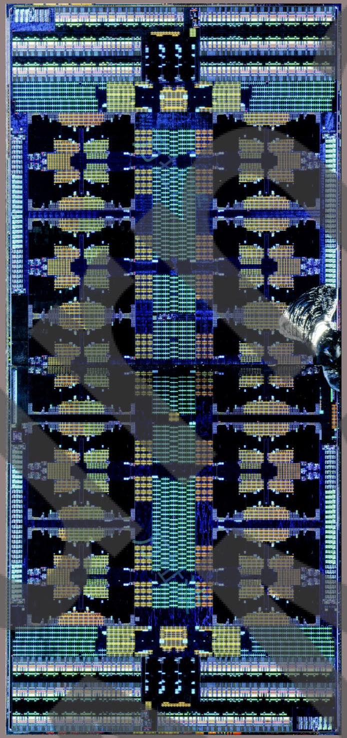
Chip Package Analyze-Decaped



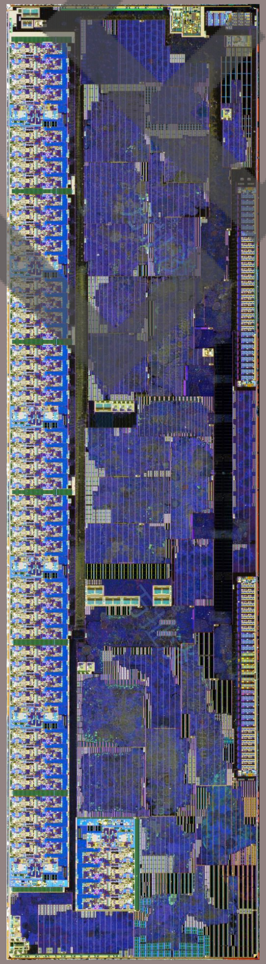
Package size 58.00mm x 77.50mm

Package opening reveals
2 CPU dies
2 IO dies



CPU die

CPU Die x2
Die size:23.47mmx10.75mm



io die

IO Die x2
Die size: 6.41mm x 24.40mm

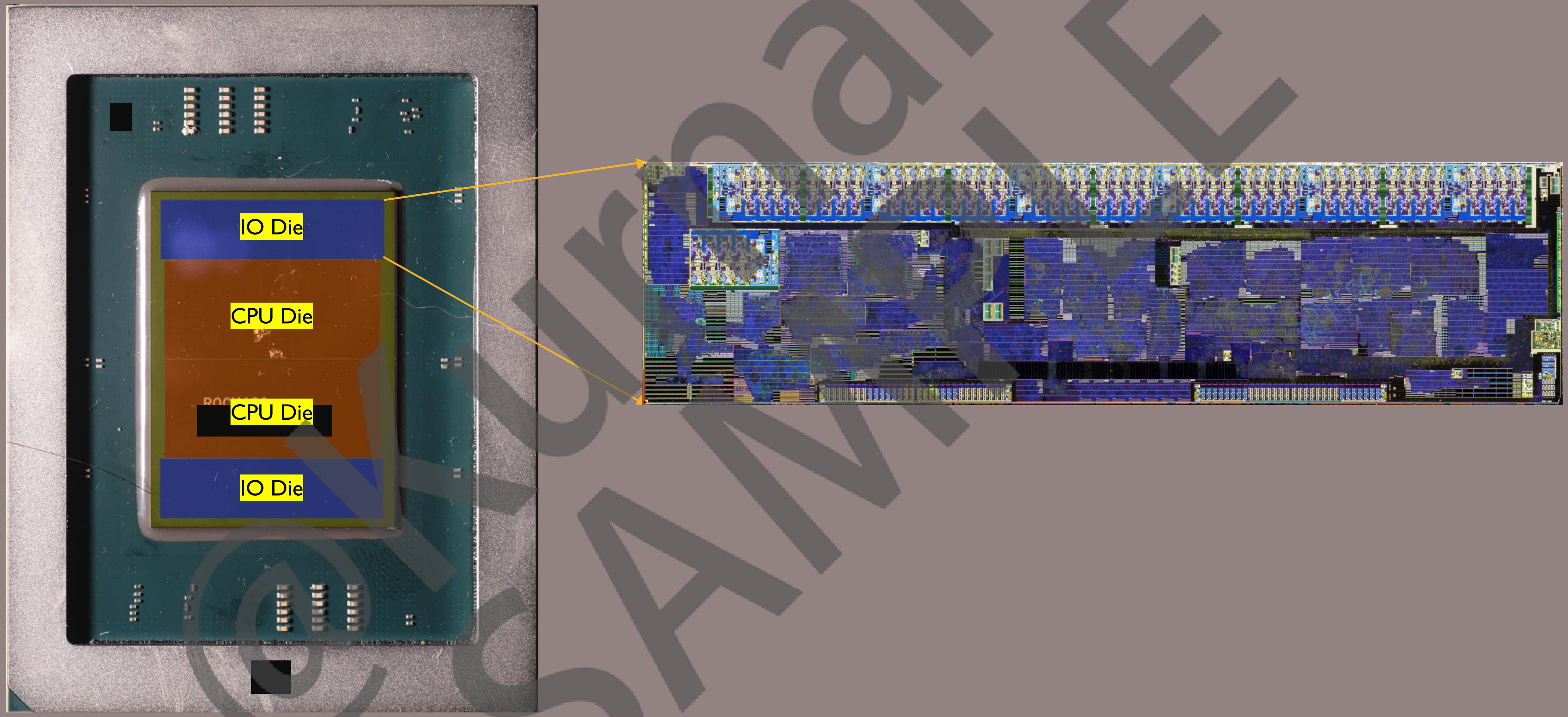
@Kurnal SAMPLE

io Die Analyze

Kun Peng 930

@Kurnal SAMPLE

io Die Analyze



[redacted]

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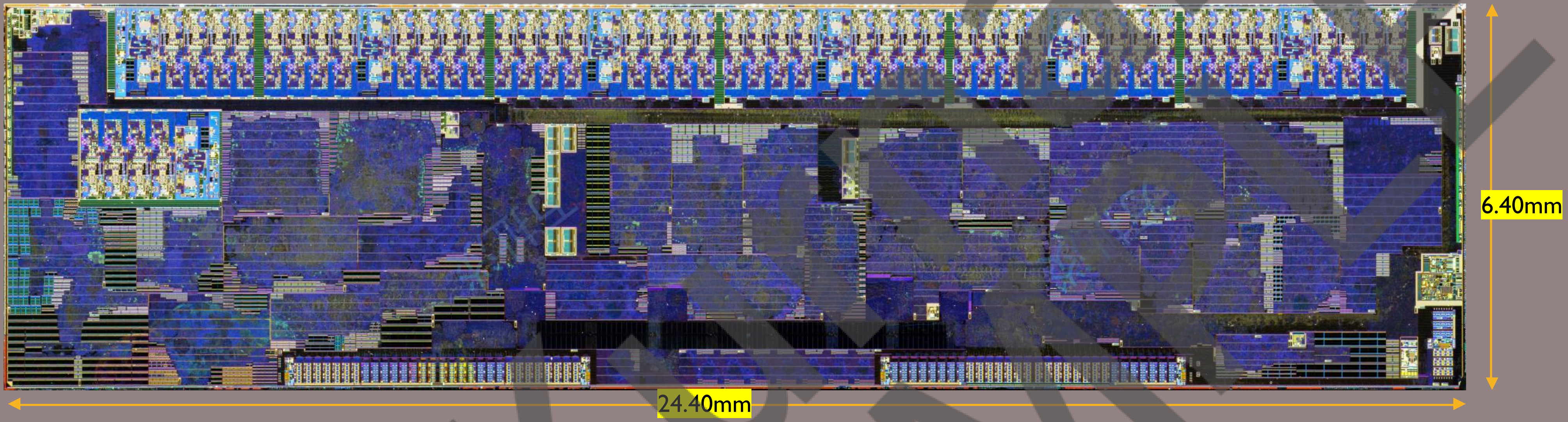
[redacted]

@Kurnal SAMPLE

io Die Analyze



IO Die Length :	24.40mm
IO Die Width :	6.41mm
IO Die Thickness :	700um
IO Die size :	156.404mm2
Die Aspect Ratio:	3.8125:1

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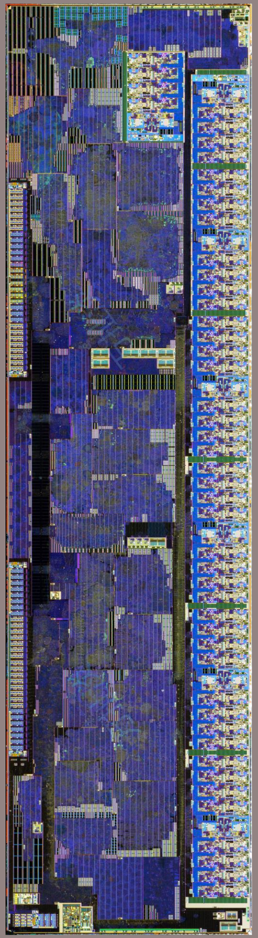
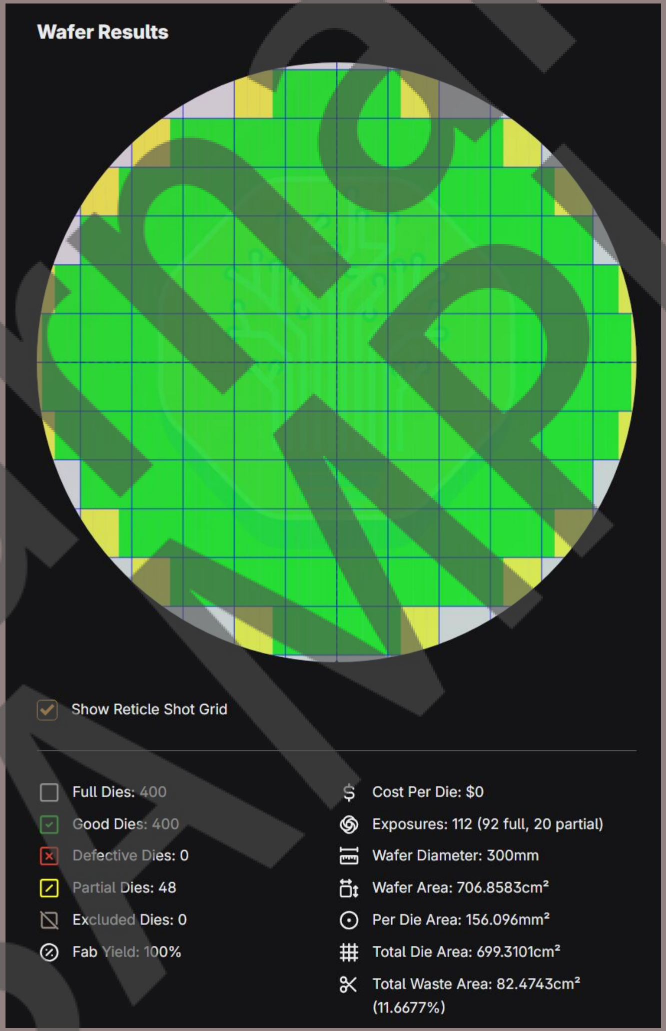
io Die Analyze-Die Per Wafer



io Die
Package size: 24.40mmx6.41mm

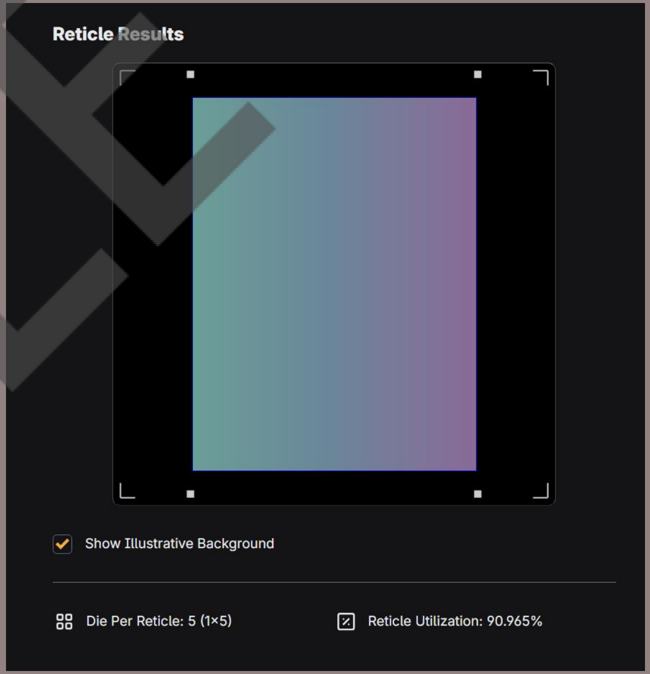
Die Per Wafer 400
Die Per Mask 5:1



Wafer Results

☑ Show Reticle Shot Grid

Full Dies: 400	Cost Per Die: $0
Good Dies: 400	Exposures: 112 (92 full, 20 partial)
Defective Dies: 0	Wafer Diameter: 300mm
Partial Dies: 48	Wafer Area: 706.8583cm²
Excluded Dies: 0	Per Die Area: 156.096mm²
Fab Yield: 100%	Total Die Area: 699.3101cm²
	Total Waste Area: 82.4743cm² (11.6677%)



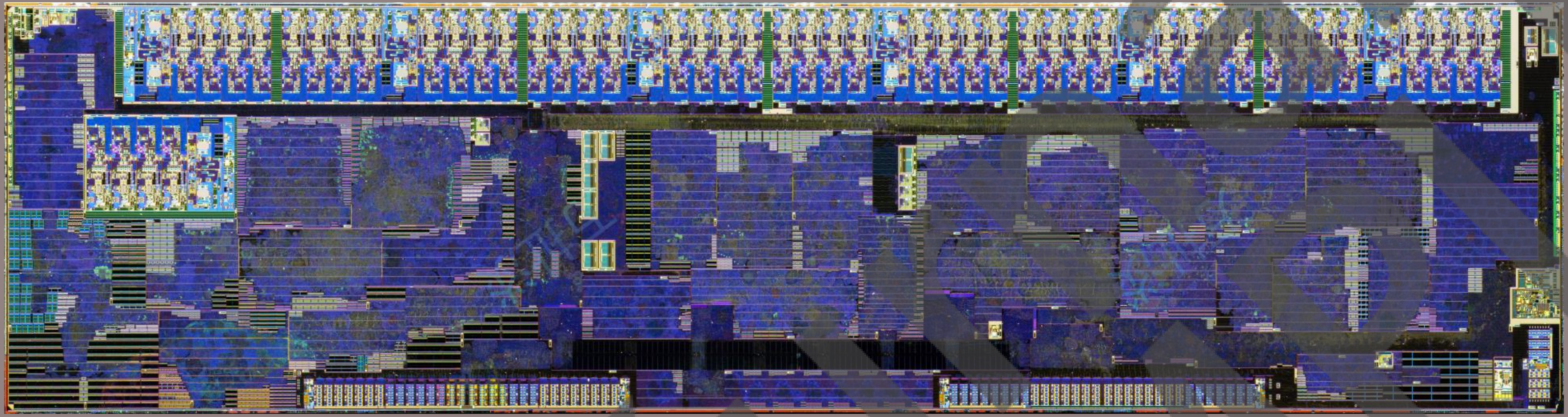
Reticle Results

☑ Show Illustrative Background

Die Per Reticle: 5 (1×5)
Reticle Utilization: 90.965%

@Kurnal SAMPLE

io Die Analyze



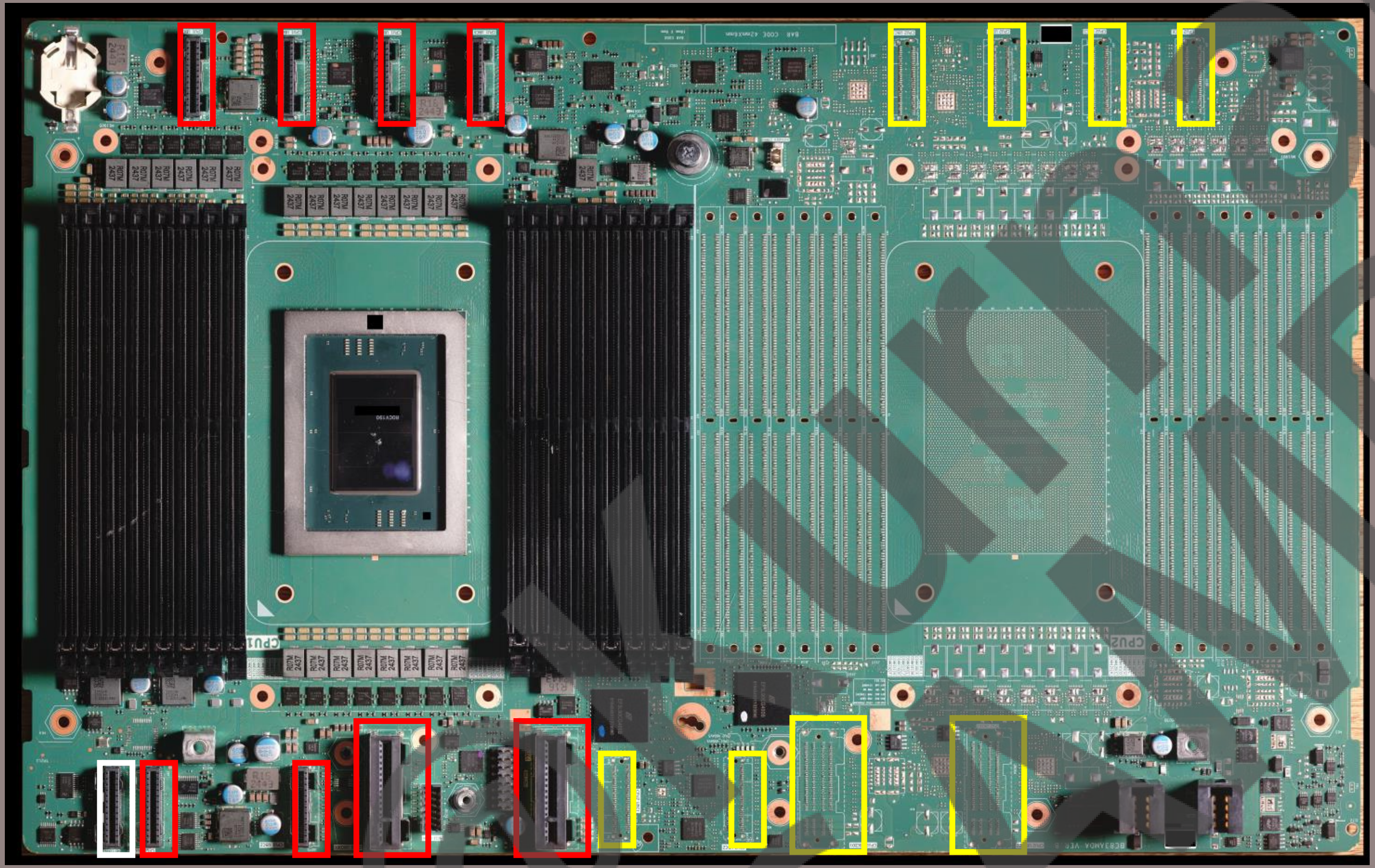
On this IOD, there are a total of PCIE 48 lines
And 2 sets of Die to Die interfaces

[redacted]

The full chip has 2 IODs,
totaling PCIE 96 lines

@Kurnal
SAMPLE

io Die Analyze


[redacted]

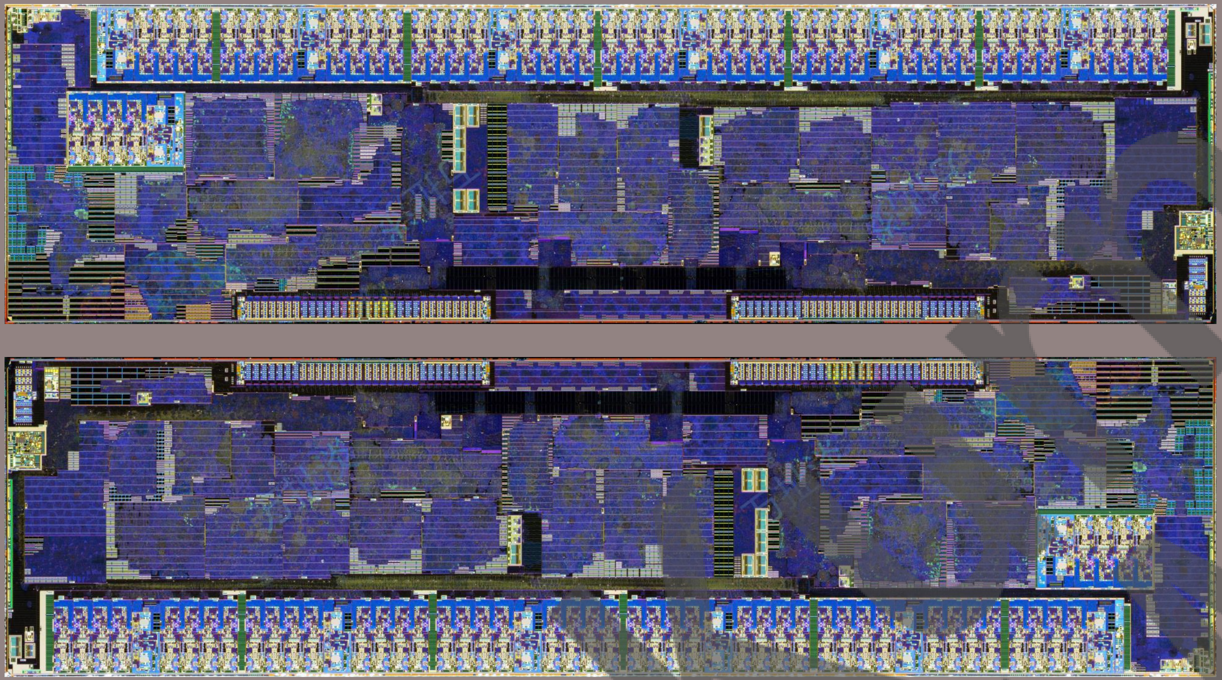
[redacted]

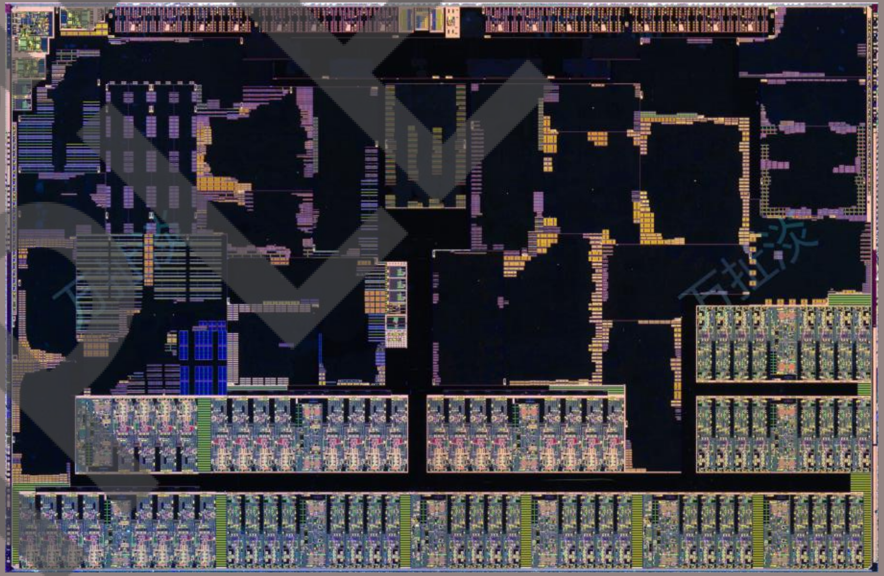
On this motherboard
each CPU has 2 x16 UBCDDs and 6 x8 UBCs,totaling 80 lines.
The remaining PCIE x16 is wasted or used for interconnection.

The full chip has 2 IODs,
totaling PCIE 96 lines

@Kurnal
SAMPLE

KunPeng 920 iod vs KunPeng 930 iod





KunPeng 930
IO Die size： 156.404mm2 x2
PCIE Channel: x48
Full chip PCIE channel: x96

KunPeng 920
IO Die size： 172.306mm2
PCIE Channel: x68
Full chip PCIE channel: x68

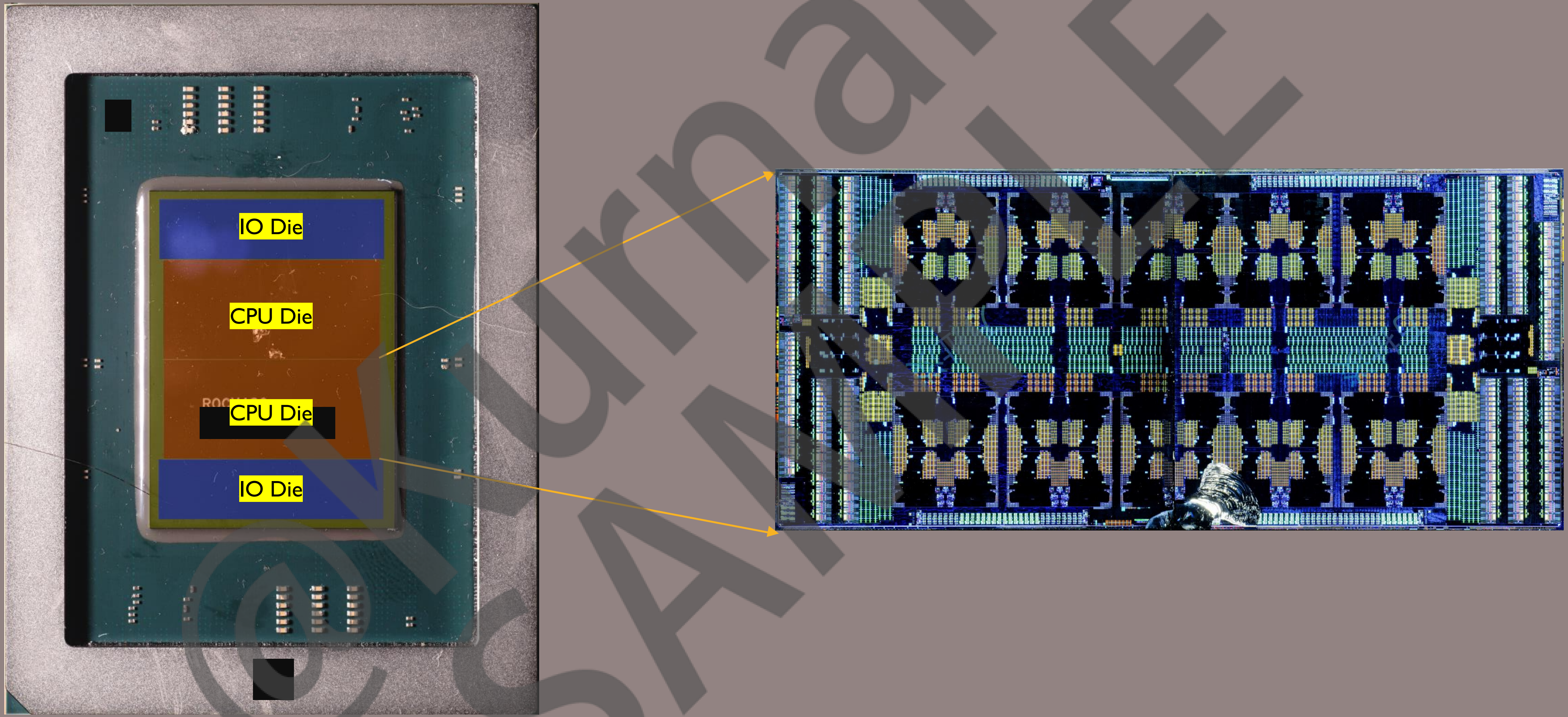
@Kurnal SAMPLE

CPU Die Analyze

Kun Peng 930

@Kurnal SAMPLE

CPU Die Analyze



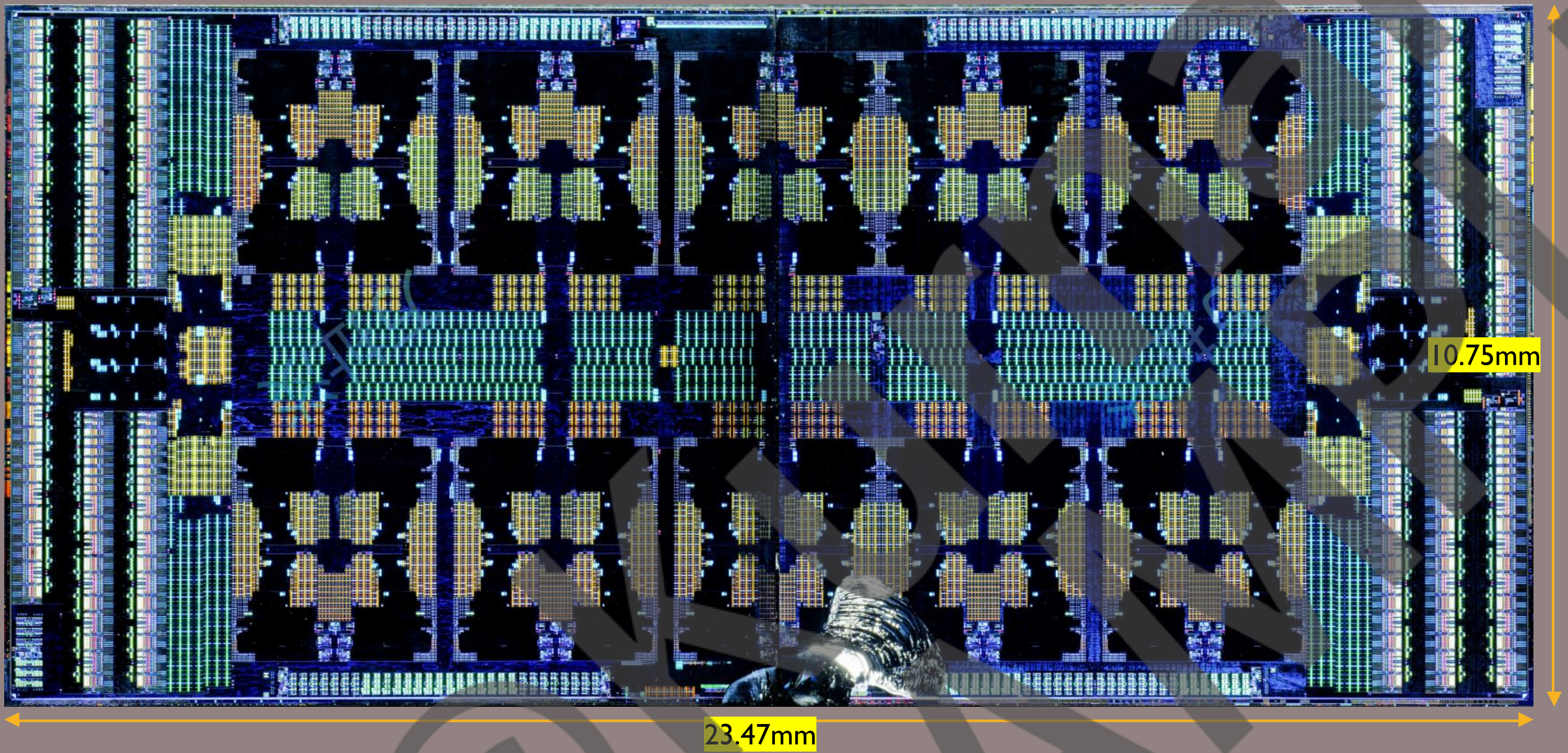
[redacted]

[redacted]

[redacted]

@Kurnal SAMPLE

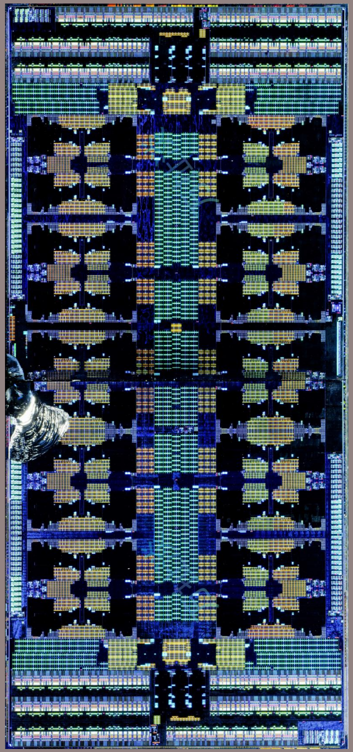
CPU Die Analyze



CPU Die Length :	23.47mm
CPU Die Width :	10.75mm
CPU Die Thickness :	700um
CPU Die size :	252.30mm2
Die Aspect Ratio:	2.183:1

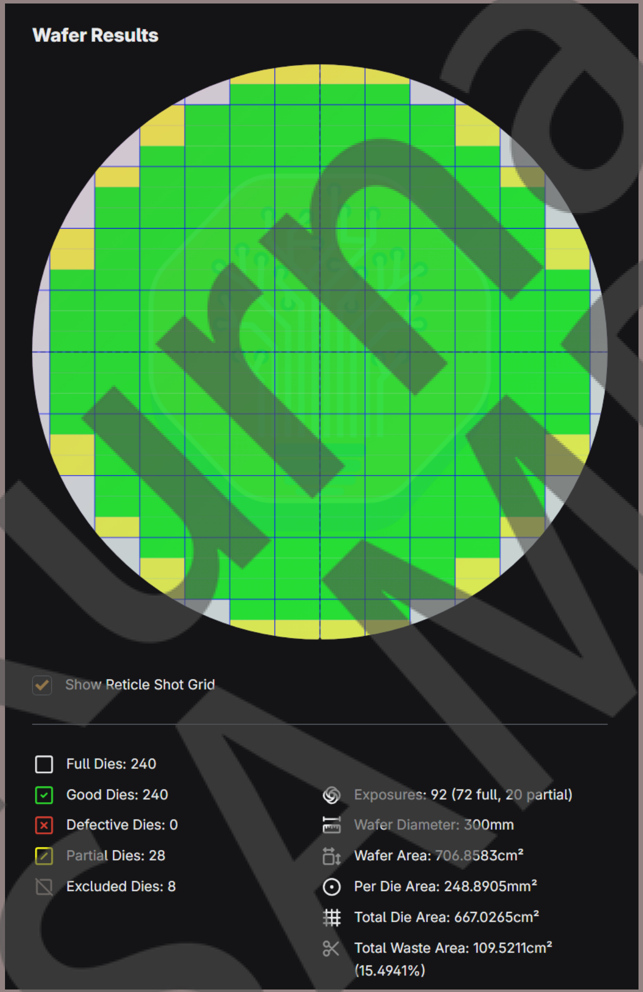
@Kurnal SAMPLE

CPU Die Analyze-Die Per Wafer



CPU Die
Diesize: 23.47mmx10.75mm

Die Per Wafer 240
Die Per Mask 3:1

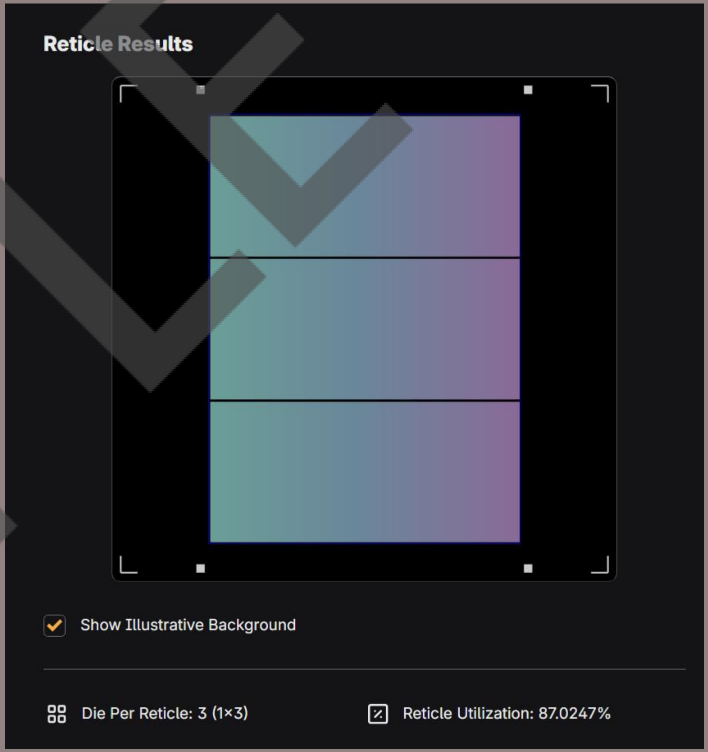


Wafer Results

☑ Show Reticle Shot Grid

☐ Full Dies: 240
☑ Good Dies: 240
☒ Defective Dies: 0
☐ Partial Dies: 28
☐ Excluded Dies: 8

Exposures: 92 (72 full, 20 partial)
Wafer Diameter: 300mm
Wafer Area: 706.8583cm²
Per Die Area: 248.8905mm²
Total Die Area: 667.0265cm²
Total Waste Area: 109.5211cm² (15.4941%)



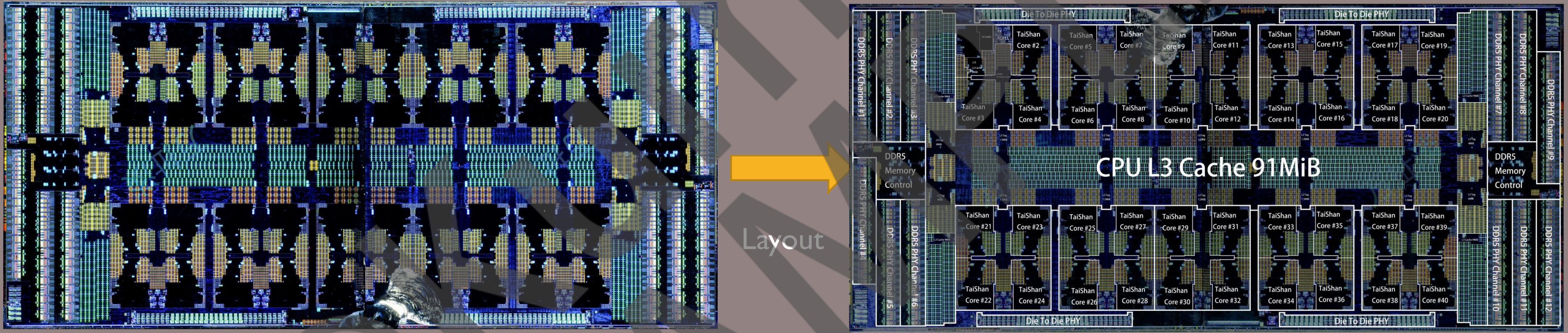
Reticle Results

☑ Show Illustrative Background

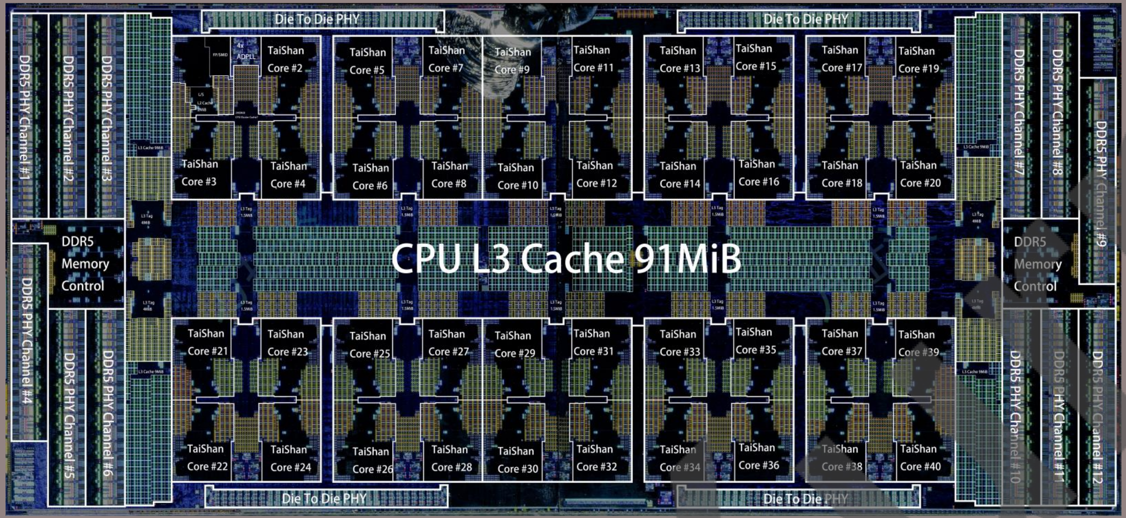
Die Per Reticle: 3 (1×3)
Reticle Utilization: 87.0247%

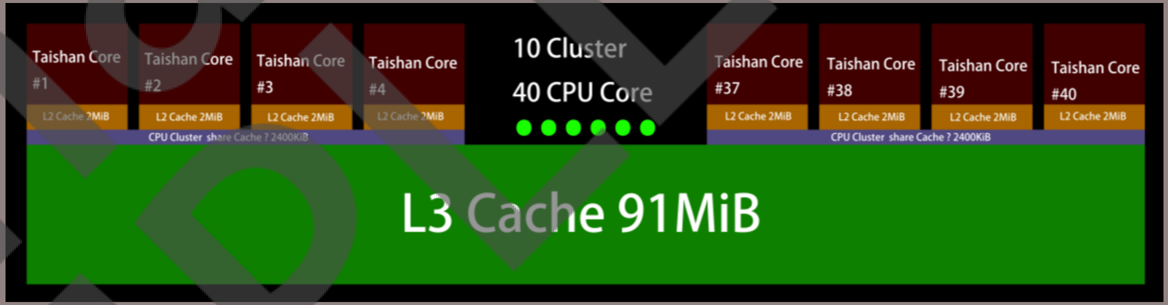
@Kurnal SAMPLE

CPU Die Analyze



CPU Die Analyze





CPU Core Nb	40
CPU Cluster Nb	10
CPU Core Per Cluster	4
CPU L2 Cache	2MiB(Only)
CPU L3 Cache	91MiB(40core shared)
CPU Core Per L3 Cache	2.275MiB

Memory Channel Nb: 12

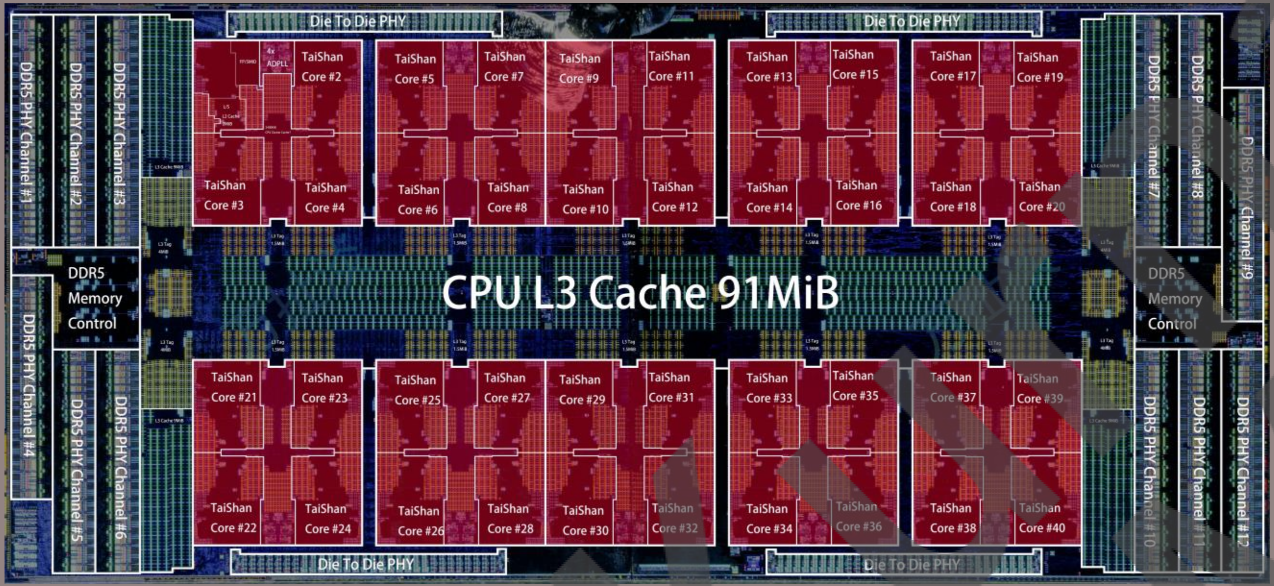
@Kurnal SAMPLE

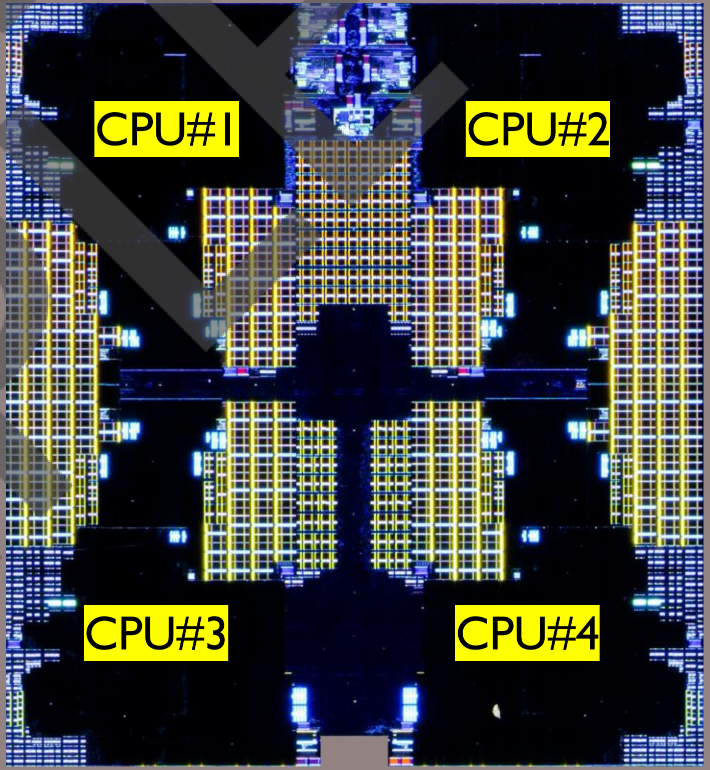
CPU Die Analyze

CPU Core

@Kurnal SAMPLE

CPU Die Analyze-CPU Cluster



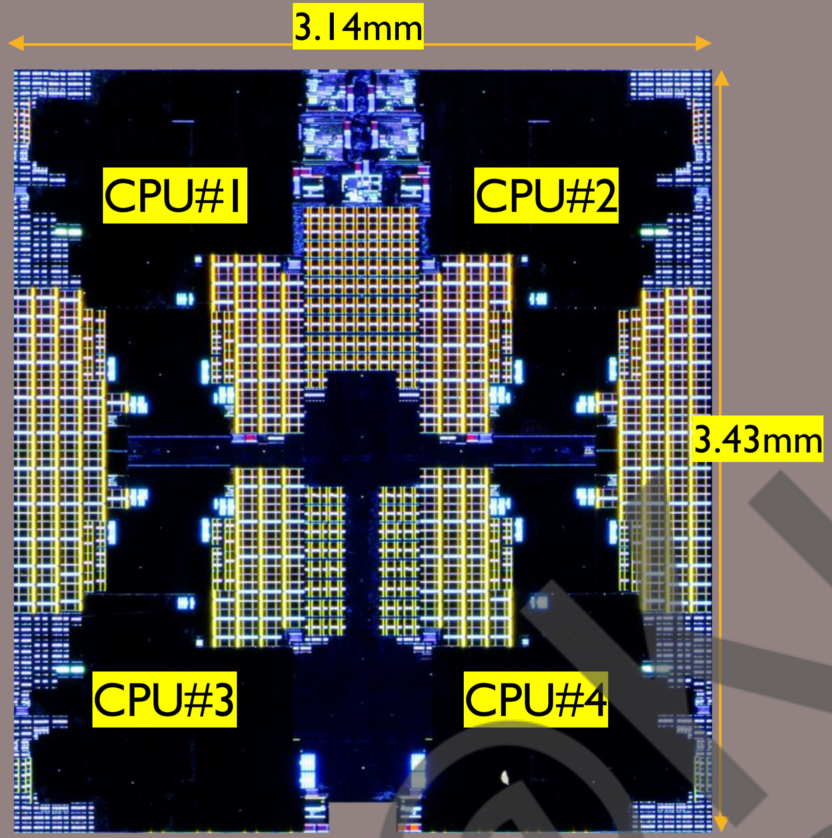


KP930 CPU Cluster

Each CPU Die has 10 CPU clusters
Each Cluster has 4 Taishan cores
So each CPU Die have 40 CPU Cores
And KunPeng 930 have 80 CPU Cores

@Kurnal SAMPLE

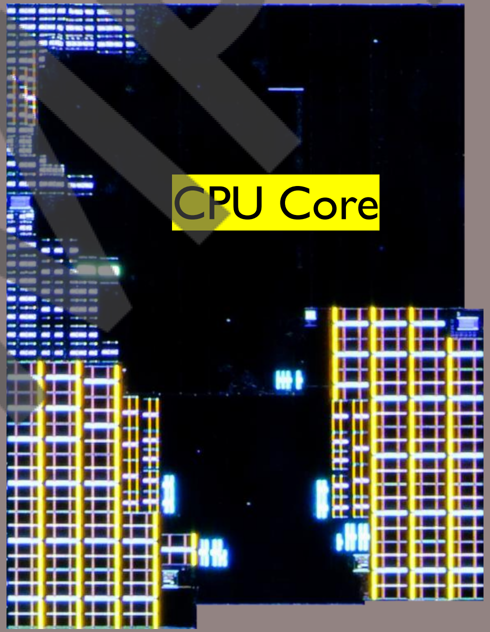
CPU Die Analyze-CPU Cluster



KP930 CPU Cluster

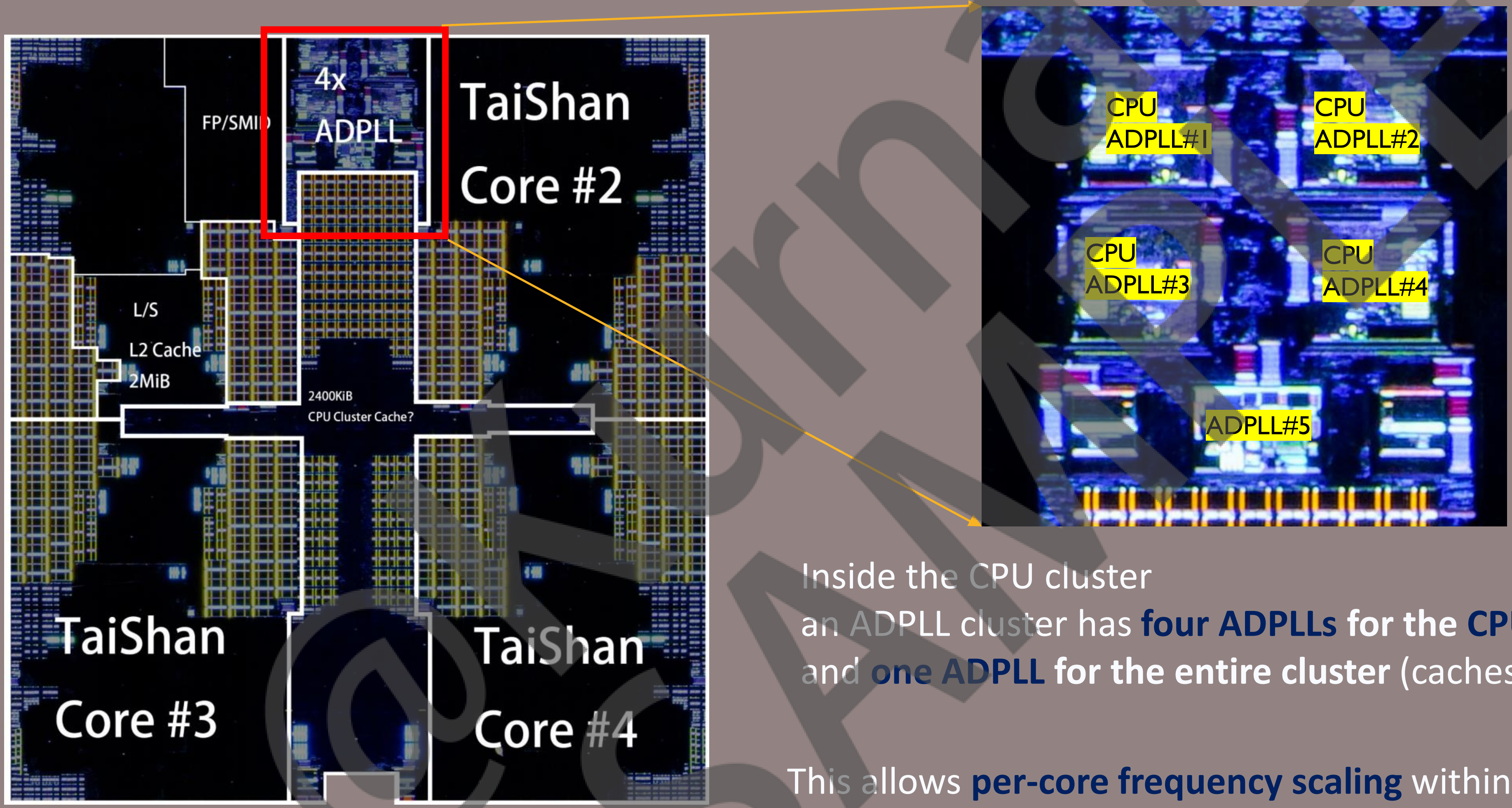
Each CPU cluster has 4 CPU cores,
but the Freq and Arch cannot be confirmed

CPU Cluster area : 10.77mm2



@Kurnal SAMPLE

CPU Die Analyze-CPU Cluster



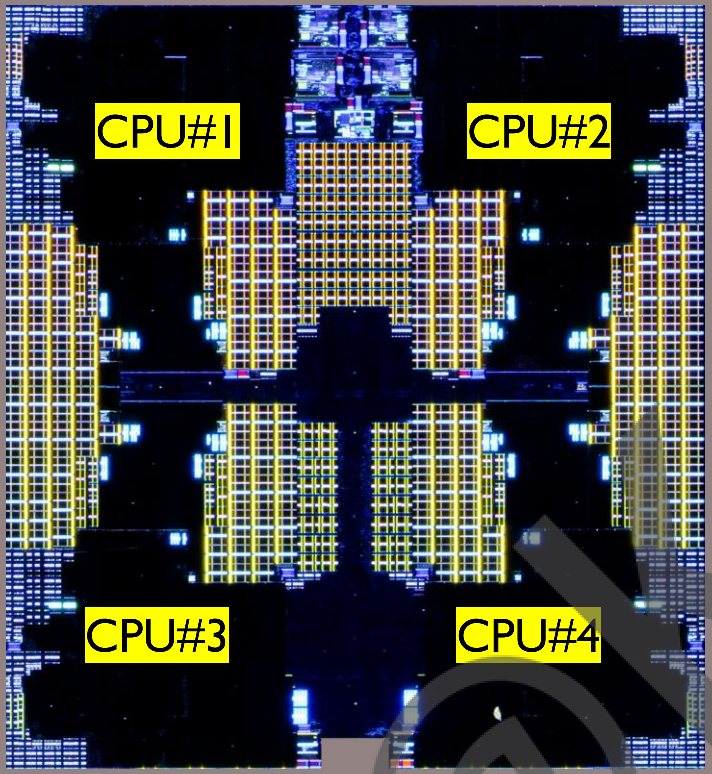
KP930 CPU Cluster

Inside the CPU cluster
an ADPLL cluster has **four ADPLLs for the CPU cores**
and **one ADPLL for the entire cluster** (caches, etc.).

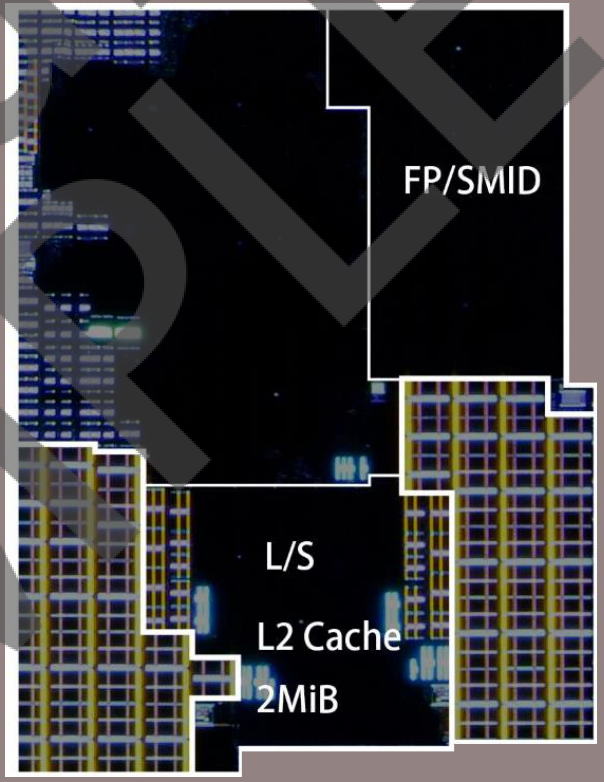
This allows **per-core frequency scaling** within the CPU cluster.

@Kurnal SAMPLE

CPU Die Analyze-CPU Core



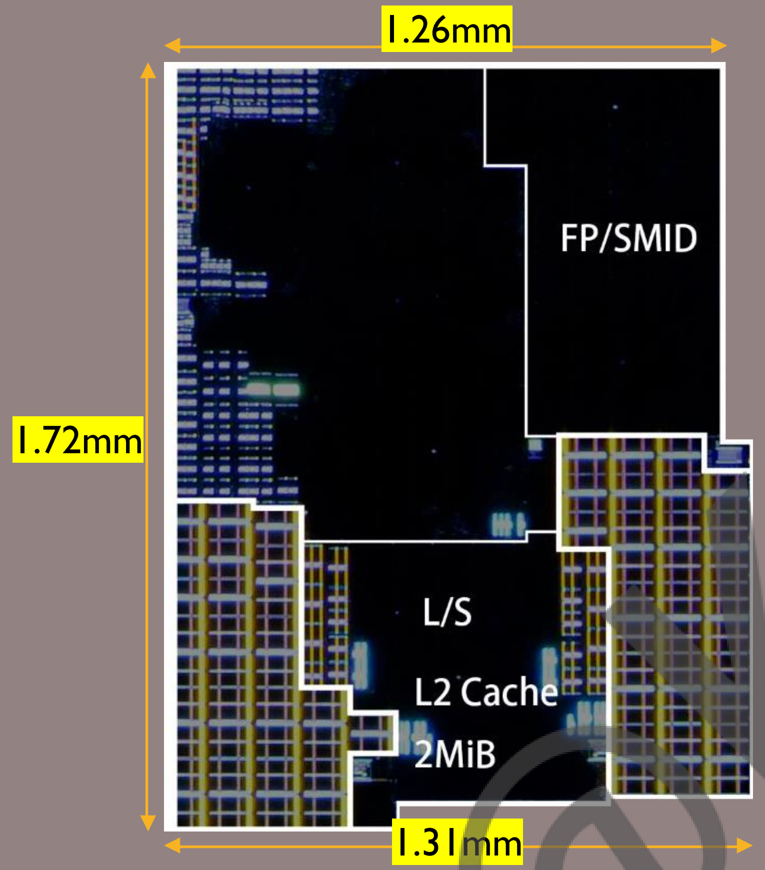
KP930 CPU Cluster



KP930 CPU Core

@Kurnal SAMPLE

CPU Die Analyze-CPU Core



KP930 CPU Core

I cannot confirm its detailed CPU Arch
but it is suspected to be the new Taishan CPU core
with FPU and 2MiB L2 Cache.

CPU Core area :	2.154mm2
CPU FPU area:	0.40mm2
CPU without L2 L/S area:	1.23mm2
CPU L2 Size:	2048KiB
CPU L2 area:	0.54mm2(0.27mm2 x2)
CPU L2 Macro Density:	3,792.59KiB/mm2

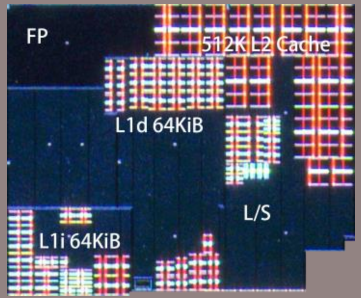
@Kurnal SAMPLE

CPU Core VS

CPU Core VS

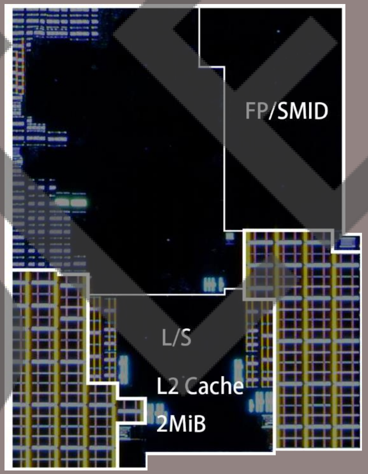
@Kurnal SAMPLE

VS old KunPeng



KunPeng 920

Next Gen KunPeng



KunPeng 930

CPU Core area：	1.437mm2
CPU FPU area:	0.16mm2
CPU without L2 L/S area:	0.865mm2
CPU L2 Size:	512KiB
CPU L2 area:	0.286mm2
CPU L2 Macro Density:	1,790.21KiB/mm2

Double

CPU Core area：	2.154mm2
CPU FPU area:	0.40mm2
CPU without L2 L/S area:	1.23mm2
CPU L2 Size:	2048KiB
CPU L2 area:	0.54mm2(0.27mm2 x2)
CPU L2 Macro Density:	3,792.59KiB/mm2

@Kurnal
SAMPLE

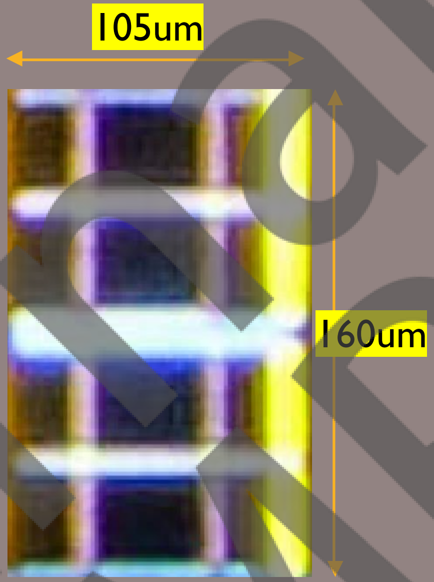
CPU Die Analyze

L2/L3 Cache SRAM Density

@Kurnal
SAMPLE

CPU Die SRAM Density-L2 Cache

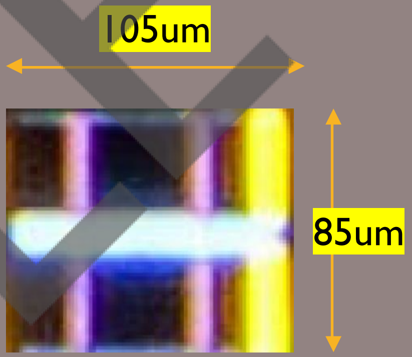
KP930 CPU Core



L3 Cache Sram Block

Size: 64KiB

0.0168mm2/64KiB
3,809.52KiB/mm2



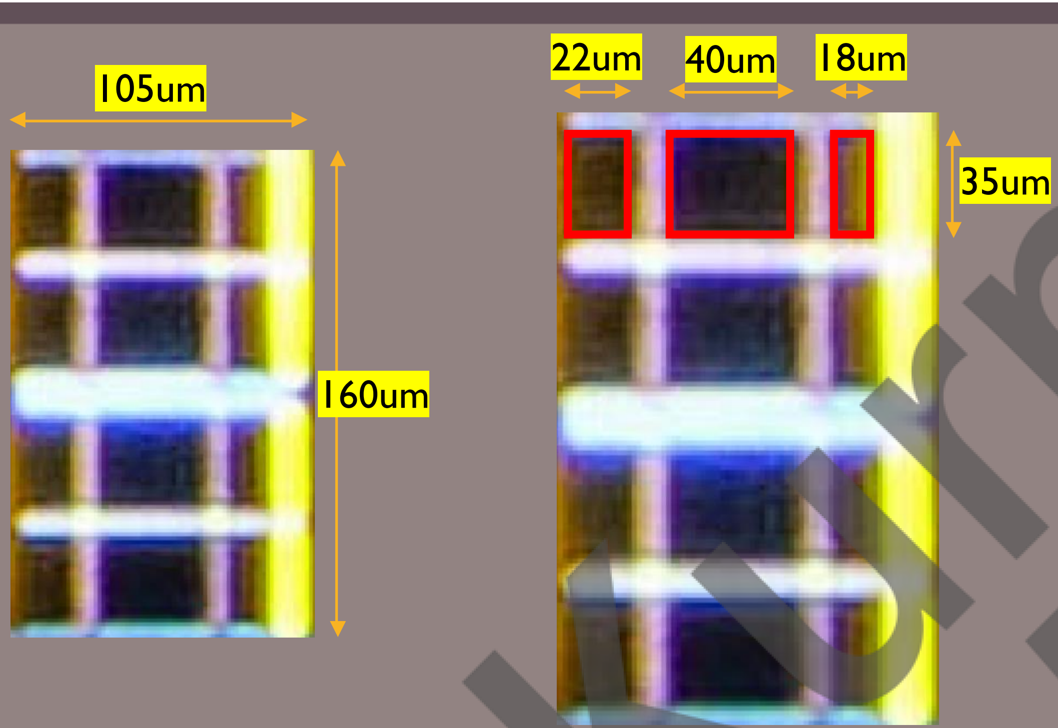
L3 Cache Sram Block

Size: 32KiB

0.008925mm2/32KiB
3,585.43KiB/mm2

@Kurnal SAMPLE

CPU Die SRAM Density-L2 Cache



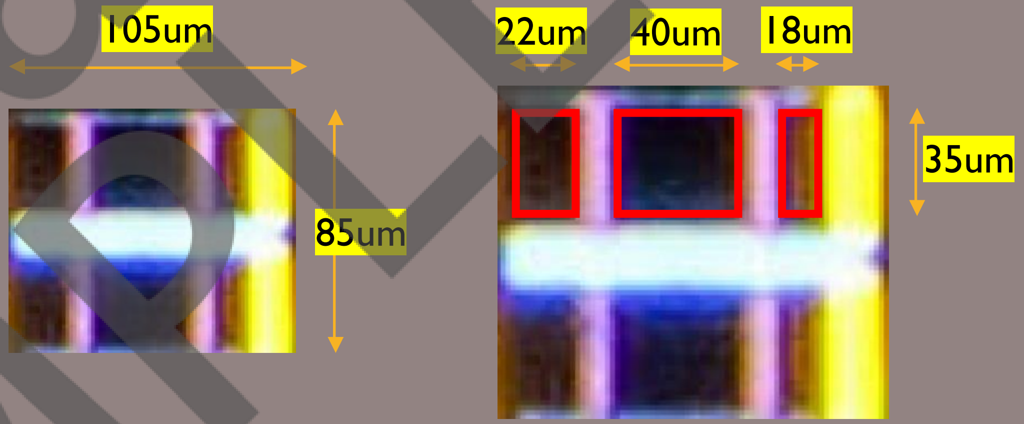
L3 Cache Sram Block

Size: 64KiB

0.0168mm2/64KiB
3,809.52KiB/mm2

Sram bit cell by used: 11,200um2
Proportion: 66.67%

Sram Bit cell Density: 0.02136um2/bit



L3 Cache Sram Block

Size: 32KiB

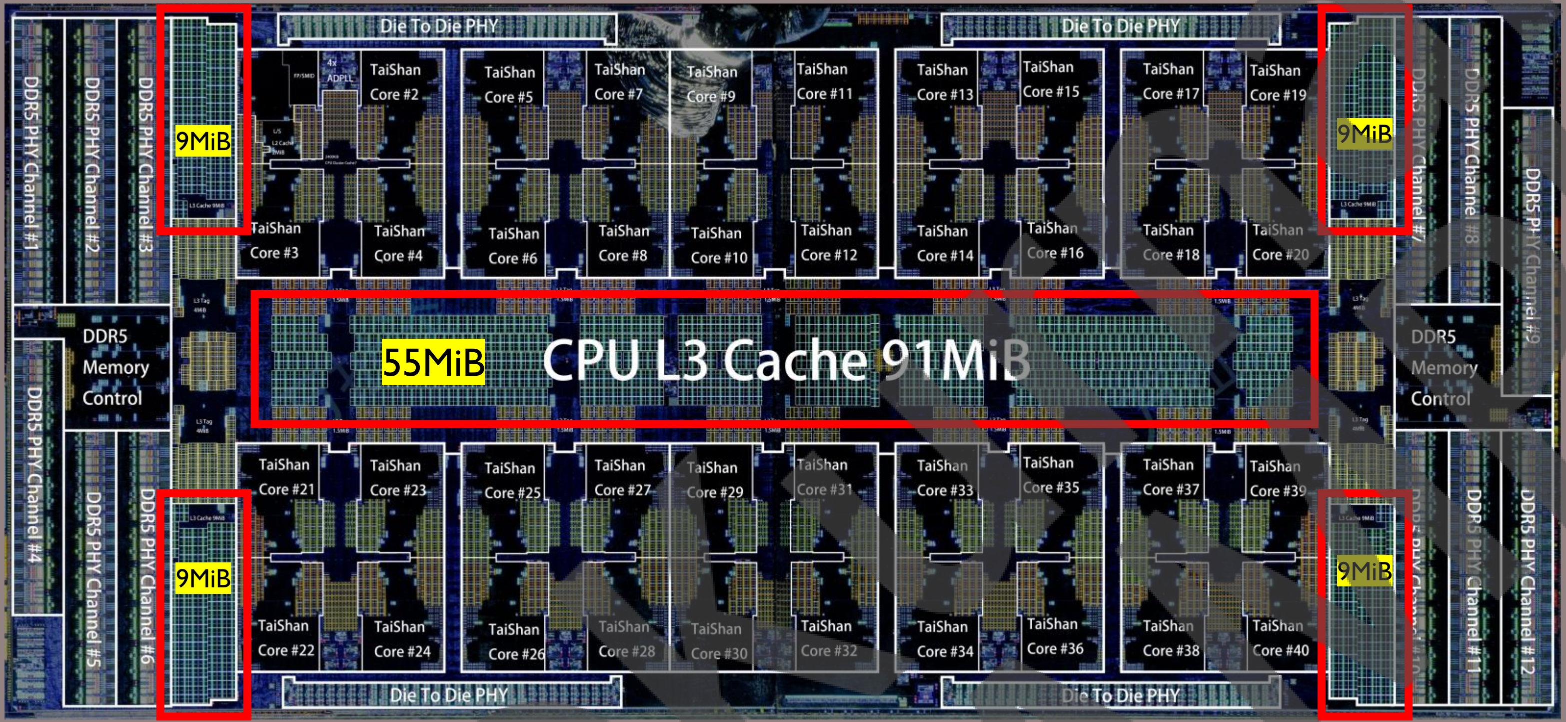
0.008925mm2/32KiB
3,585.43KiB/mm2

Sram bit cell by used: 5600um2
Proportion: 62.75%

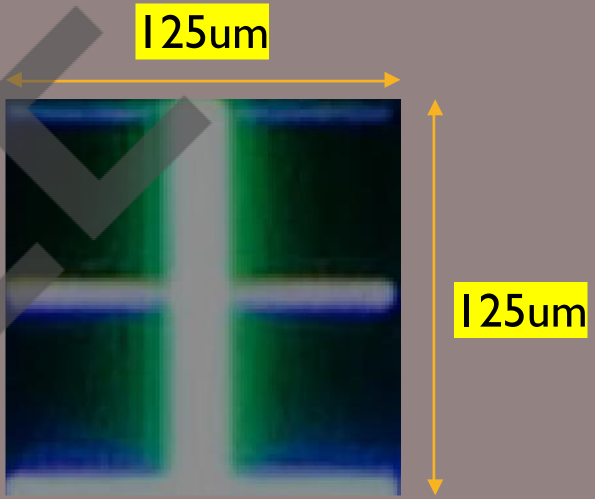
Sram Bit cell Density: 0.02136um2/bit

@Kurnal
SAMPLE

CPU Die SRAM Density-L3 Cache



In the KunPeng 930 CPU die
Have 1456Block L3 Cache
Each block size 64KiB
So in totally, CPU Die have 91MiB L3 Cache



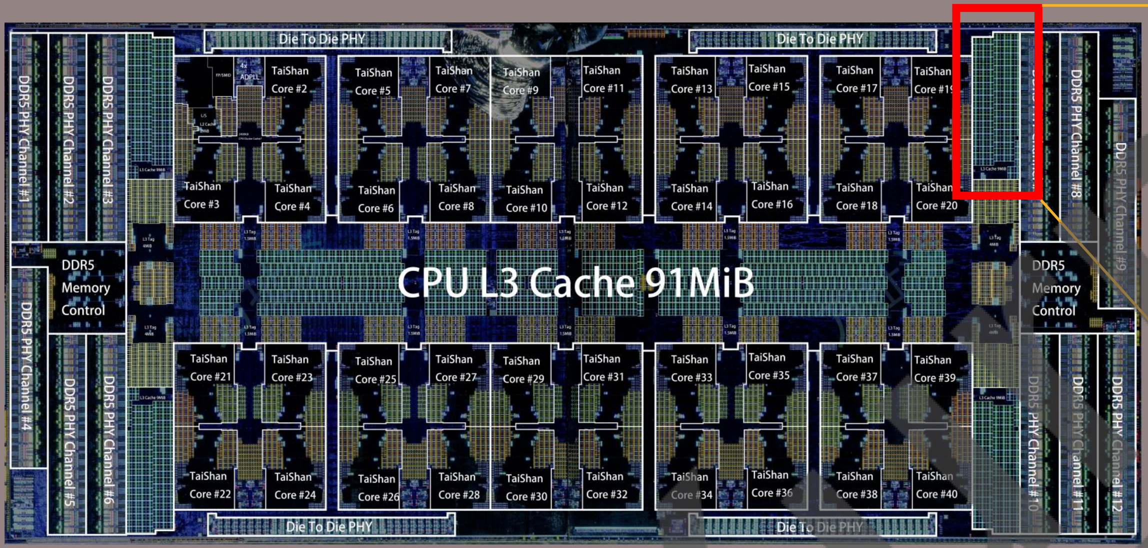
L3 Cache Sram Block

Size: 64KiB

0.015625mm2/64KiB
4096KiB/mm2

SAMPLE

CPU Die SRAM Density-L3 Cache



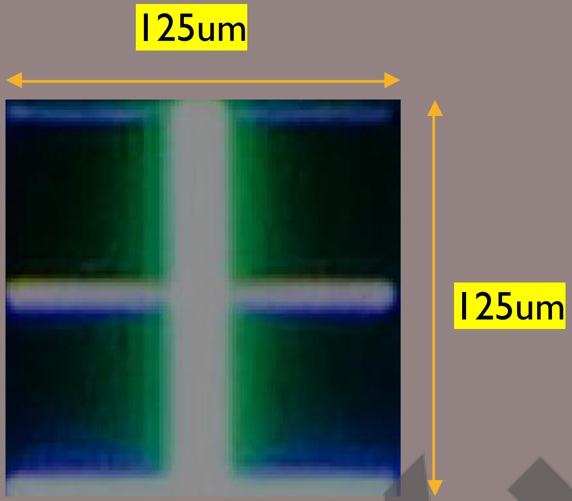
Sram Full area: 2.692mm2

Sram Block Nb: 144
Sram size: 9,216KiB

Sram Macro Density 3,423.48KiB/mm2

@Kurnal SAMPLE

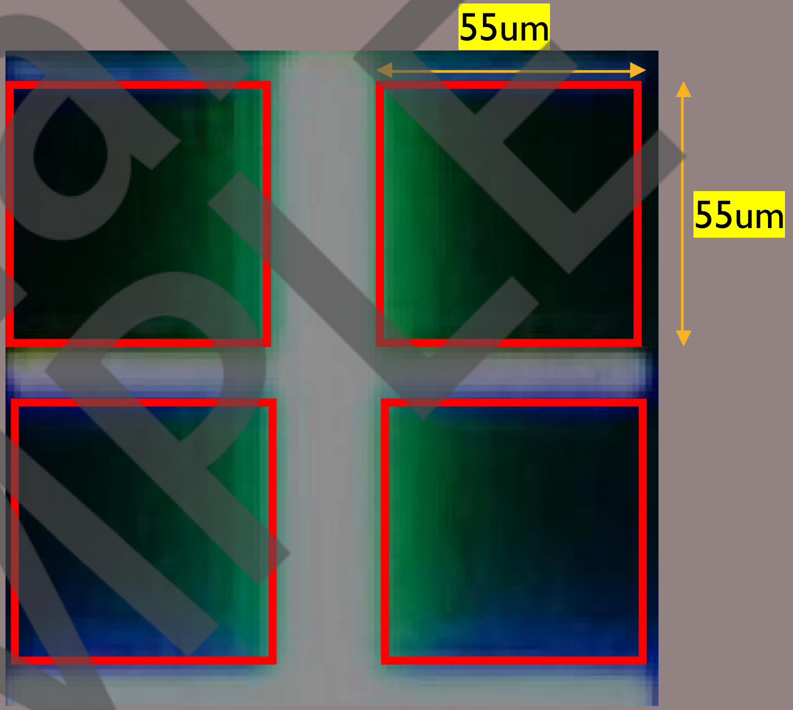
CPU Die SRAM Density-L3 Cache



L3 Cache Sram Block

Size: 64KiB

0.015625mm2/64KiB
4096KiB/mm2

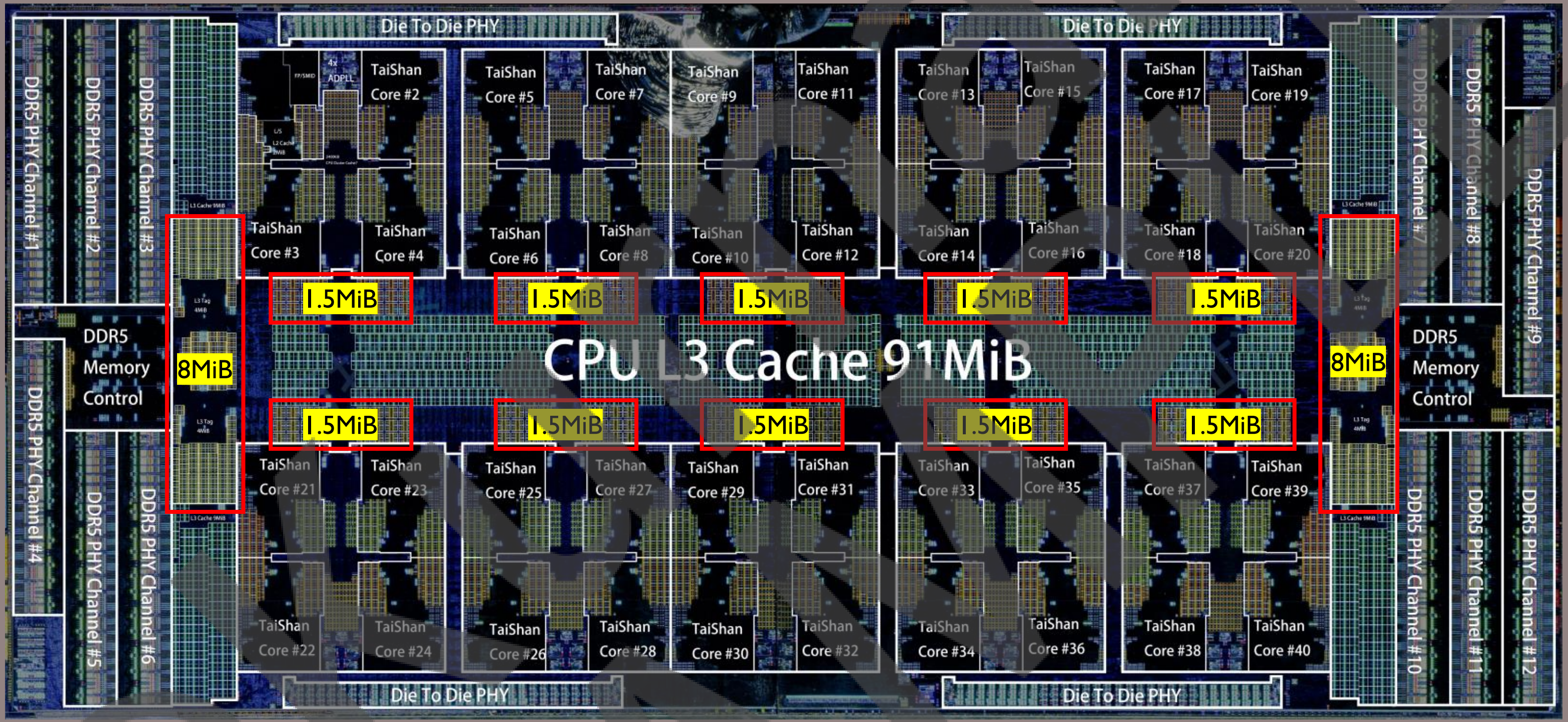


Sram bit cell by used: 12,100um2
Proportion: 77.44%

Sram Bit cell Density: 0.0231um2/bit

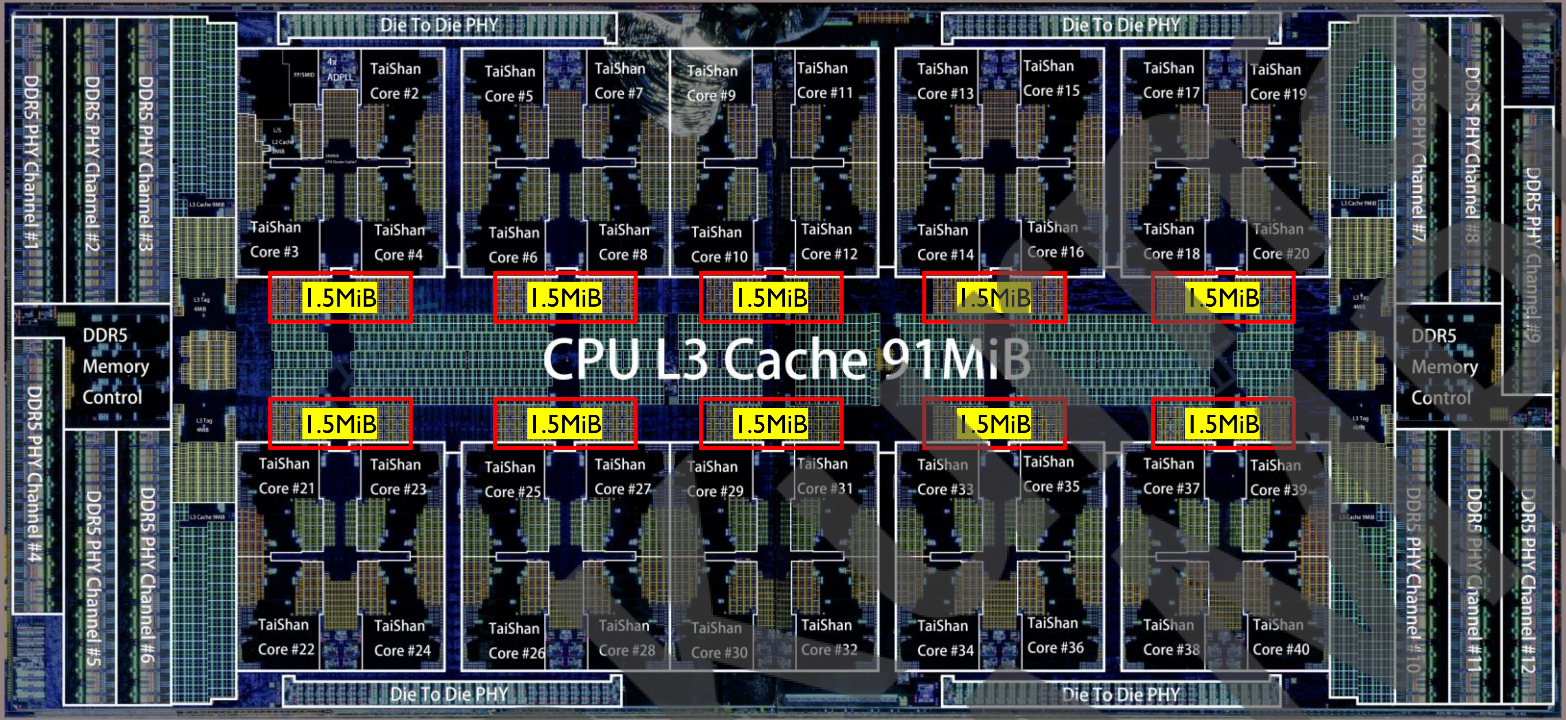
@Kurnal SAMPLE

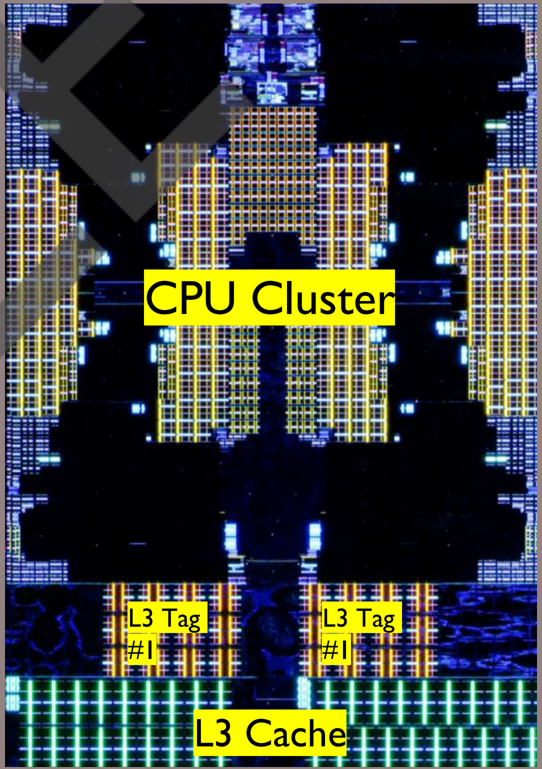
CPU Die SRAM Density-L3 Tag



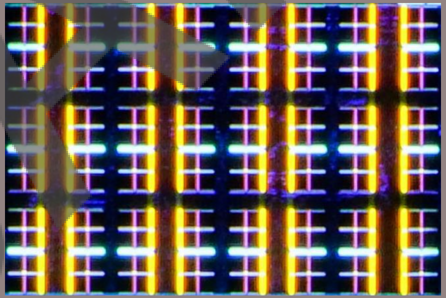
There have 2 types of L3 Tag cache
One type are under the each CPU Cluster
And another type are near the DDR5 PHY

CPU Die SRAM Density-L3 Tag#1



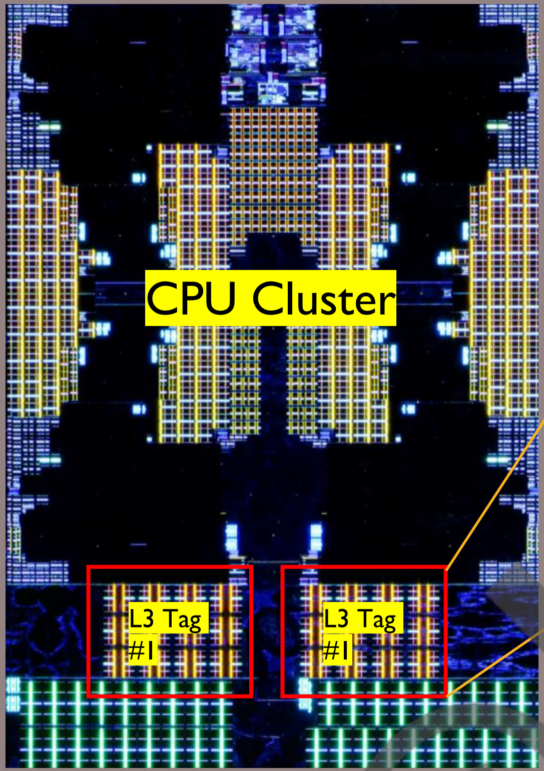


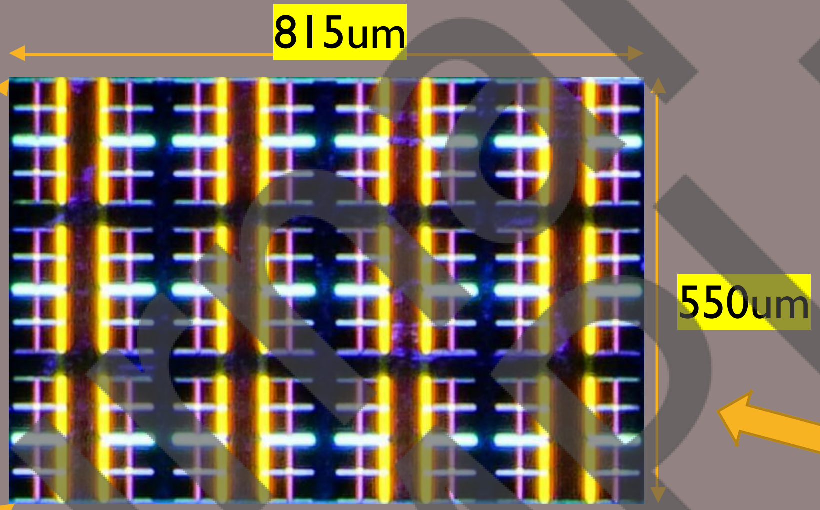
Each CPU cluster has two L3 Tag #1 clusters, each 768KiB, for a total of 1.5MiB.
A total of 15MiB of L3 Tag #1.



L3 Tag #1 (768KiB)

CPU Die SRAM Density-L3 Tag#1



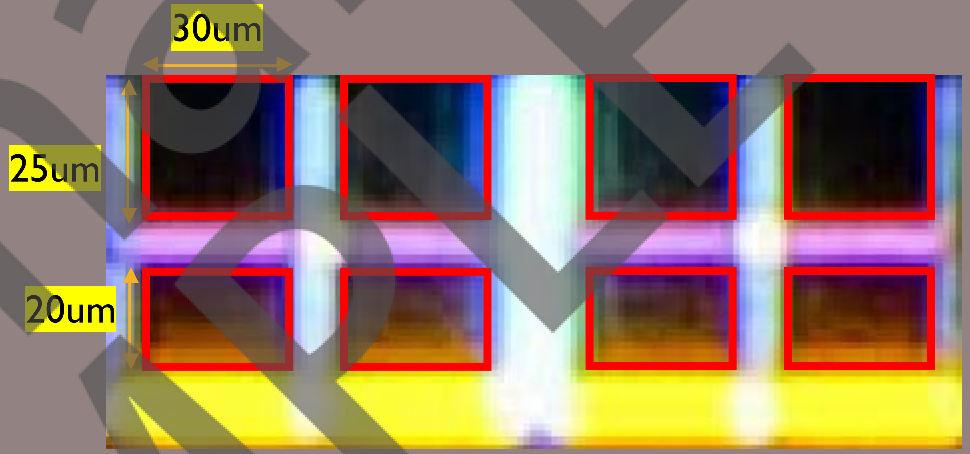


L3 Tag #1
(768KiB)

Sram Full area:	0.44825mm2
Sram Block Nb:	24
Sram size:	768KiB
Sram Macro Density	1,713.33KiB/mm2

@Kurnal SAMPLE

CPU Die SRAM Density-L3 Tag#1



L3 Tag #1 Sram Block

Size: 32KiB

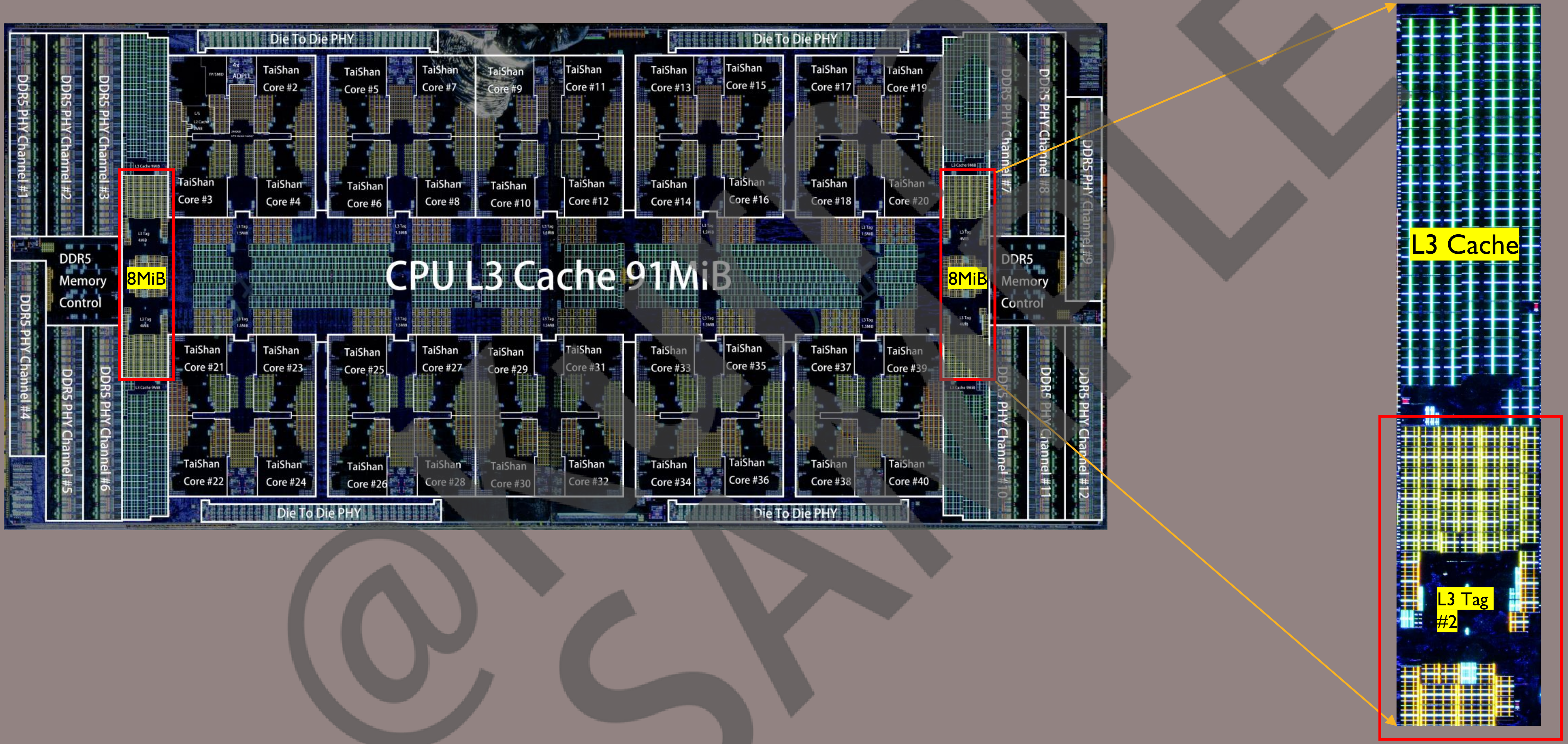
0.012375mm2/32KiB
2,585.86KiB/mm2

Sram bit cell by used: 5,400um2
Proportion: 43.64%

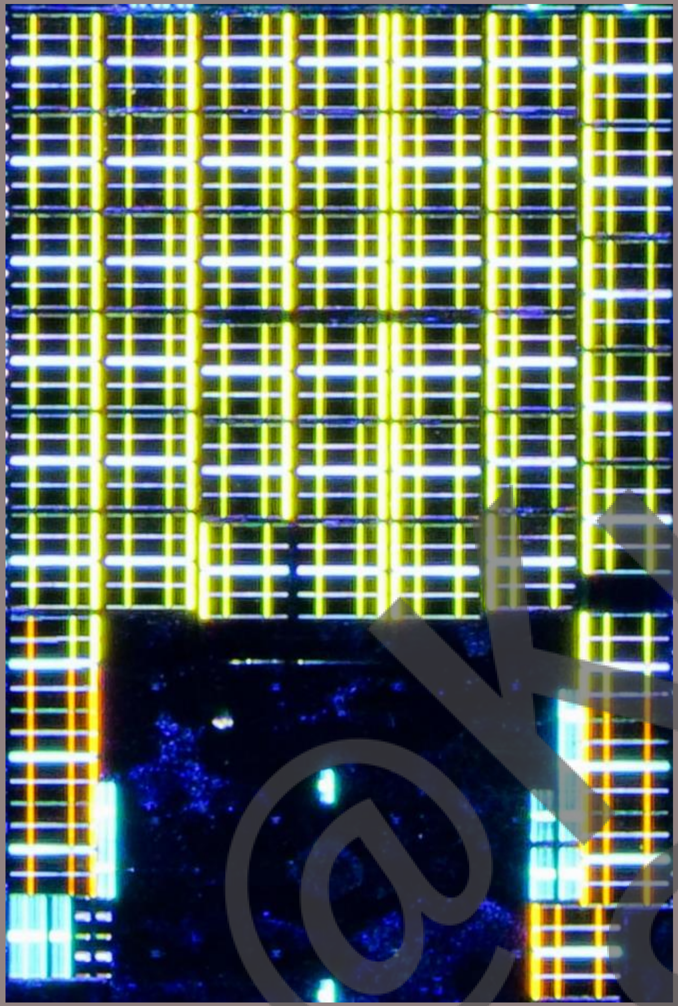
Sram Bit cell Density: 0.0206um2/bit

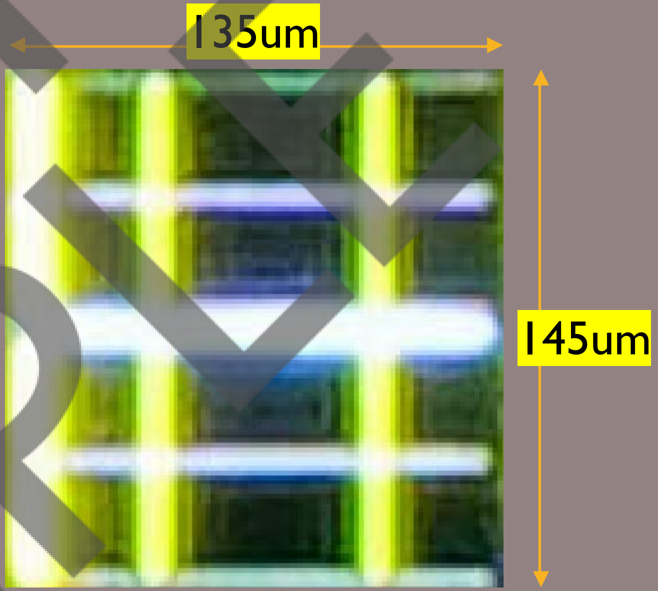
@Kurnal
SAMPLE

CPU Die SRAM Density-L3 Tag#2



CPU Die SRAM Density-L3 Tag#2





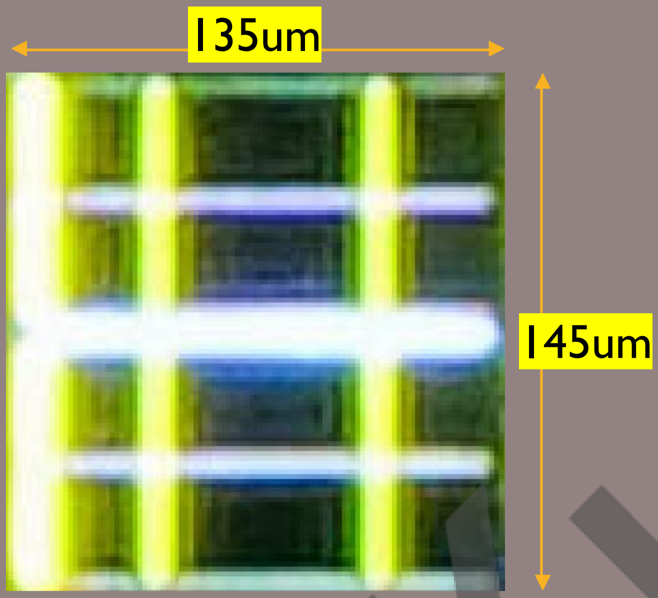
L3 Tag #2 Sram Block

Size: 64KiB

0.019575mm2/64KiB
3,269.47KiB/mm2

@Kurnal SAMPLE

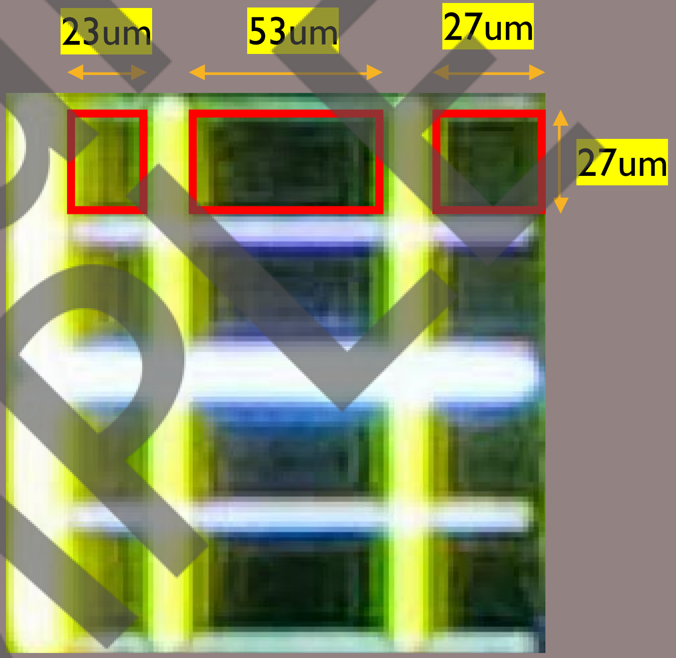
CPU Die SRAM Density-L3 Tag#2



L3 Tag #2 Sram Block

Size: 64KiB

0.019575mm2/64KiB
3,269.47KiB/mm2

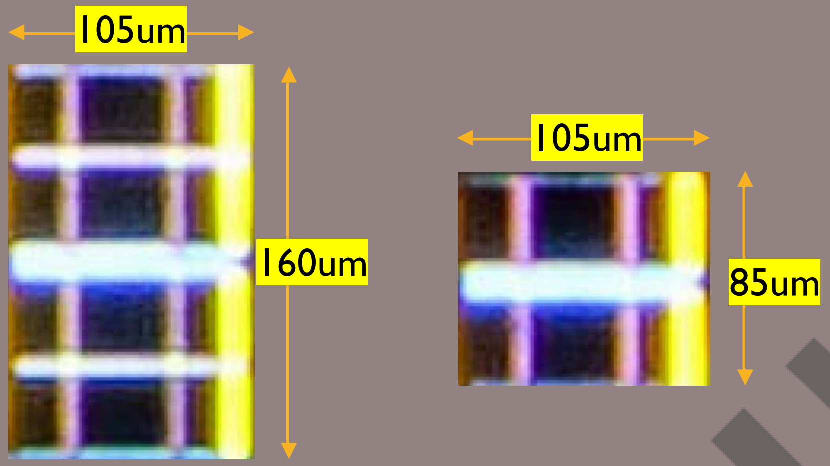


Sram bit cell by used: 11,124um2
Proportion: 56.83%

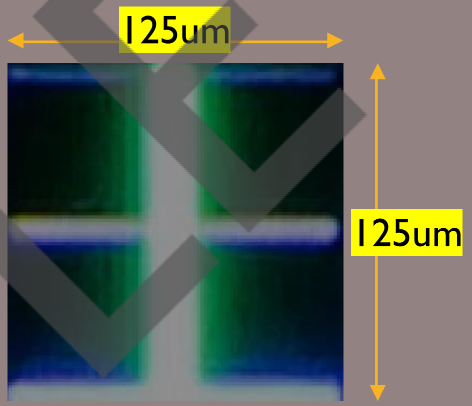
Sram Bit cell Density: 0.02122um/bit

@Kurnal
SAMPLE

CPU Die SRAM Density-END(L2/L3)



CPU L2 Cache Block



CPU L3 Cache Block

CPU L2 Macro Density: 3,792.59KiB/mm2

CPU L2 SRAM Block area: 0.0168mm2/64KiB
3,809.52KiB/mm2
0.00892mm2/32KiB
3,585.43KiB/mm2

CPU L2 SRAM Bit area : 0.02136um2/bit
CPU L2 SRAM Block Density : 28Mbit/mm2

CPU L3 Macro Density: 3,423.48KiB/mm2

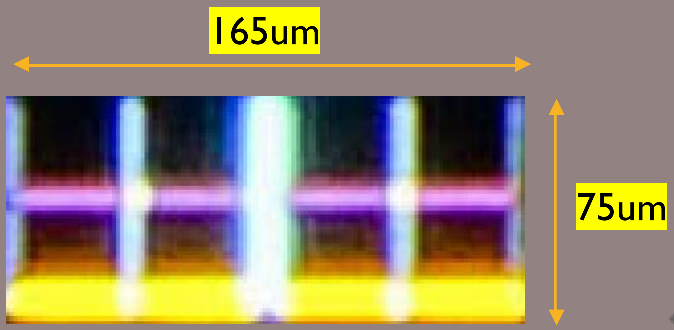
CPU L3 SRAM Block area: 0.015625mm2/64KiB
4096KiB/mm2

CPU L3 SRAM Bit area : 0.0231um2/bit
CPU L3 SRAM Block Density : 32Mb/mm2

@Kurnal
SAMPLE

CPU Die SRAM Density-END(L3 Tag)

@Kurnal SAMPLE

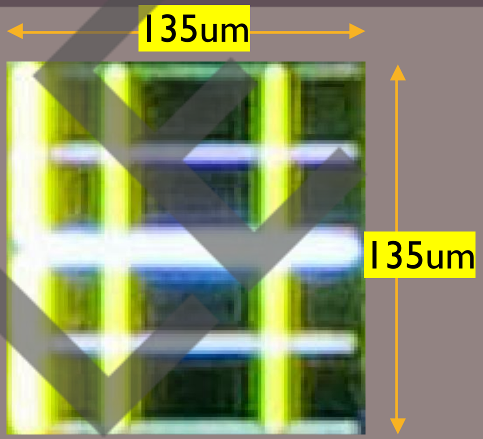


CPU L3 Tag Block #1

CPU L3 Tag Macro Density: 2,585.86KiB/mm2

CPU L3 Tag SRAM Block area: 0.012375mm2/32KiB
2,585.86KiB/mm2

CPU L3 Tag SRAM Bit area : 0.0206um2/bit
CPU L3 Tag SRAM Block Density : 20.2Mb/mm2



CPU L3 Tag Block #2

CPU L3 Tag Macro Density: 3,269.47KiB/mm2

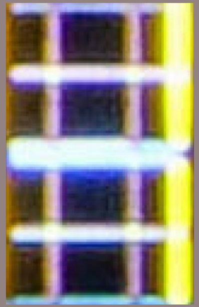
CPU L3 Tag SRAM Block area: 0.019575mm2/64KiB
3,269.47KiB/mm2

CPU L3 Tag SRAM Bit area : 0.02122um/bit
CPU L3 Tag SRAM Block Density : 25.52/mm2

CPU Die SRAM Density-END(Chip Technology)

High Performance Cell(HPC)

High Density Cell(HDC)



CPU L2 Cache

0.02136um2/bit

CPU L3 Tag

0.0206um2/bit

0.02122um/bit

HPC SRAM Density： 0.021um2/bit
HPC Macro Density: 28Mb/mm2

CPU L3 Cache

0.0231um2/bit

HDC SRAM Density： 0.023um2/bit
HDC Macro Density: 32Mb/mm2

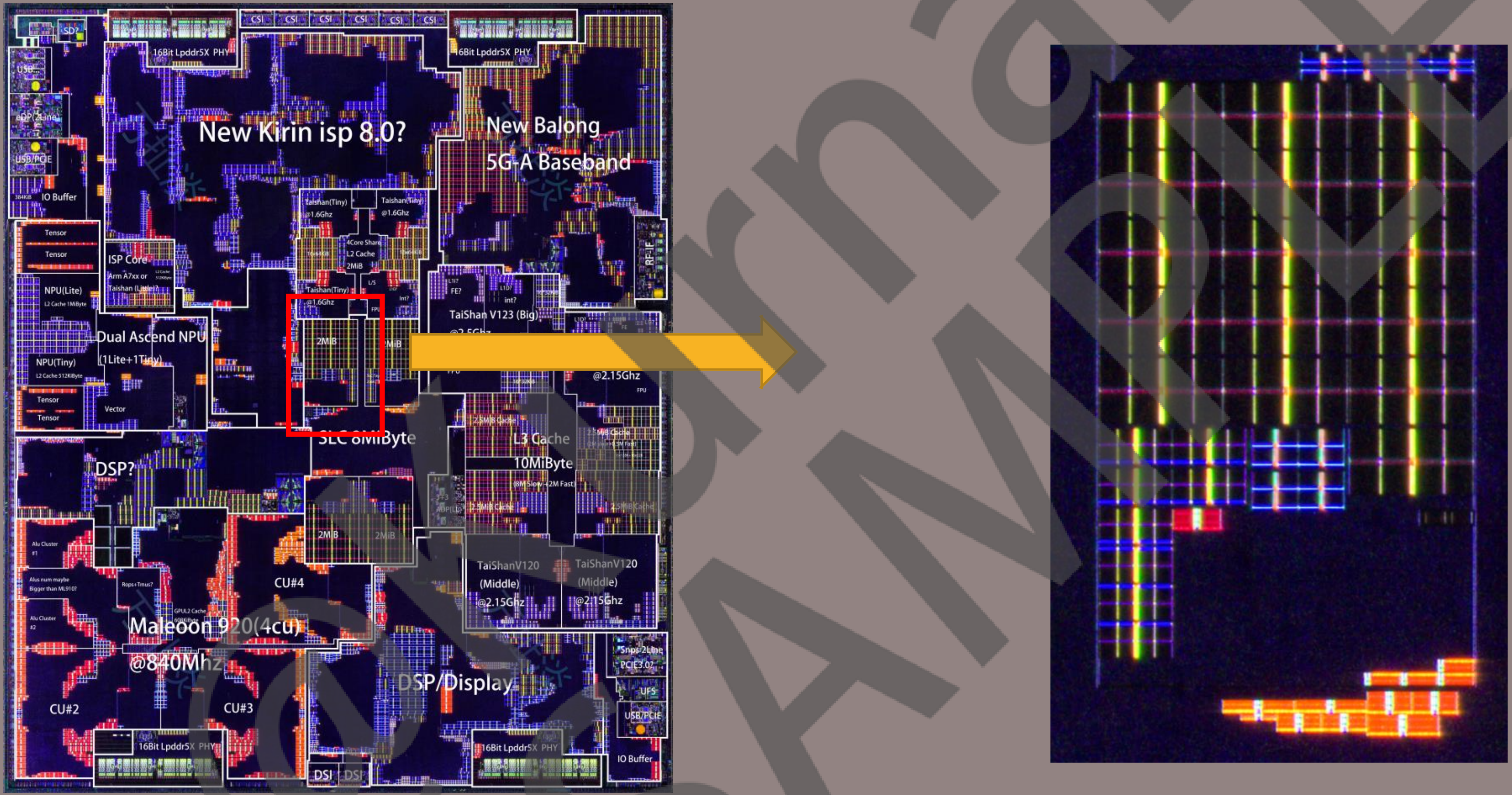
@Kurnal
SAMPLE

Sram Density VS

VS SMIC N+2 and TSMC N5P

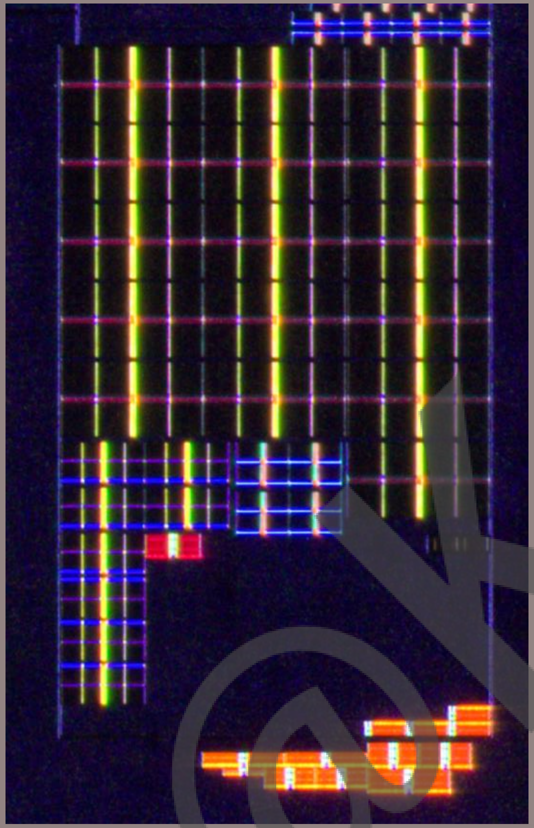
@Kurnal SAMPLE

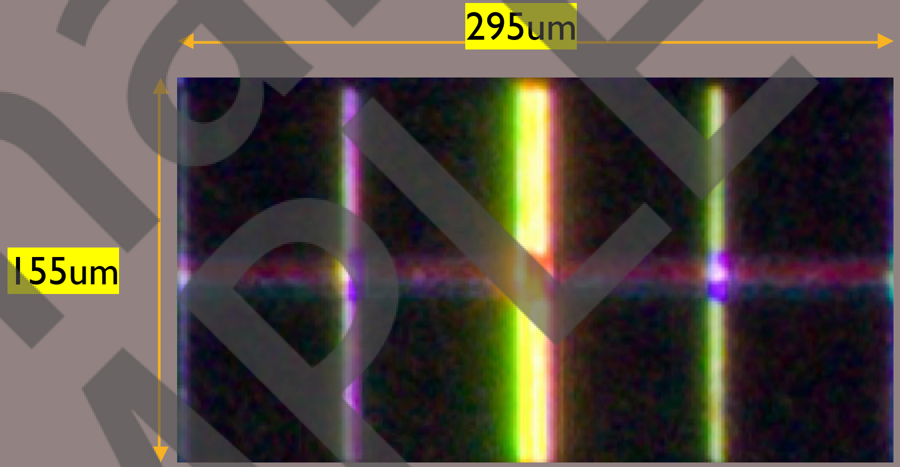
CPU Die SRAM Density-END (VS SMICN+2)



@Kurnal
SAMPLE

CPU Die SRAM Density-END (VS SMICN+2)





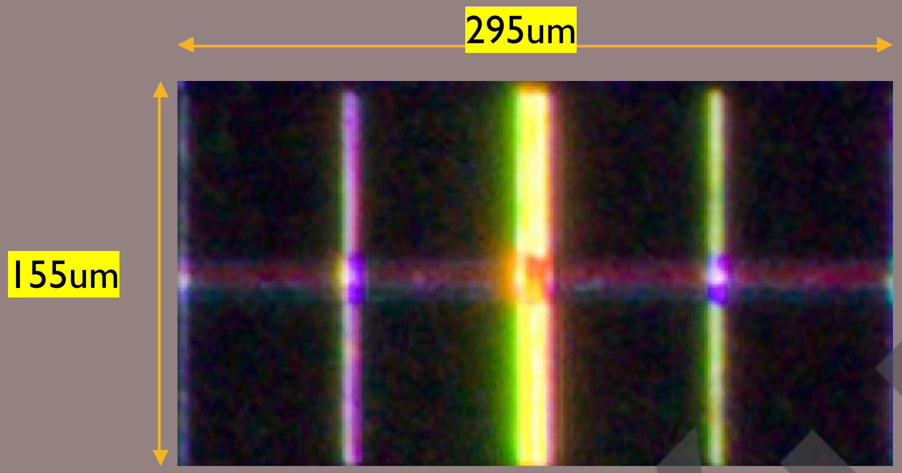
SLC Sram Block

Size: 128KiB

0.045725mm2/128KiB
2,799.34KiB/mm2

@Kurnal SAMPLE

CPU Die SRAM Density-END (VS SMICN+2)



SLC Sram Block

Size: 128KiB

0.045725mm2/128KiB
2,799.34KiB/mm2

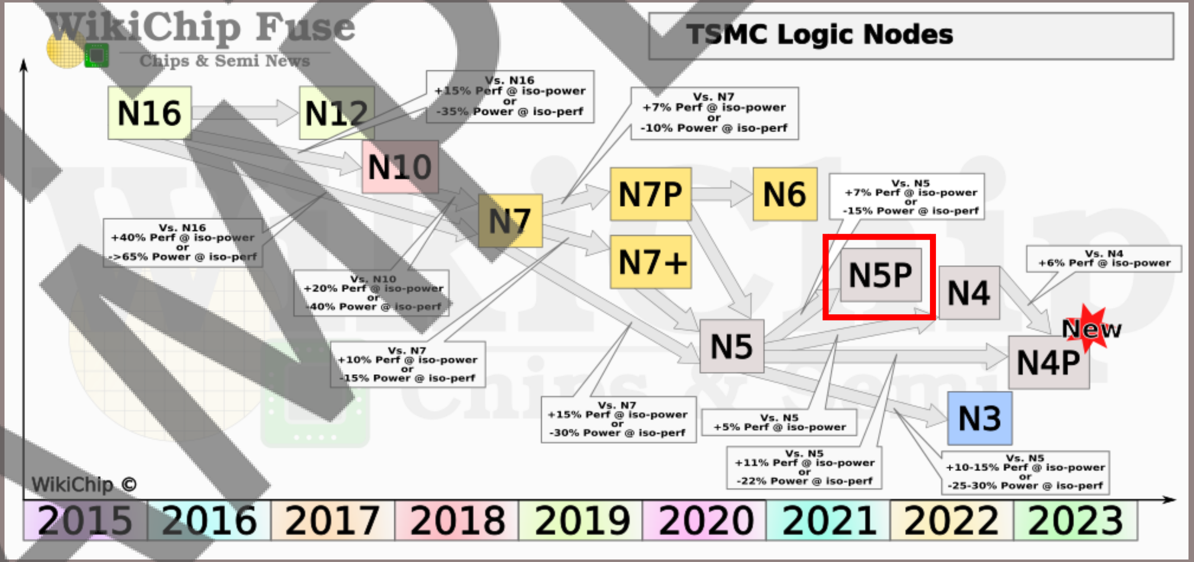
Sram bit cell by used: 36,400um2
Proportion: 79.60%

Sram Bit cell Density: 0.03471um2/bit

@Kurnal SAMPLE

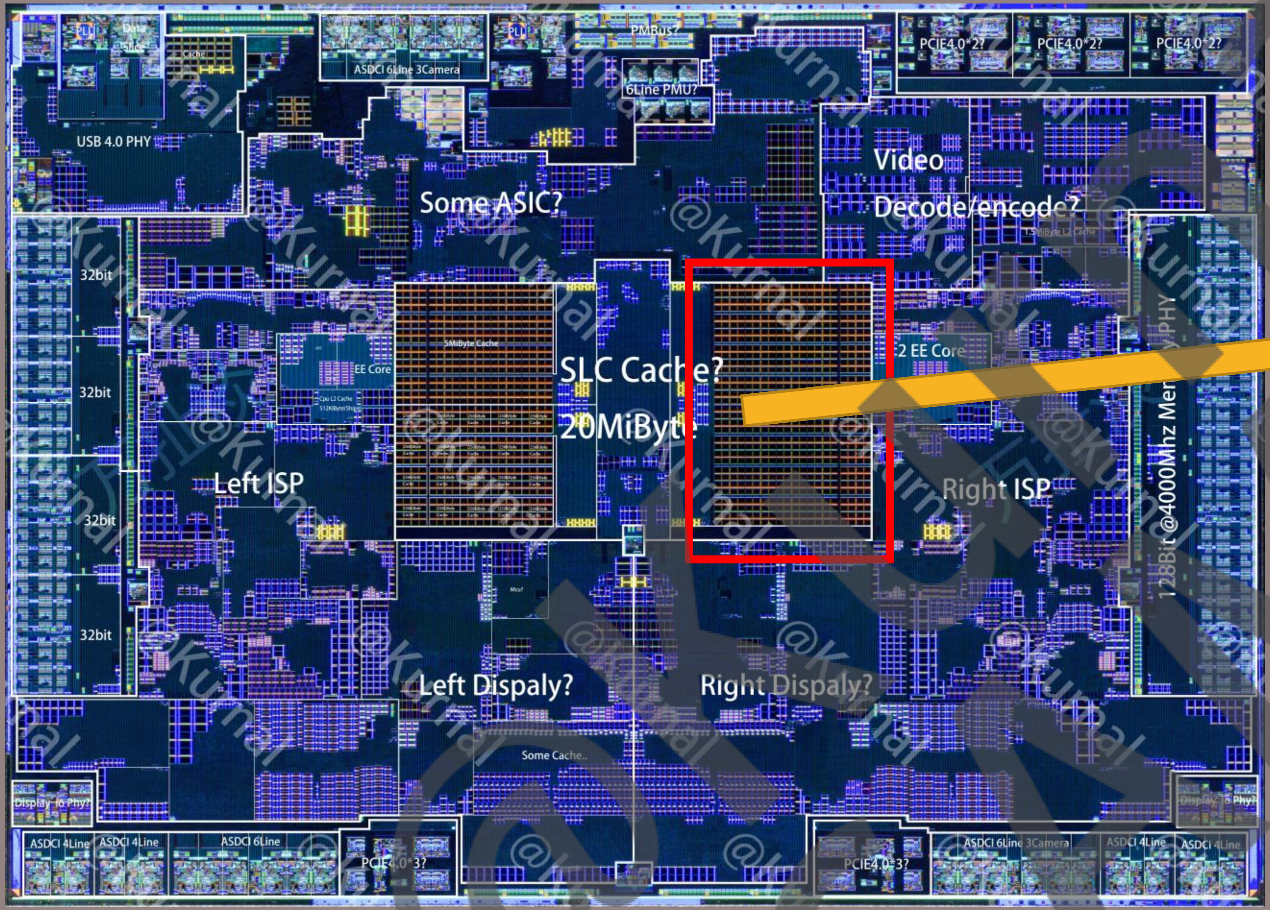
CPU Die SRAM Density-END (VS TSMC N5 apple R1)

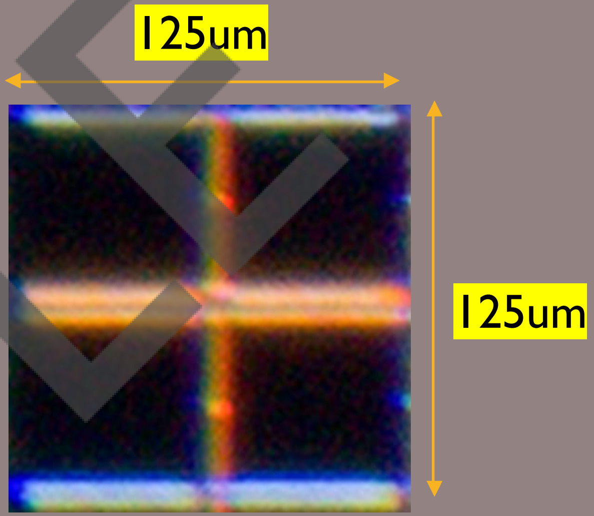
Apple R1
Technology： TSMC N5P



@Kurnal SAMPLE

CPU Die SRAM Density-END (VS TSMC N5 apple M2)





SLC Cache Sram Block

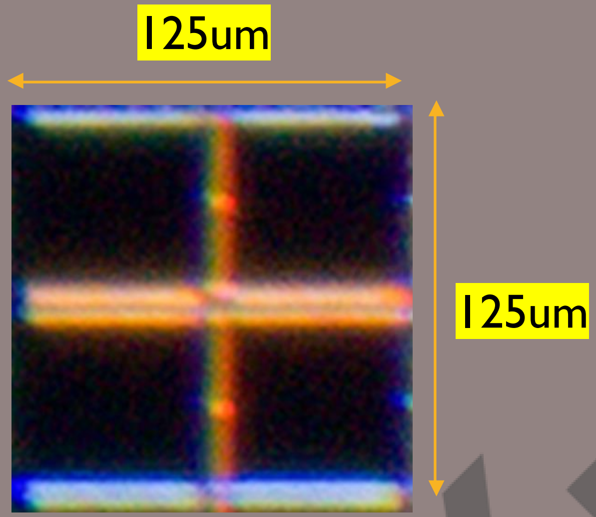
Size: 64KiB

0.015625mm2/64KiB

4096KiB/mm2

@Kurnal SAMPLE

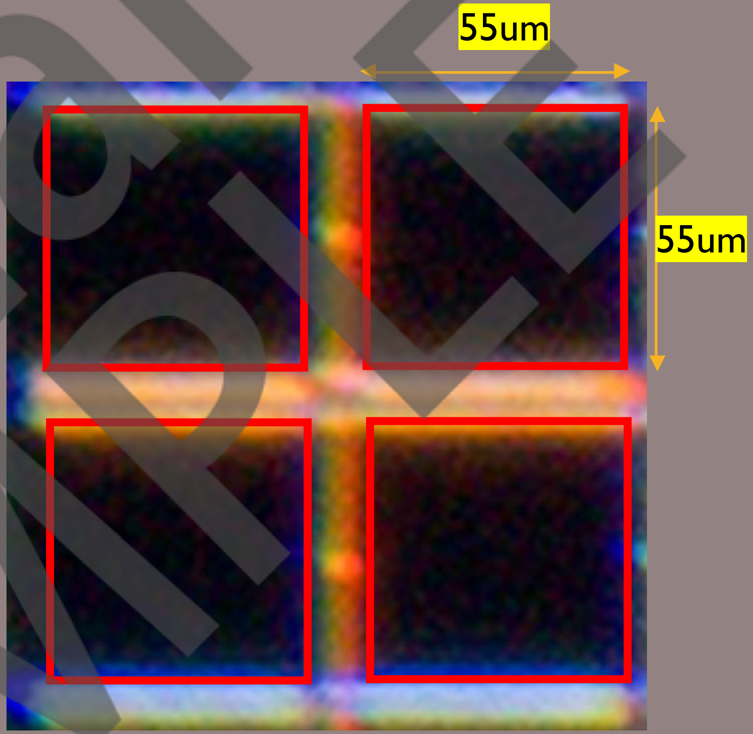
CPU Die SRAM Density-END (VS TSMC N5 apple M2)



SLC Cache Sram Block

Size: 64KiB

0.015625mm2/64KiB
4096KiB/mm2



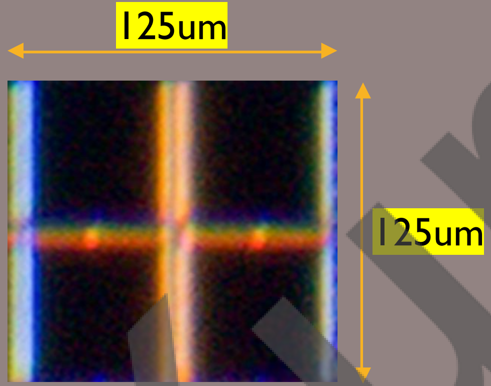
Sram bit cell by used: 12,100um2
Proportion: 77.44%

Sram Bit cell Density: 0.0231um2/bit

@Kurnal
SAMPLE

CPU Die SRAM Density-END(Chip Technology)

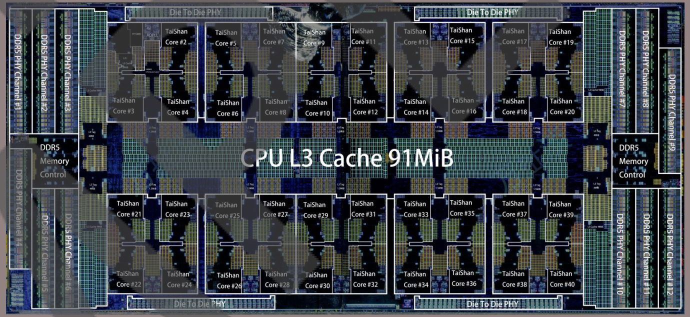
APPLE R1 Sram

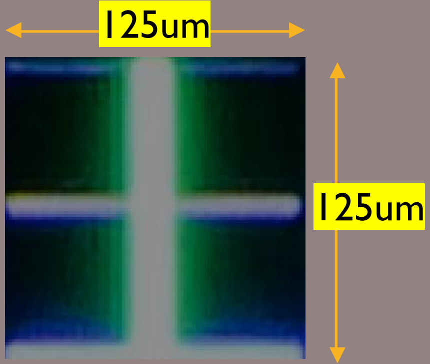


Made in TSMC N5P

SRAM Density : 0.023um2/bit
Macro Density: 32Mb/mm2

KunPeng 930 Sram





Same density and Same size

SRAM Density : 0.023um2/bit
Macro Density: 32Mb/mm2

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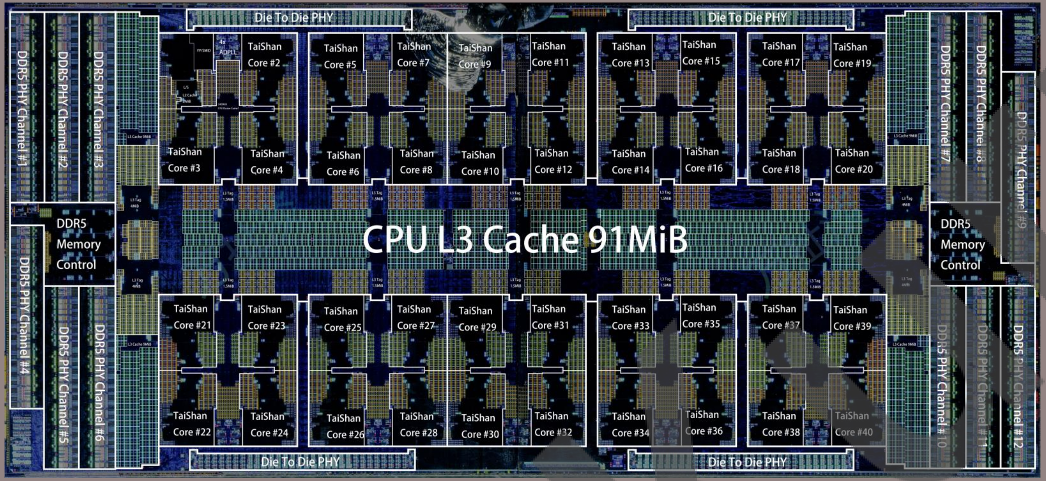
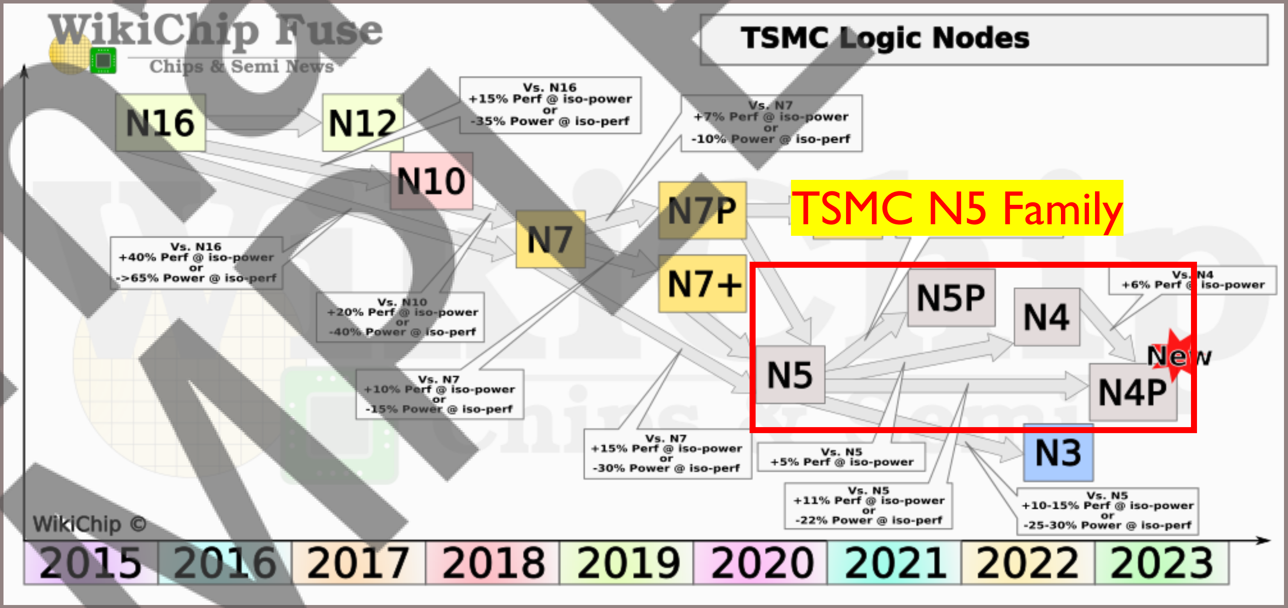
CPU Die SRAM Density-END(Chip Technology)



KunPeng 930



TSMC N5 Family

SRAM bit size: 0.021um2
SRAM Macro Density: 32Mbit/mm2

Based on my identification,
I believe that Kunpeng 930 uses TSMC N5 family

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CPU Die Analyze

IO PHY

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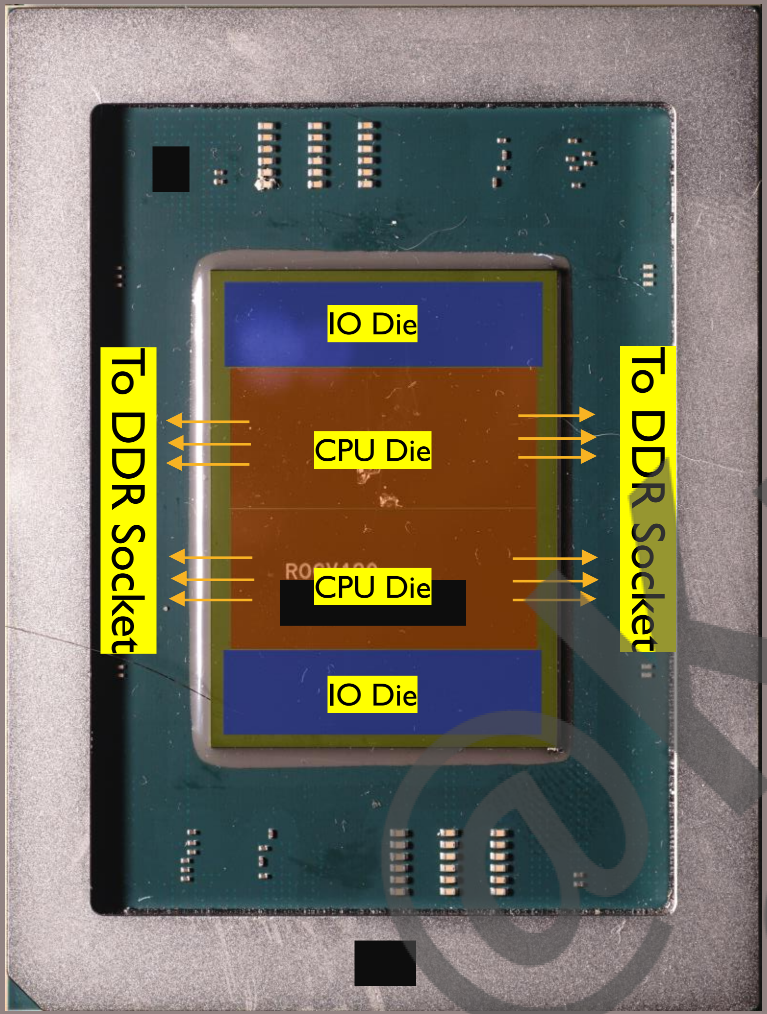
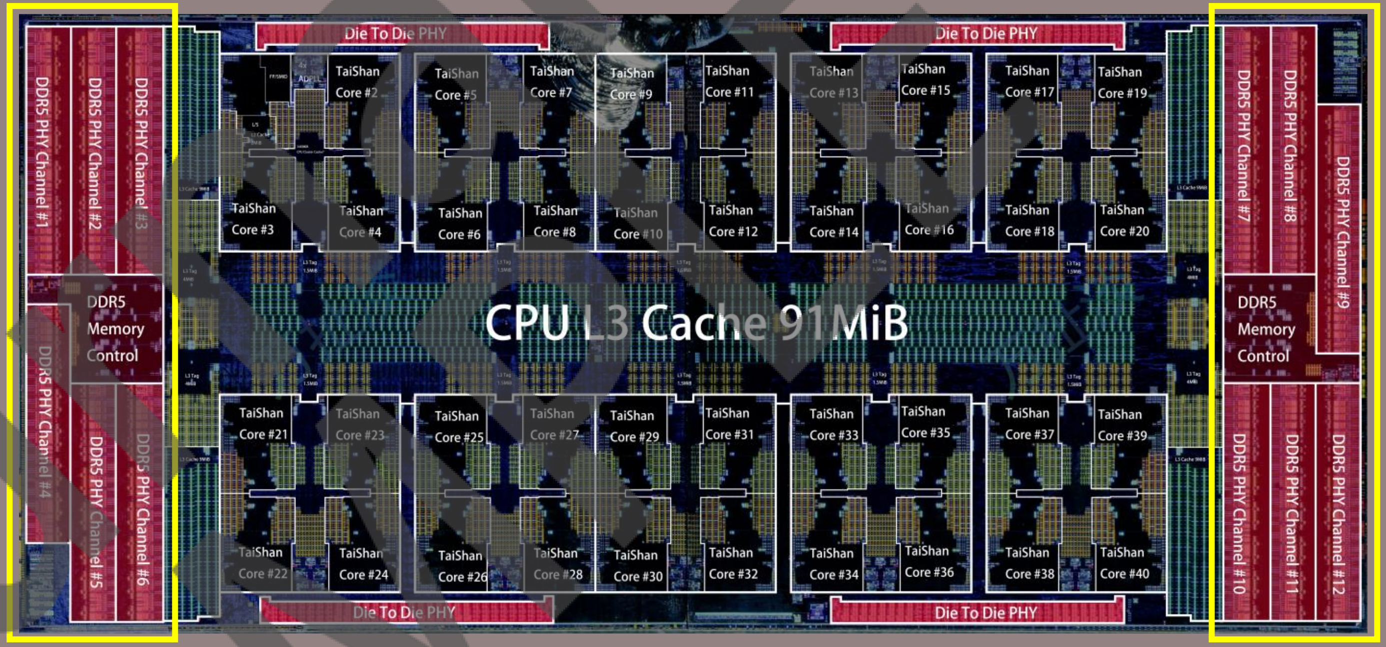
SAMPLE

CPU Die Analyze-DDR PHY





3 Channel DDR5
3x 64Bit=192bit

6 Channel x 64Bit=384Bit
2die x 6Channel x 64bit=768Bit

3 Channel DDR5
3x 64Bit=192bit

With each of its two CPU dies featuring a 6-channel DDR5 PHY,
the Kunpeng 930 supports up to 12 DDR5 channels with 768bit in total

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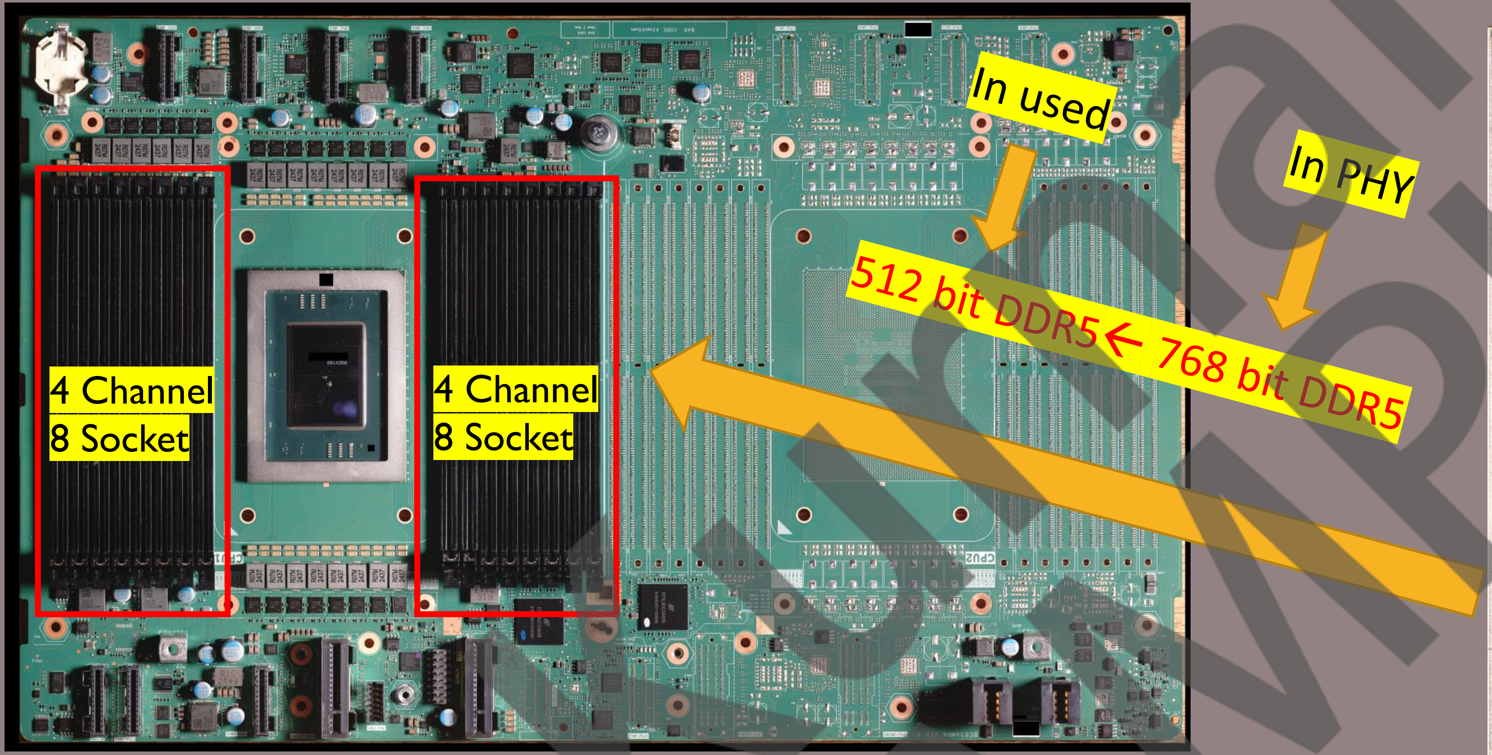
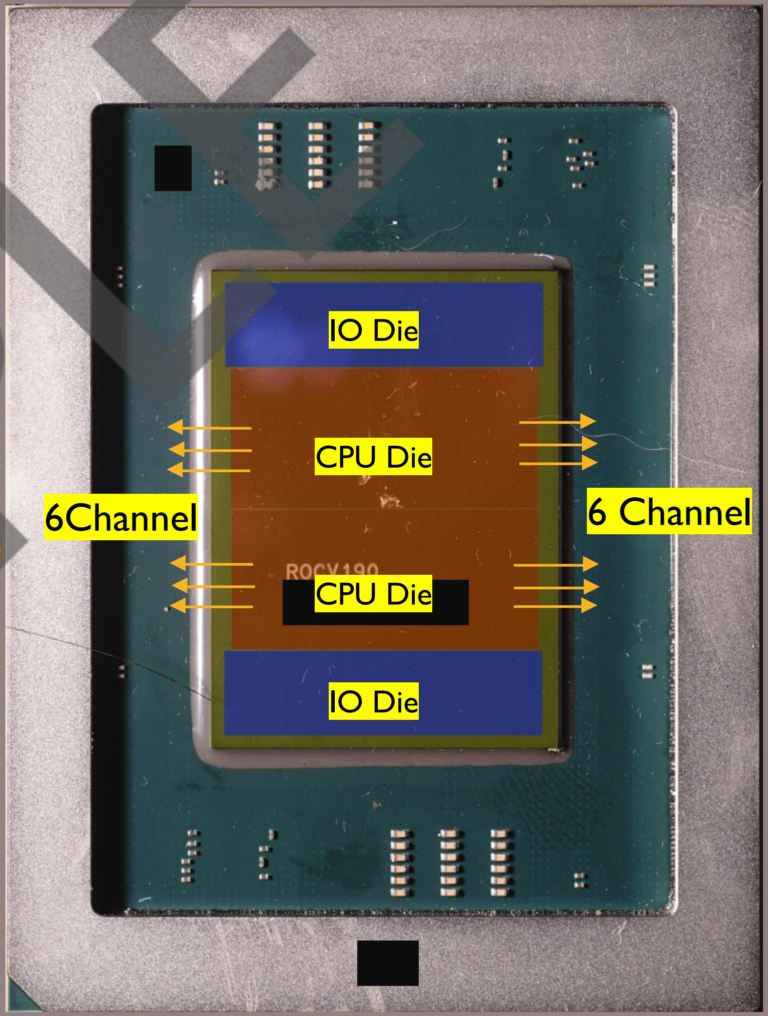
CPU Die Analyze-DDR PHY





On this board
the KunPeng930 uses only 8 DDR5 Channel of its 12 DDR5 channels.
Could future motherboards enable full channel support,
or is this inherent to single-die CPU designs?

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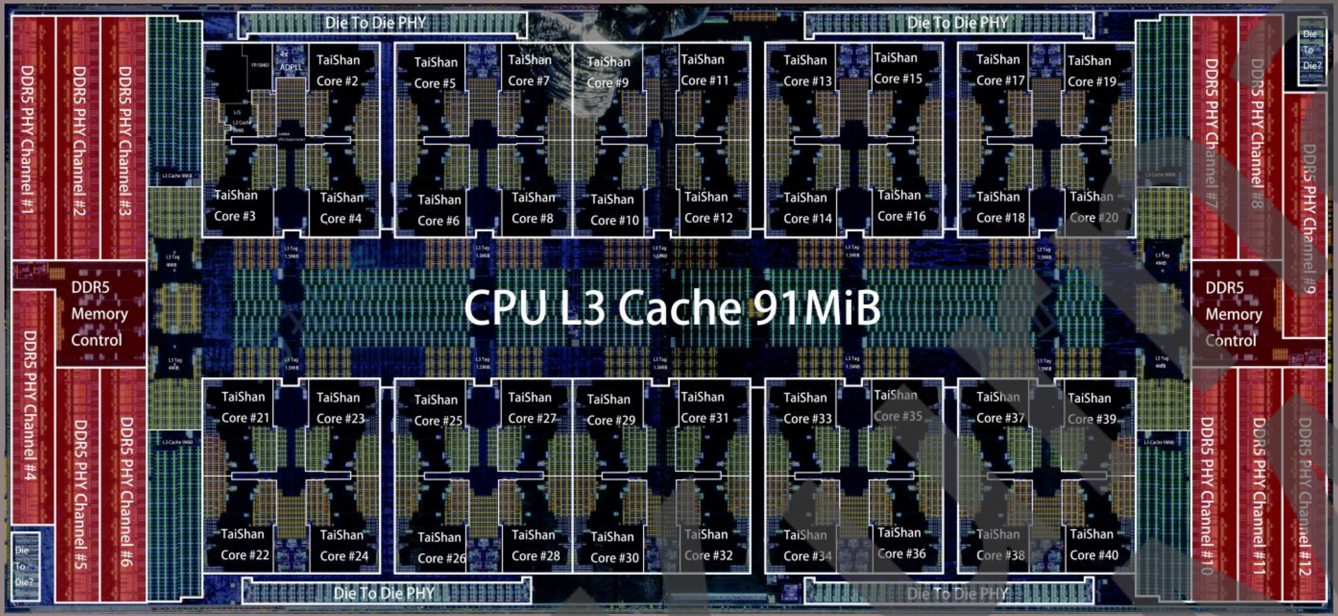
CPU Die Analyze-DDR PHY



This chip have 6 DDR5 channels.

Memory Full area	47.2mm2 (23.6mm2x2)
Memory PHY area	40.272mm2
Memory Control area	6.928mm2 (3.464mm2 x2)

DDR5 PHY Channel #1 area：	3.376mm2	DDR5 PHY Channel #7 area：	3.372mm2
DDR5 PHY Channel #2 area：	3.378mm2	DDR5 PHY Channel #8 area：	3.238mm2
DDR5 PHY Channel #3 area：	3.538mm2	DDR5 PHY Channel #9 area：	3.234mm2
DDR5 PHY Channel #4 area：	3.234mm2	DDR5 PHY Channel #10 area：	3.538mm2
DDR5 PHY Channel #5 area：	3.238mm2	DDR5 PHY Channel #11 area：	3.378mm2
DDR5 PHY Channel #6 area：	3.372mm2	DDR5 PHY Channel #12 area：	3.376mm2

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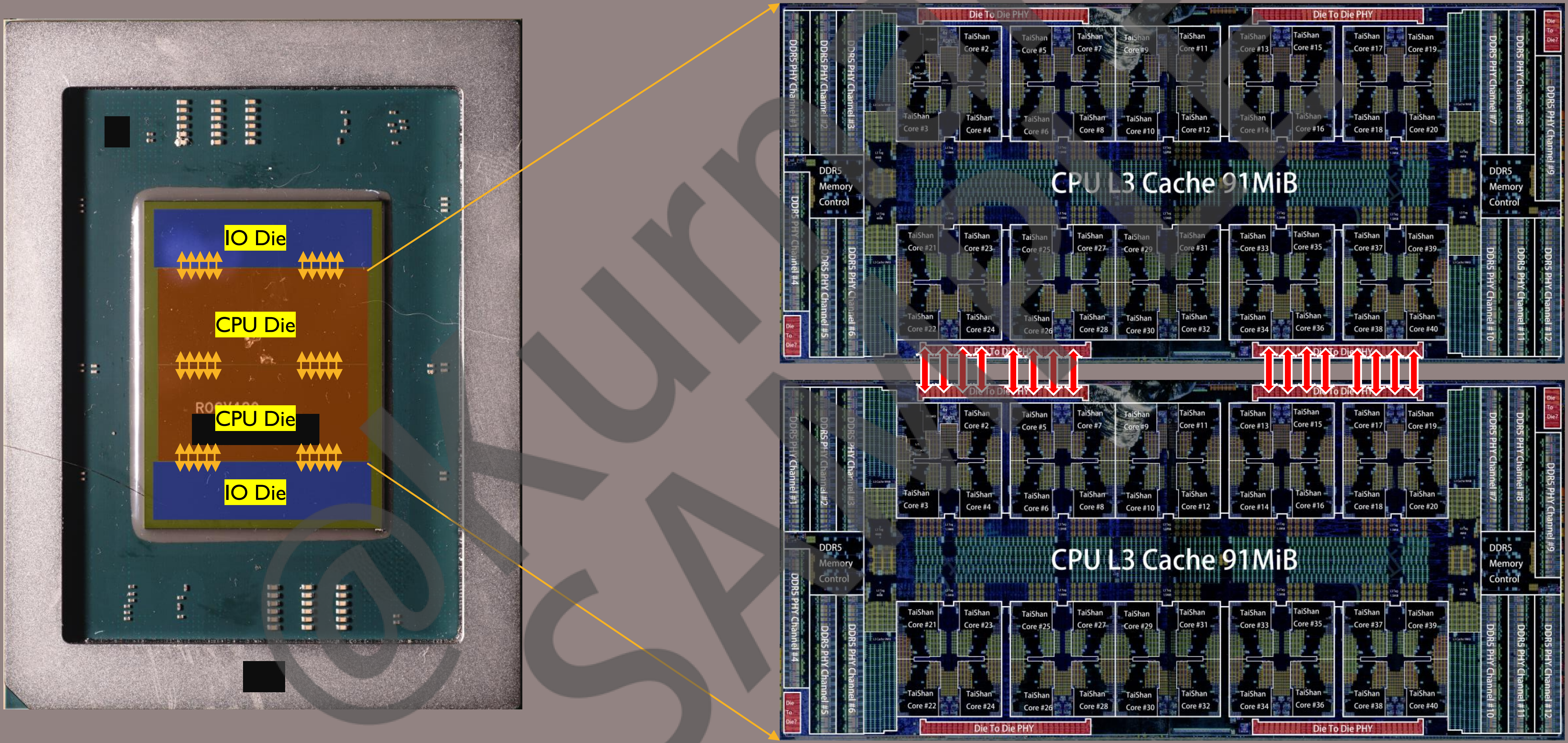
CPU Die Analyze-D2D PHY



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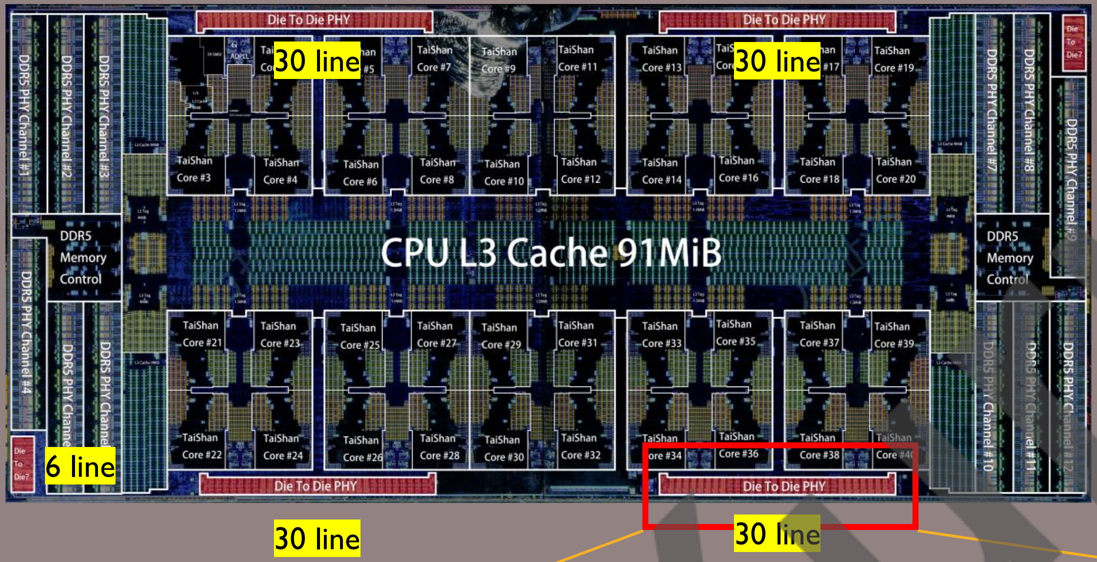
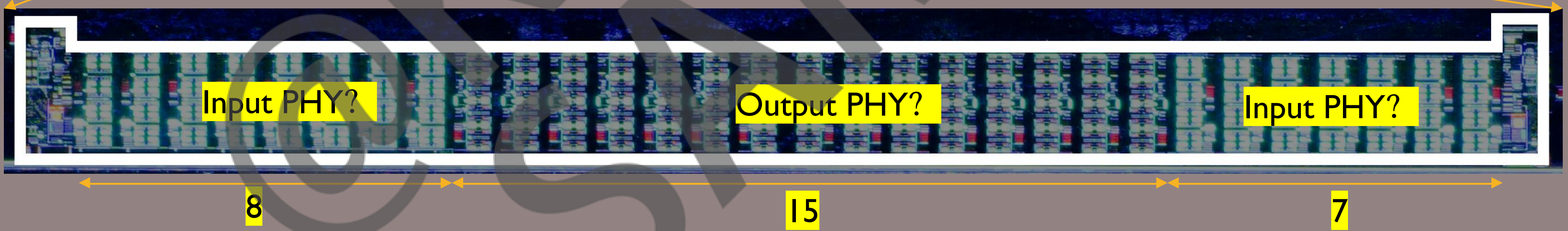
CPU Die Analyze-D2D PHY



Each CPU die has four sets of die-to-die interfaces.

Each long edge has two interfaces
each with a 30-line PHY, likely 15-in, 15-out
and traces of TSV.



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