HUAWEI MATE70PRO+ CIS&UFS ANALYSIS

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VERSION（修订版本）	

Version	Data	Updata
V1	2025/01/21	initial release(Beta)
V2	2025/02/21 22:02	Finish SC580xs/M70PP
V3	2025/02/22 3:00	Finish 1.5mp red maple

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NAND(UFS)分析

LPDDR 分析

Kirin9020 分析（见另一份）

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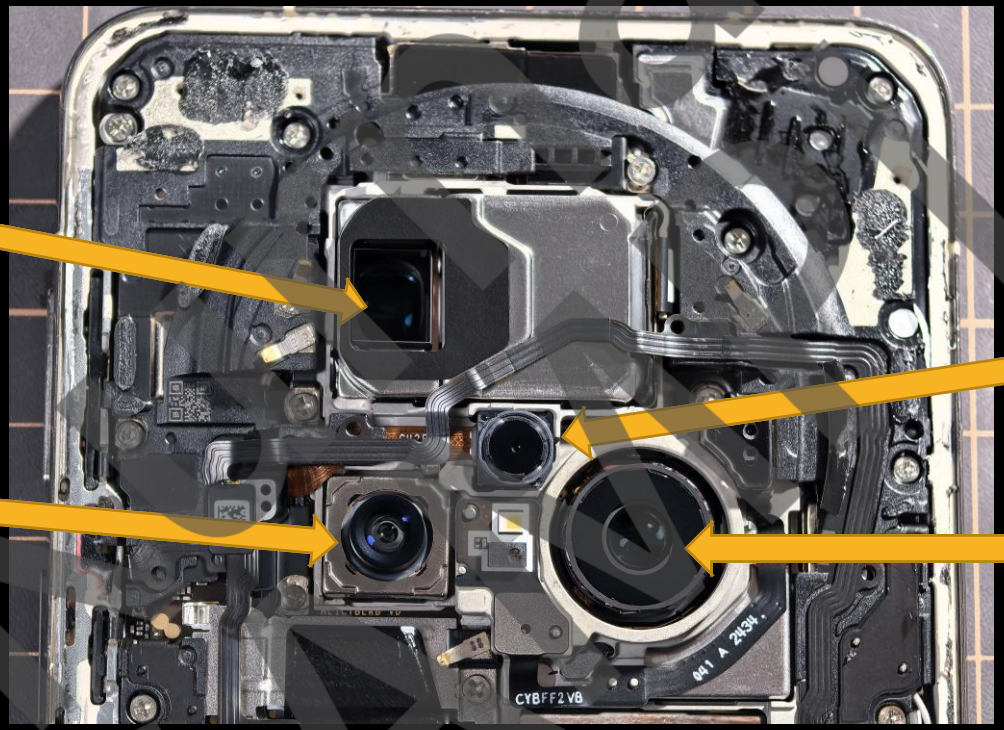

长焦:48mp F2.1 RYYB,OIS

超广角:40mp F2.2 RYYB

本次分析

红枫:1.5mp

主摄:50mp F1.4-4,RYYB, OIS

MATE70PRO+ 主摄

正文

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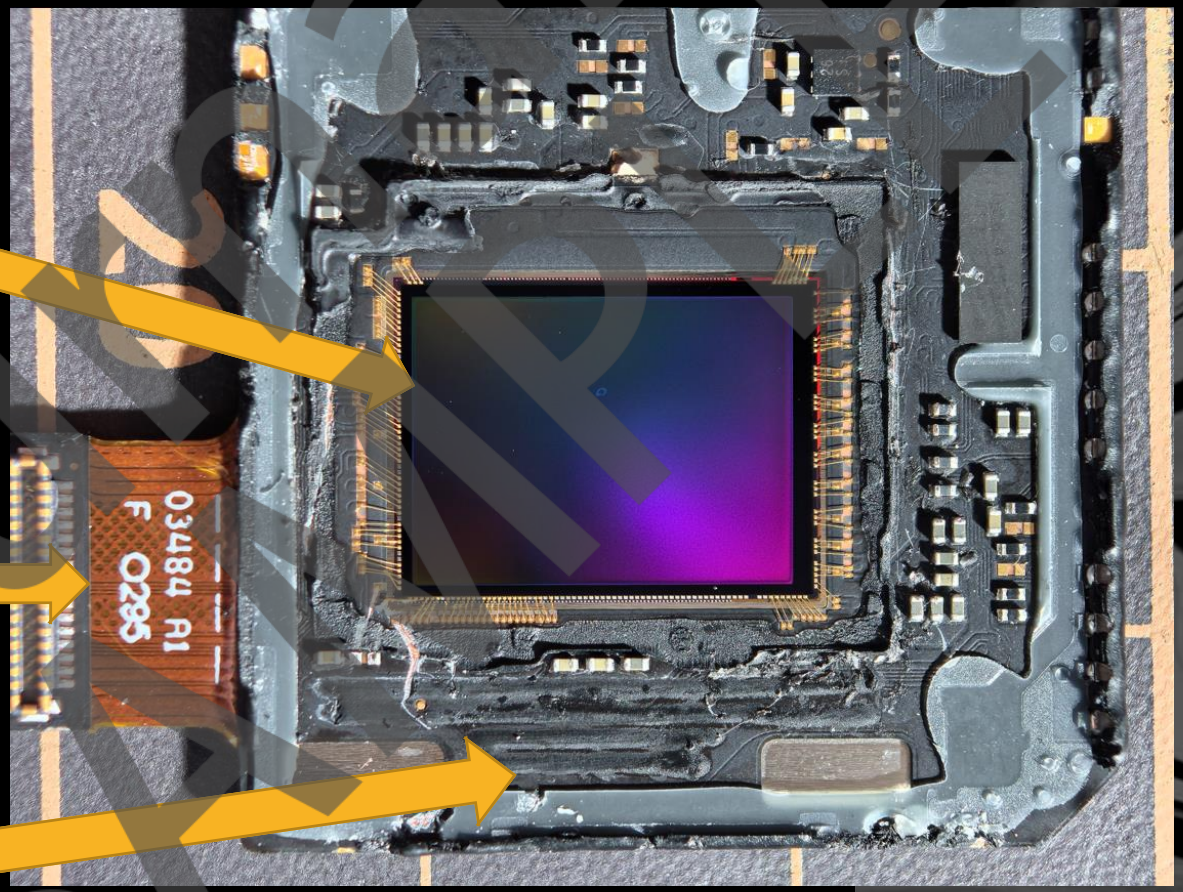
MATE70PRO+ CIS(MAIN)

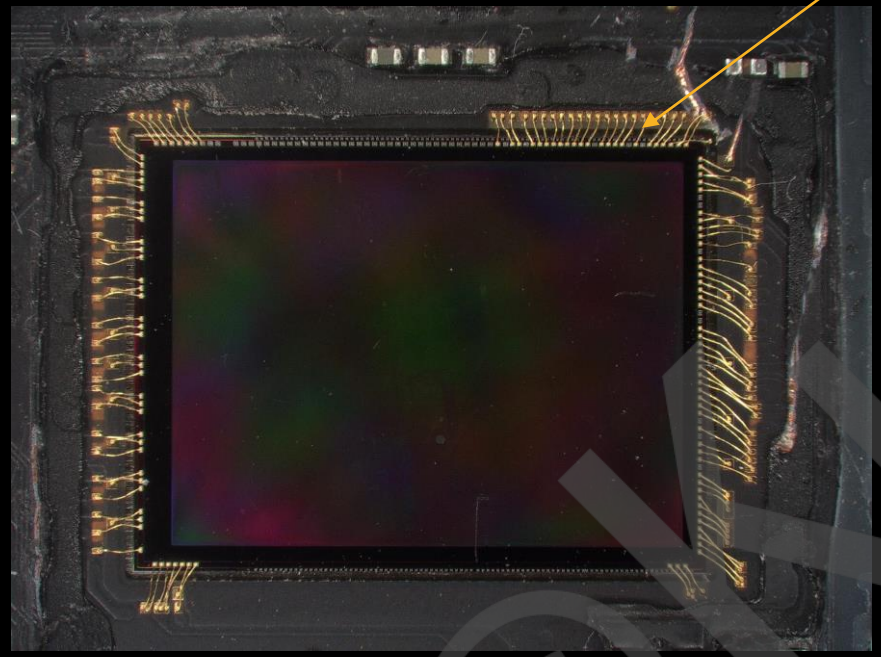
Cmos Die
50mp RYYB

FPC Mark
03484 A1
F O295

Cmos substrate & PCB

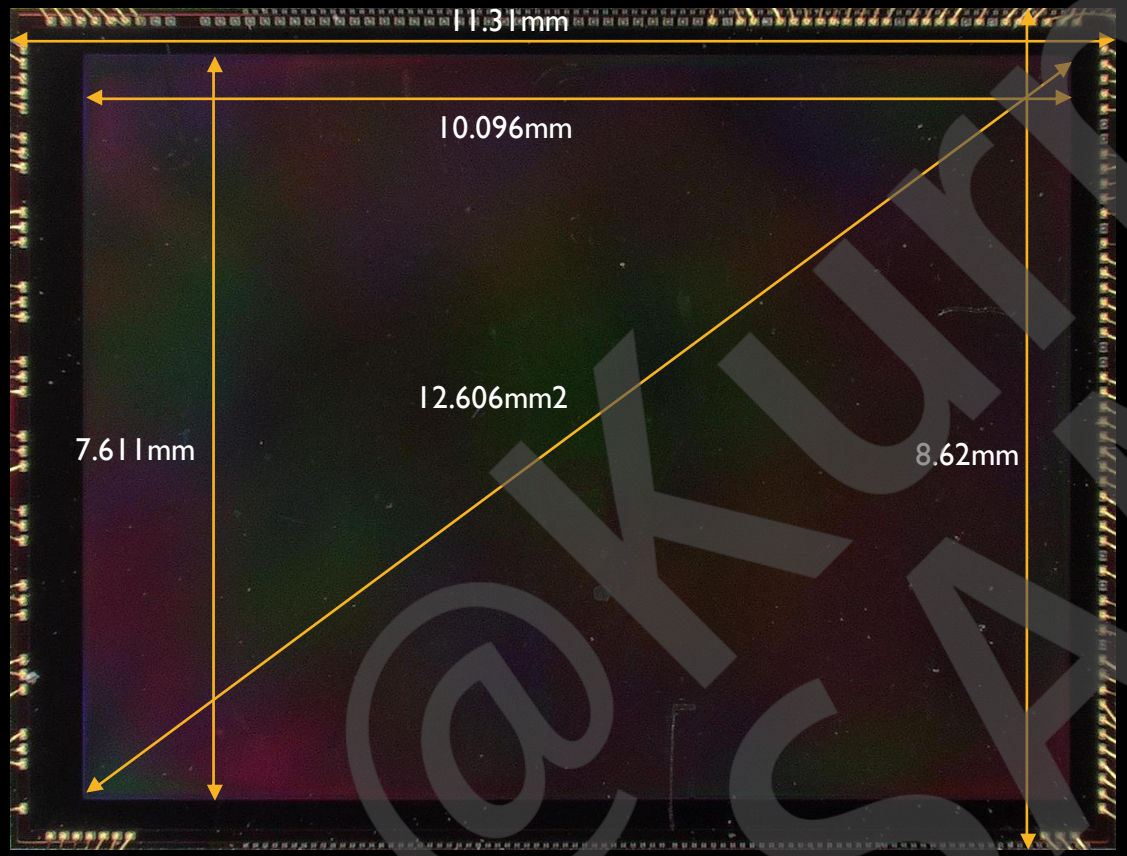


MATE70PRO+ CIS(MAIN)



Bonding Pad number: 166
Bonding Pad in use: 117

MATE70PRO+ CIS(MAIN)



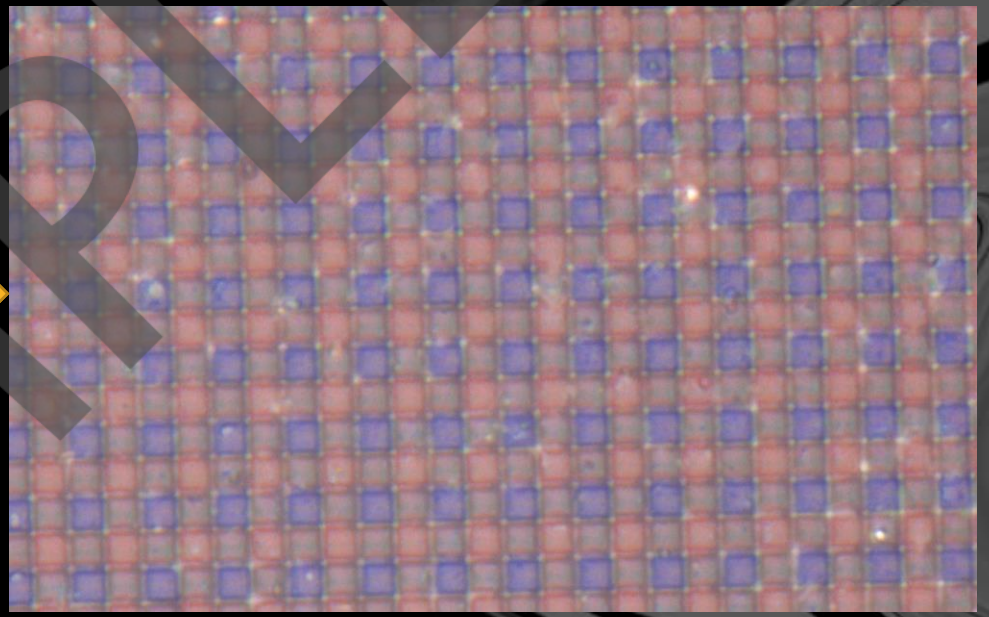
Full diesize : 97.49mm2
(11.31x8.62)

Pixel area: 76.84mm2
(10.096x7.611)

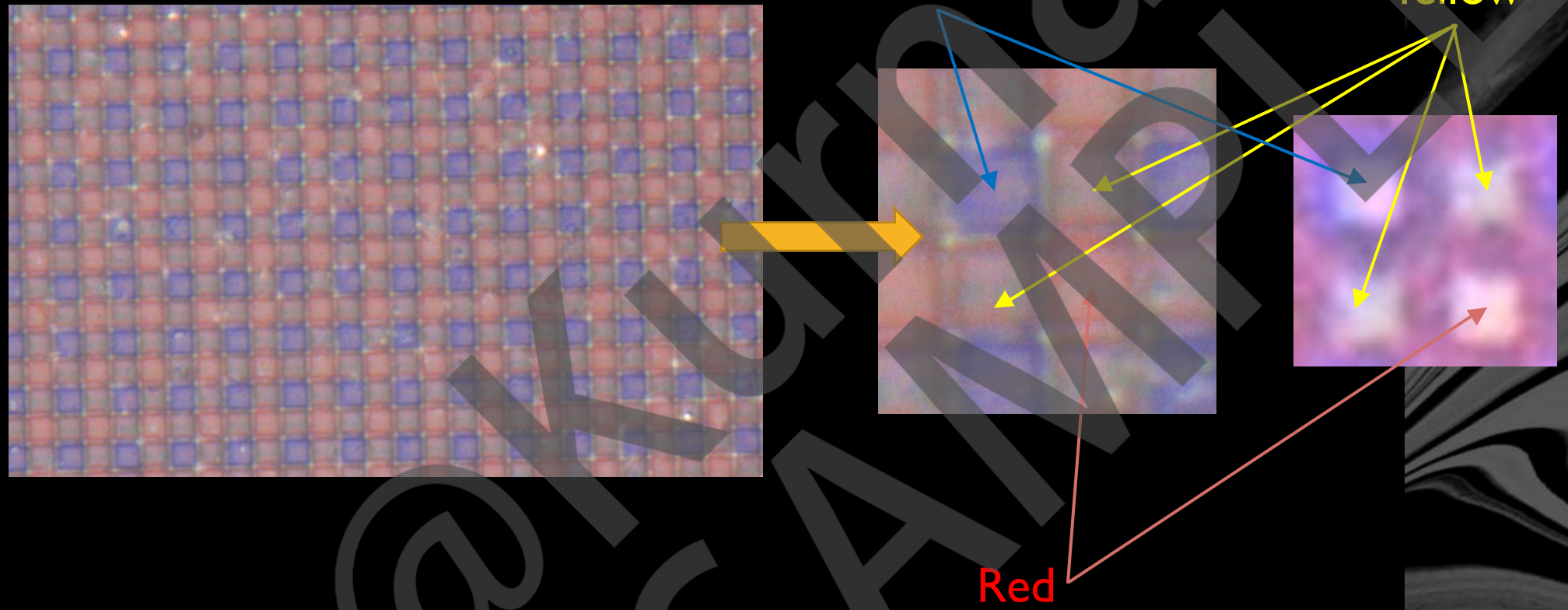
Diagonal line size: 12.606mm
(Nearly 1/1.27)

MATE70PRO+ CIS(MAIN)

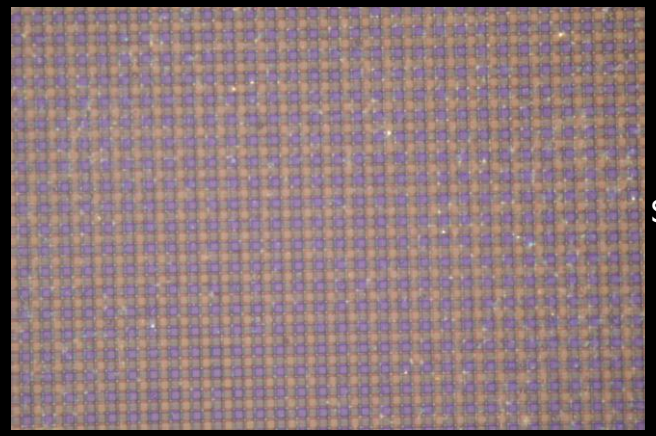
1000x in microscope



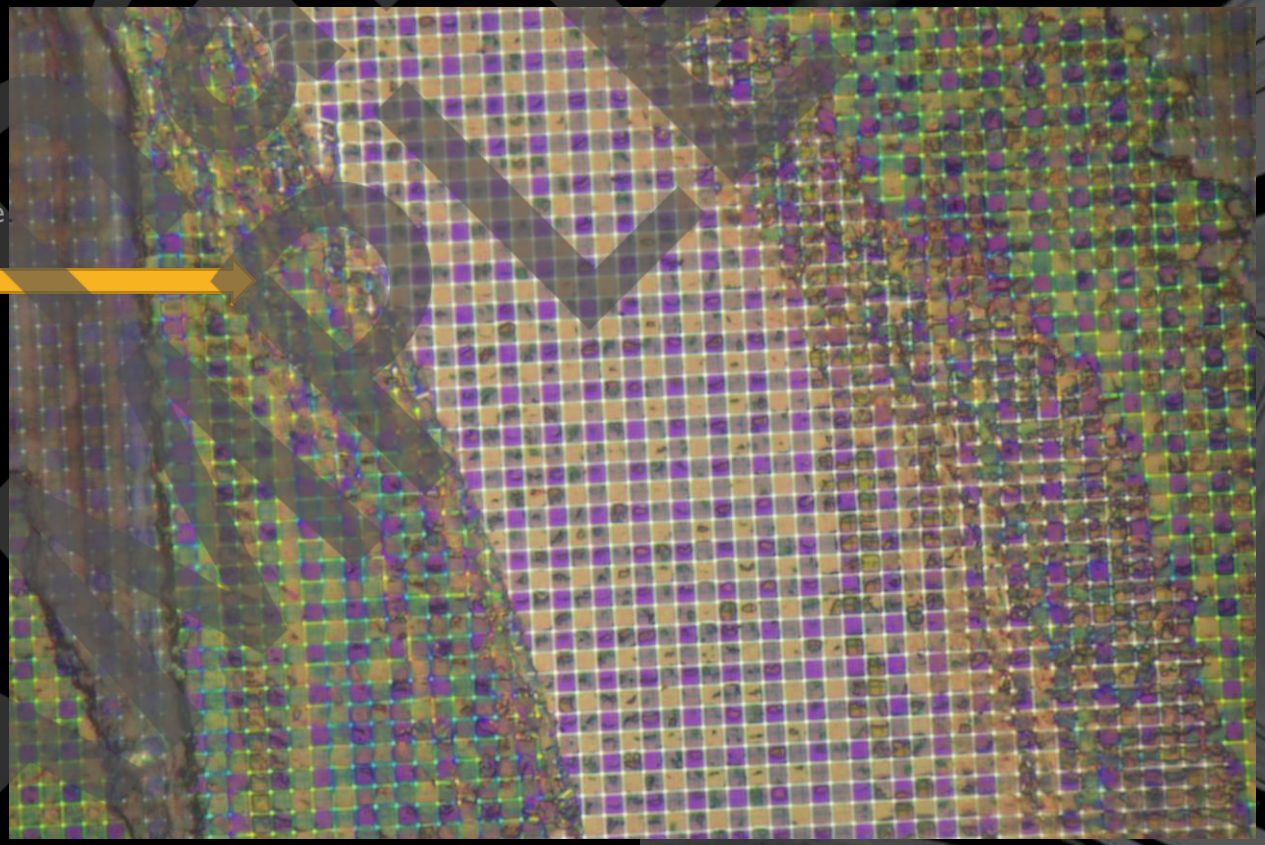
MATE70PRO+ CIS(MAIN)



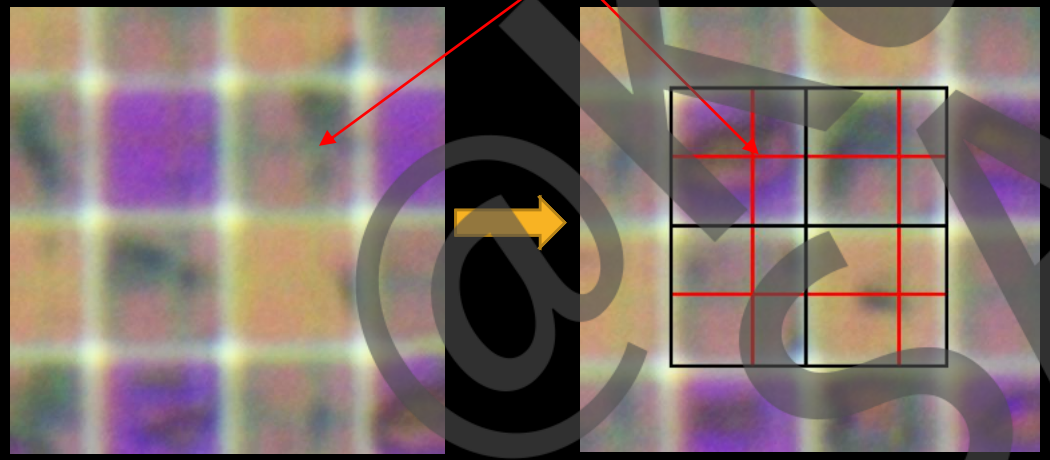
MATE7OPRO+ CIS(MAIN)



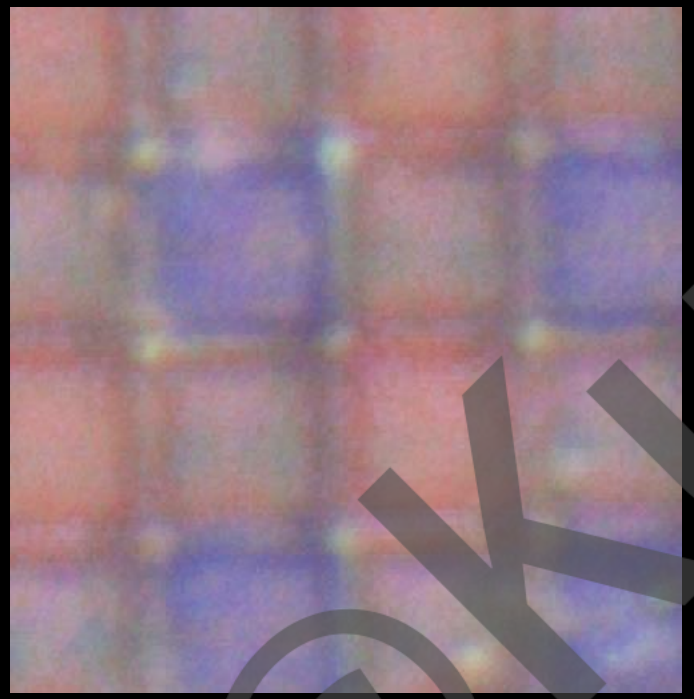
Scrape off part of the OCL with a knife



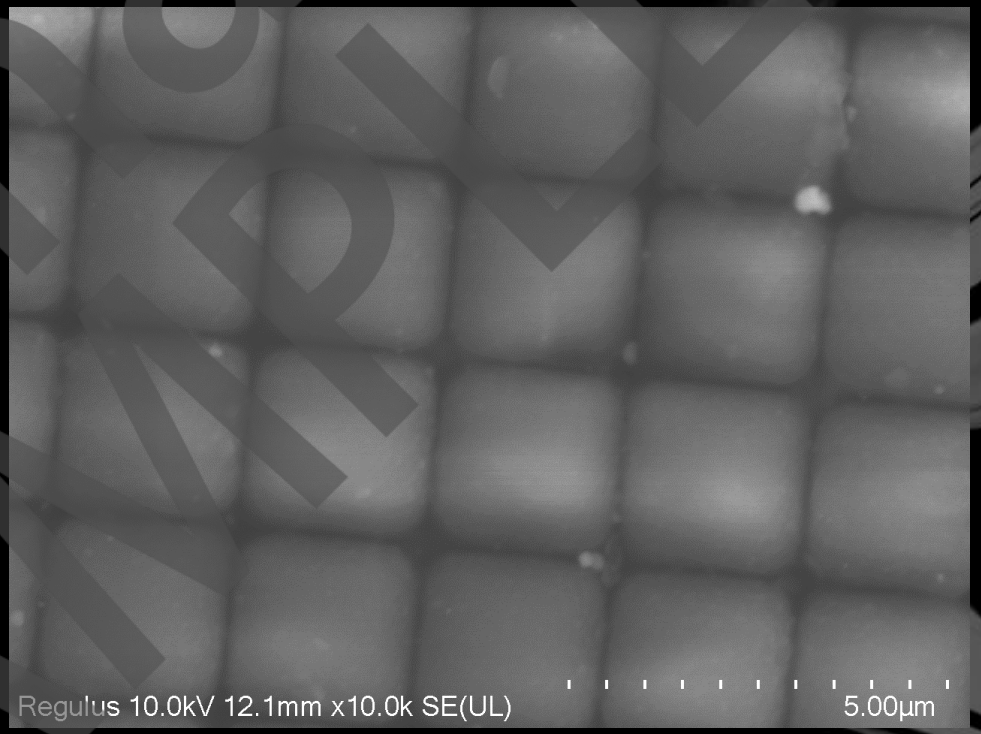
Some cut in pixel area



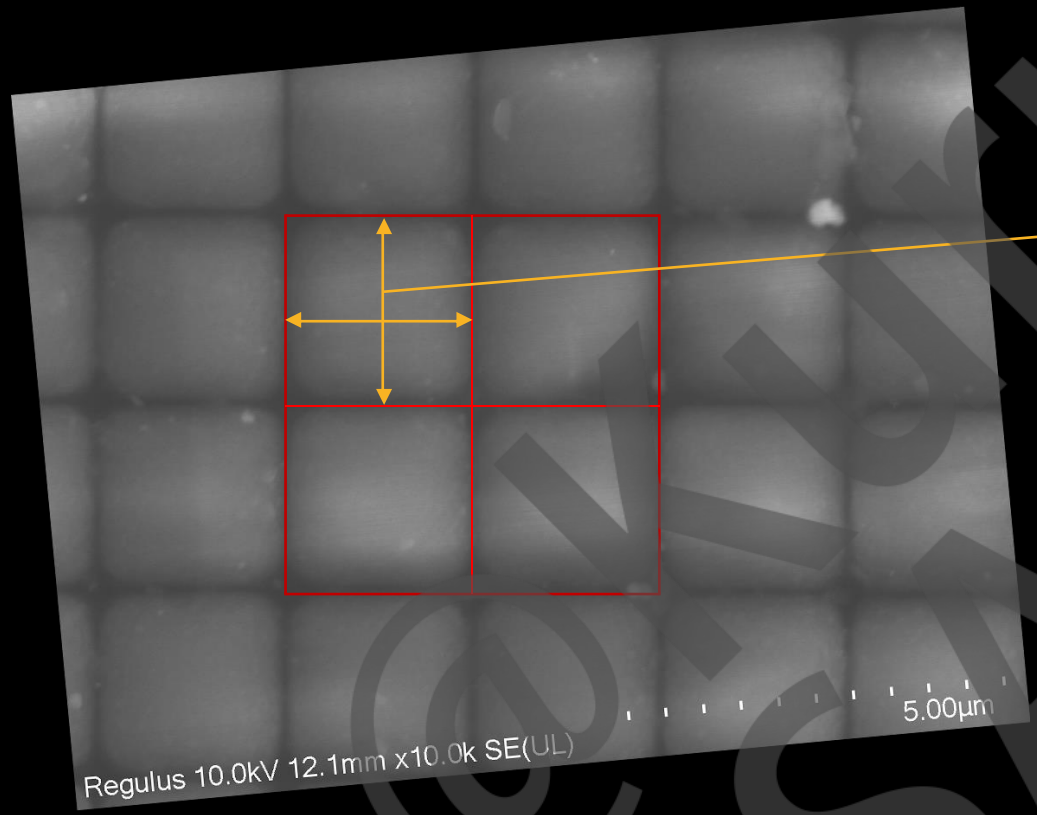
MATE70PRO+ CIS(MAIN)



SEM Photo Hitachi Su8200

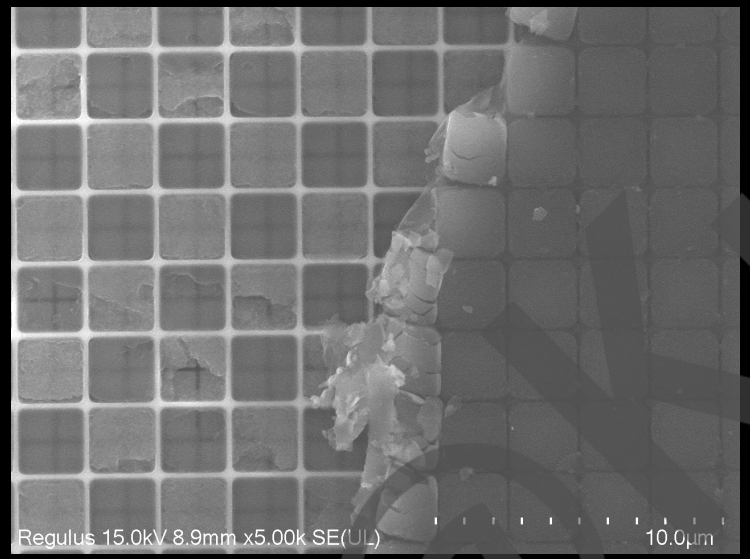


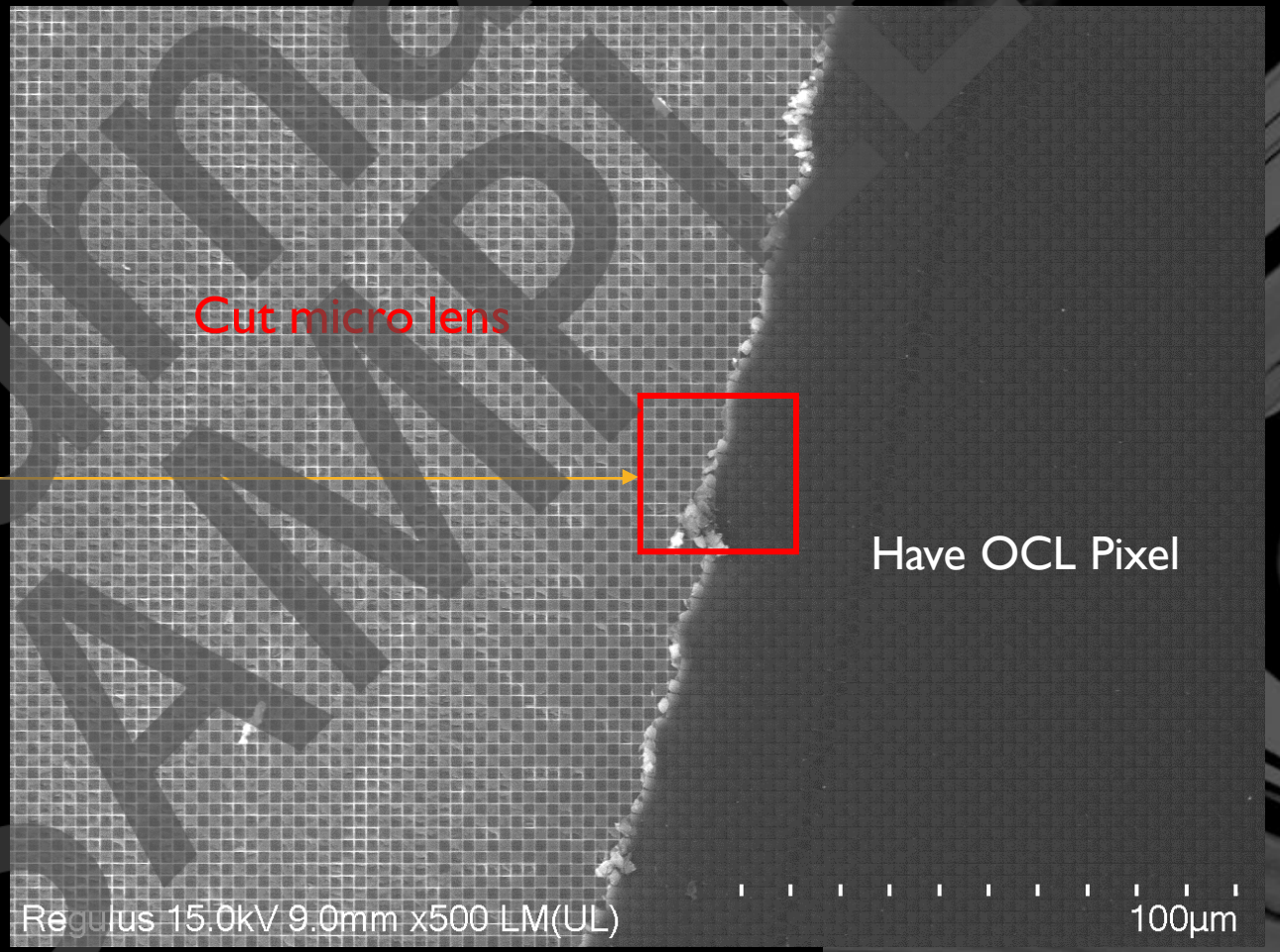
MATE70PRO+ CIS(MAIN)



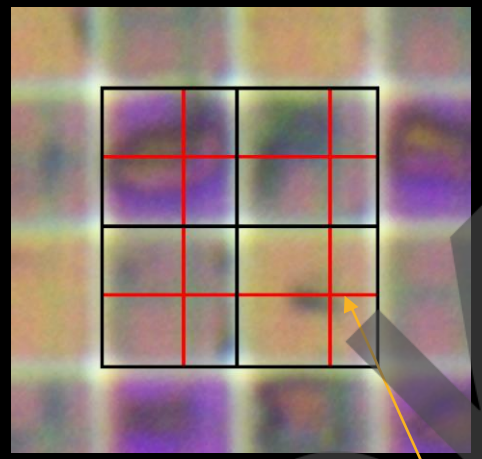
Pixel side length:2.471um

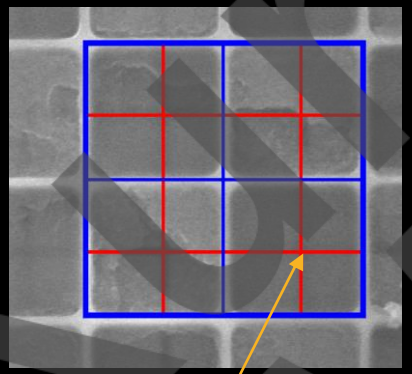
MATE70PRO+ CIS(MAIN)



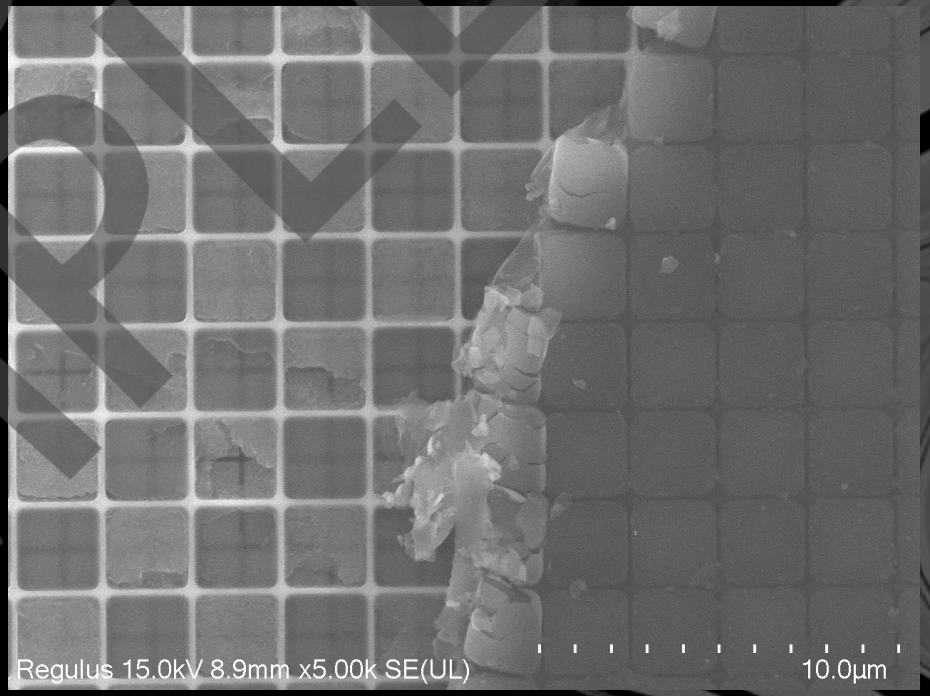


MATE7OPRO+ CIS(MAIN)

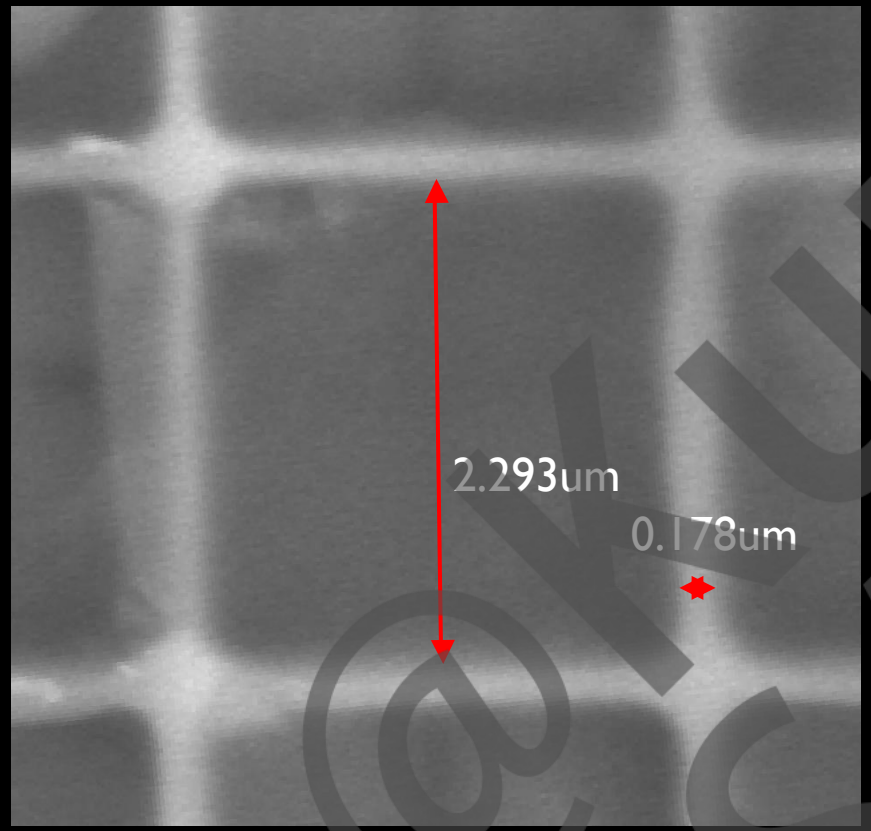




Cut line?

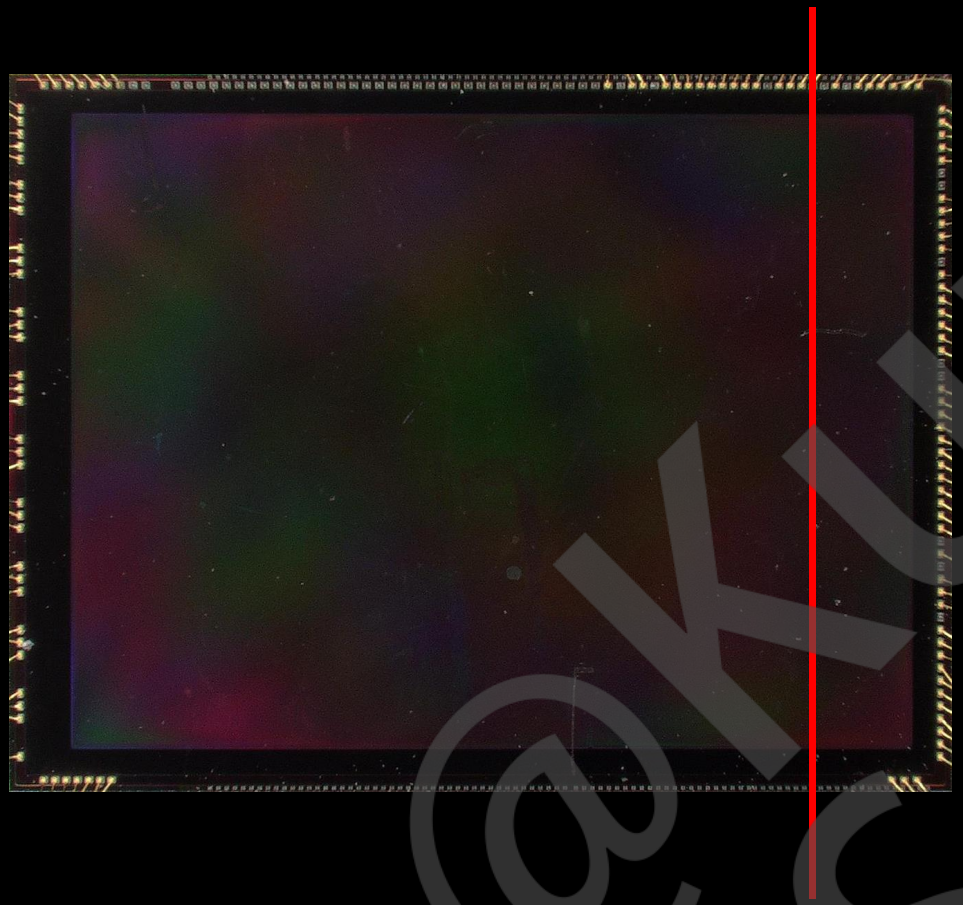


MATE70PRO+ CIS(MAIN)



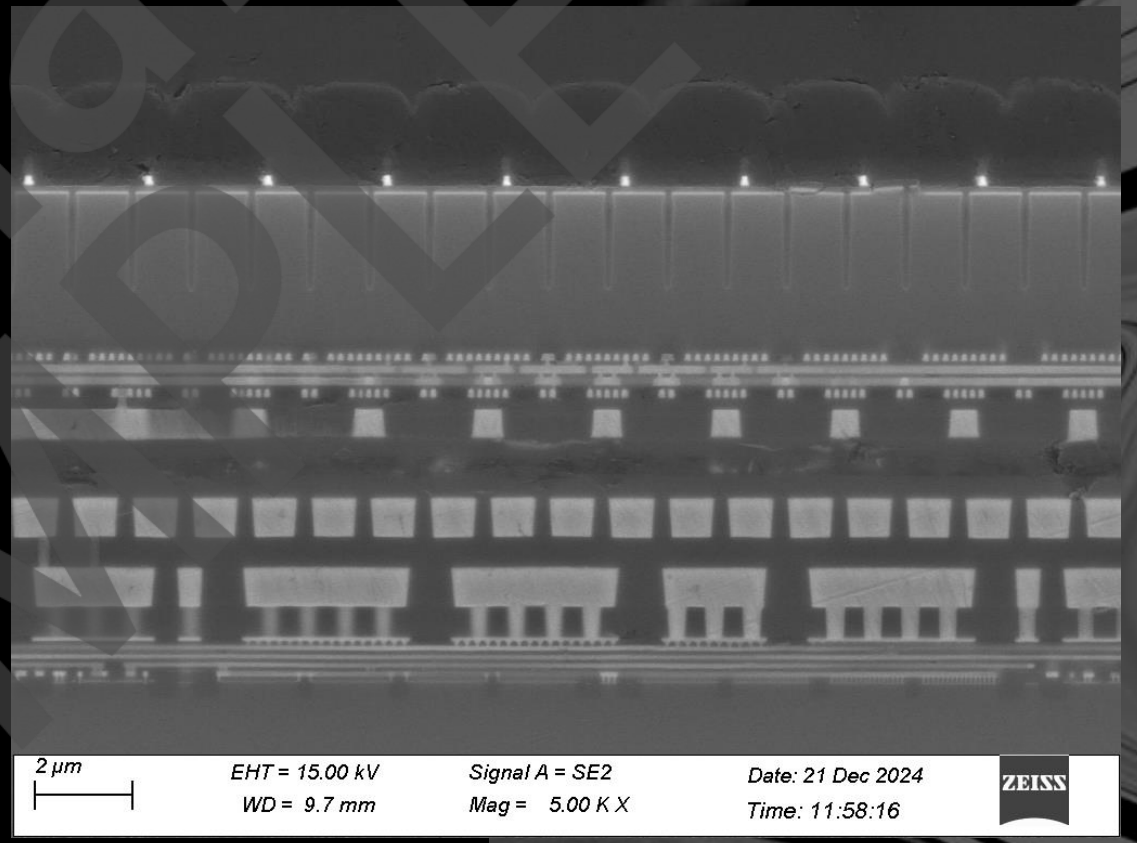
Trap size: 2.293um
Trap well size: 0.178um

MATE70PRO+ CIS(MAIN)



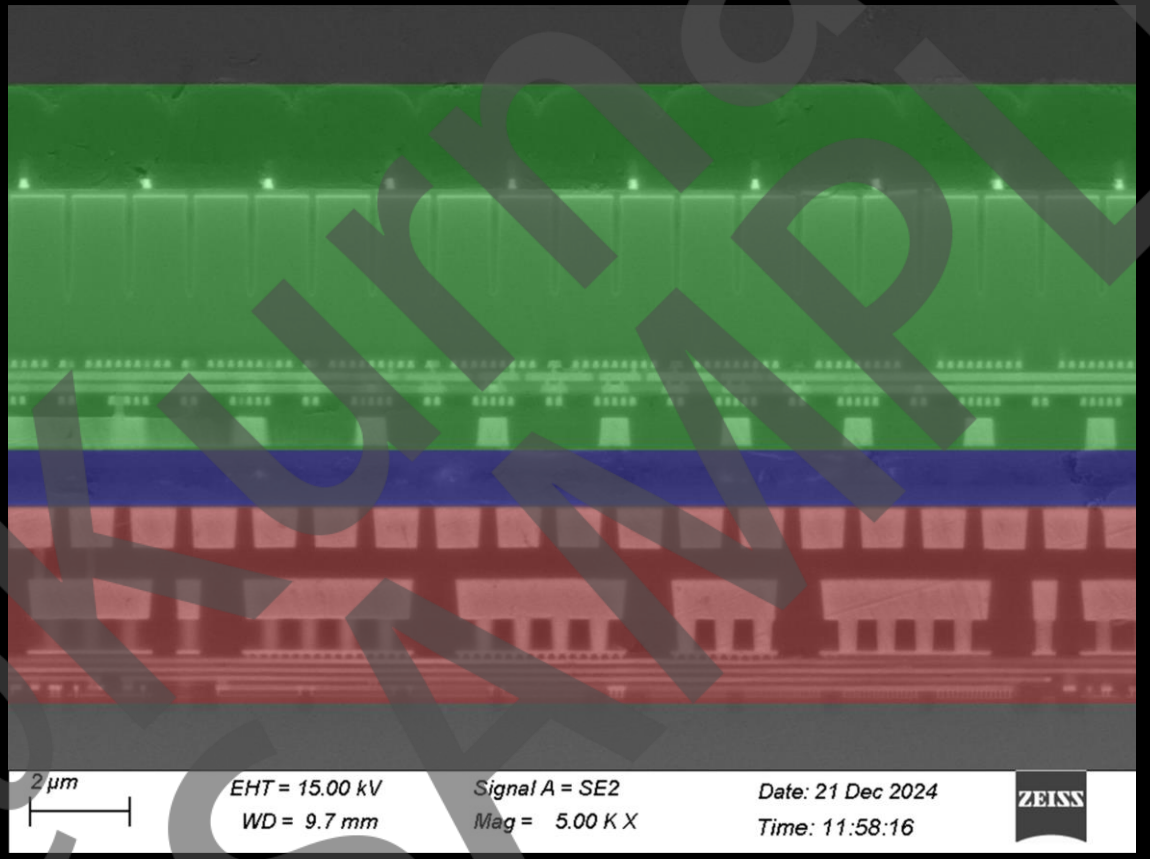
Package in X Cut

MATE70PRO+ CIS(MAIN)



MATE70PRO+ CIS(MAIN)

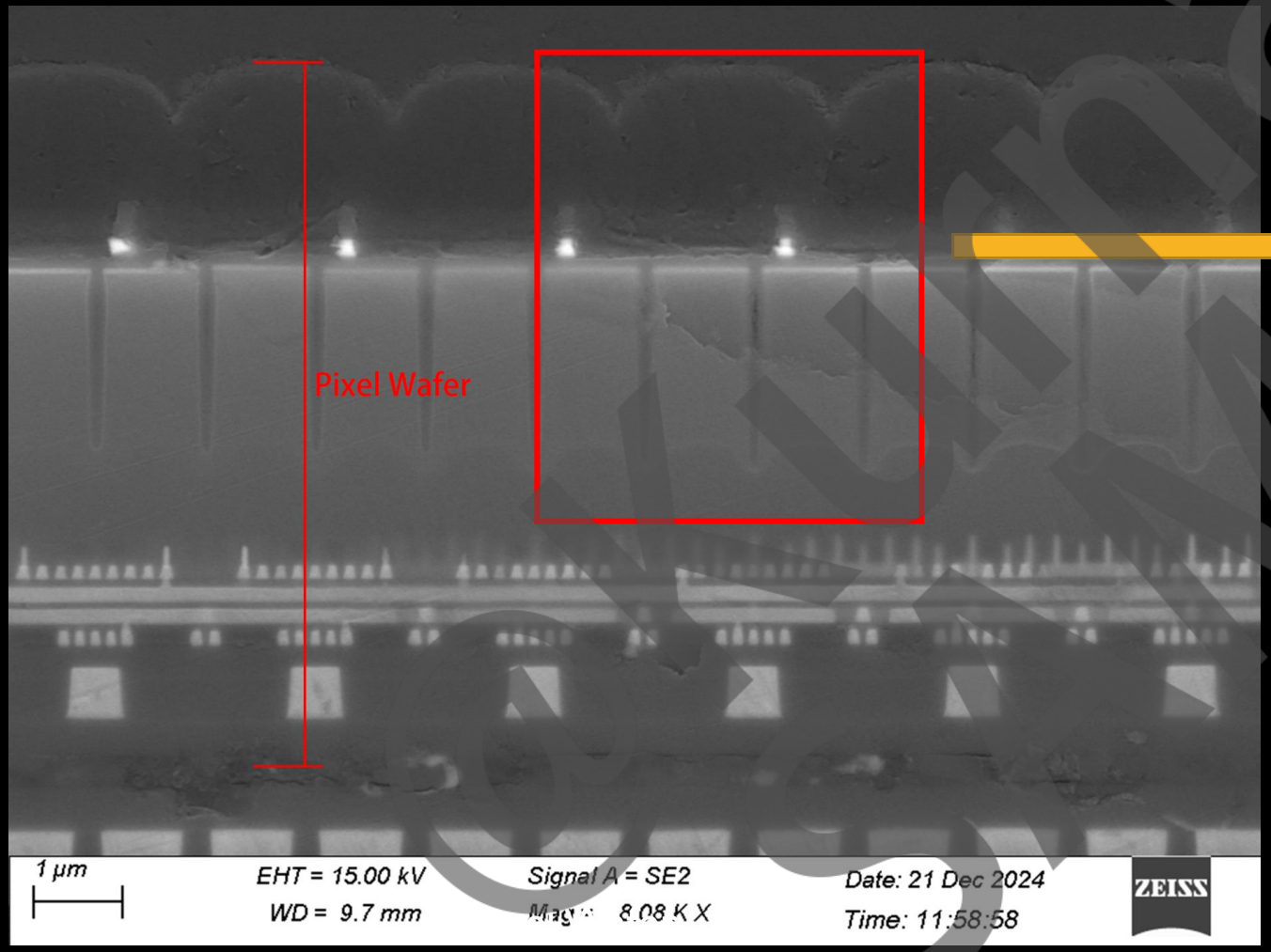
Total Height: 12.741um
Pixel wafer Height: 7.853um
Logic wafer Height: 4.905um

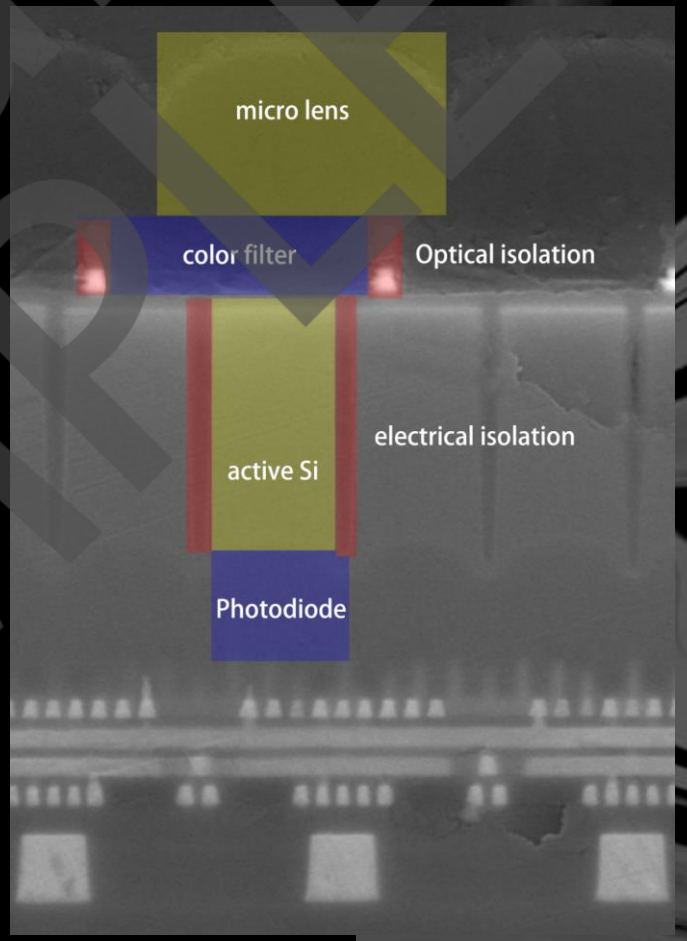


Pixel Wafer

Logic Wafer

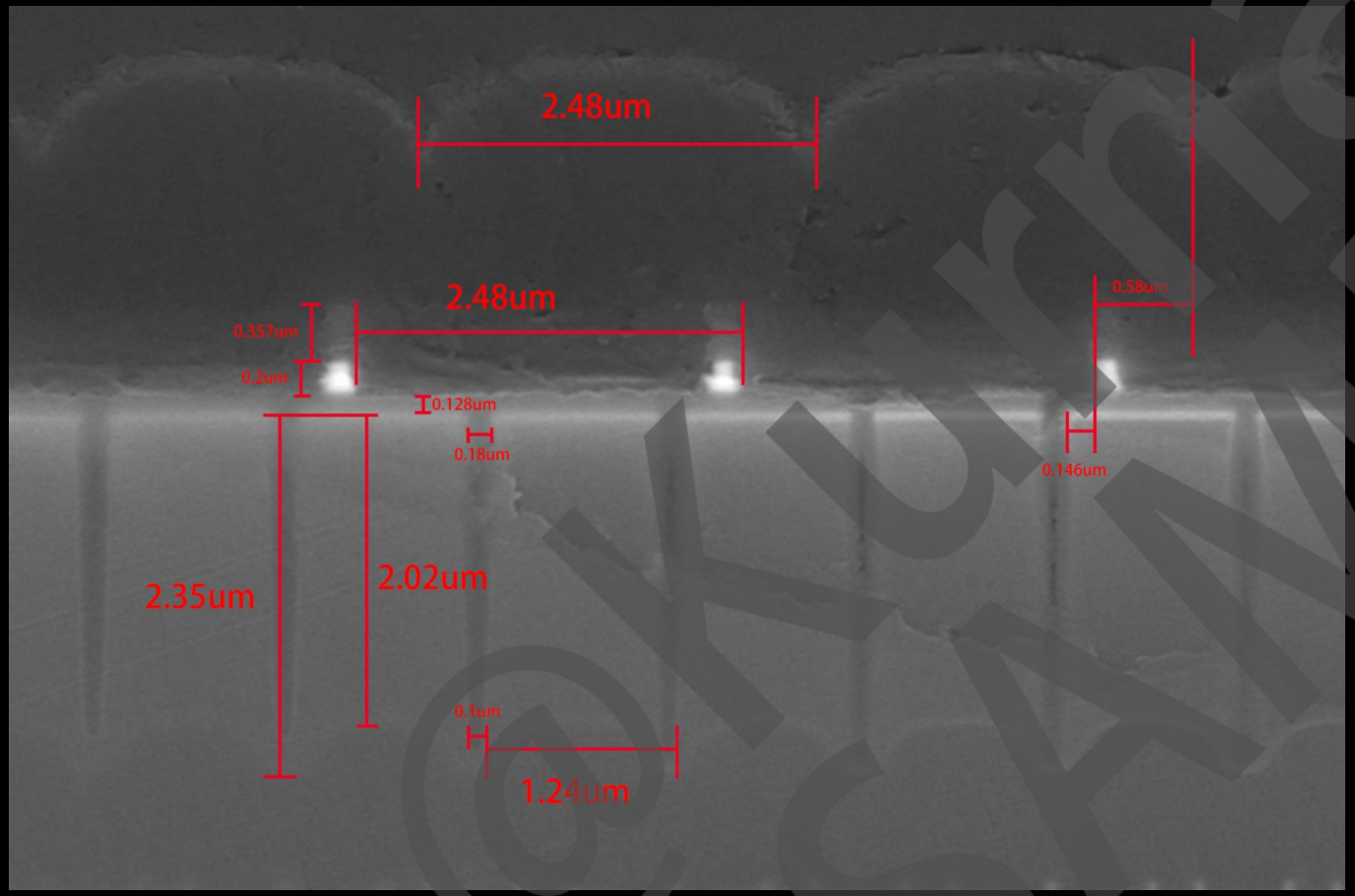
MATE70PRO+ CIS(MAIN)





Optical Layers

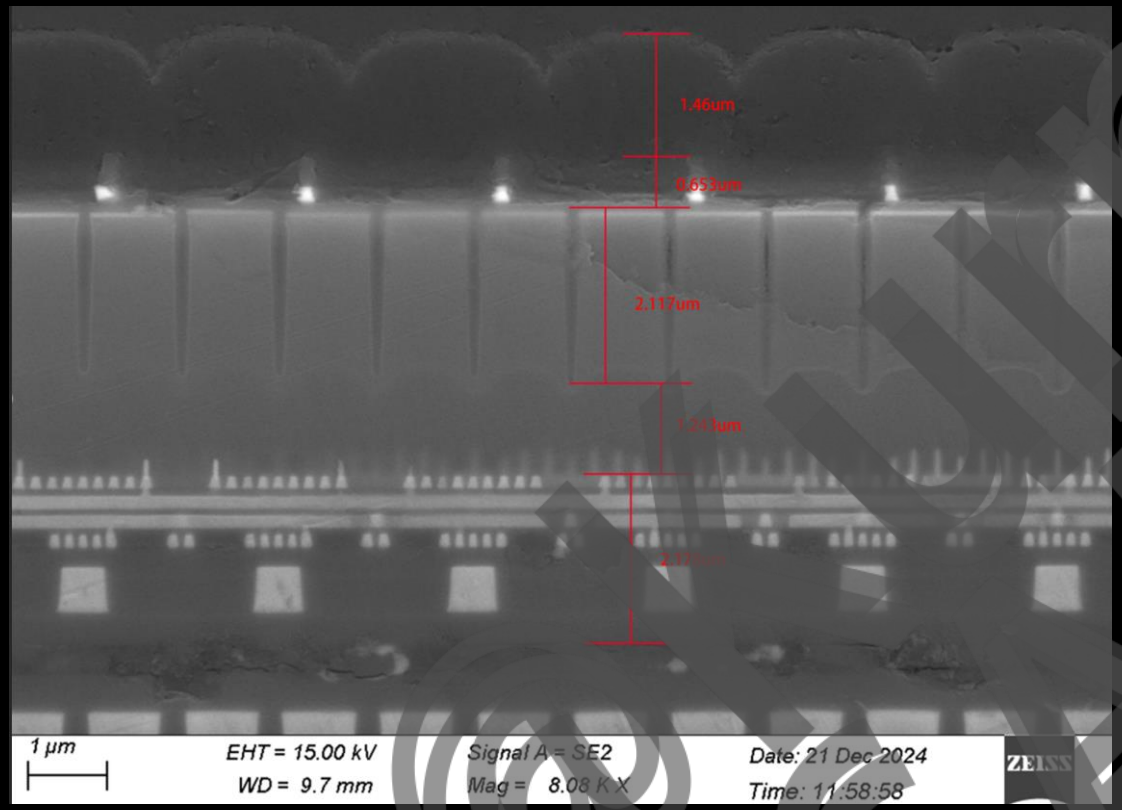
MATE70PRO+ CIS(MAIN)



Mate70P+ Pixel Wafer

Micro Lens size:	2.48um
Color Filter size:	2.48um
Photodiode size:	1.24um
Optical isolation deep:	0.357um+0.2um
Electrical isolation deep:	2.35um/2.02um
Electrical isolation top width:	0.18um
Electrical isolation down width:	0.1um
Micro lens- Color filter pitch:	0.58um
Optical - electrical pitch:	0.146um

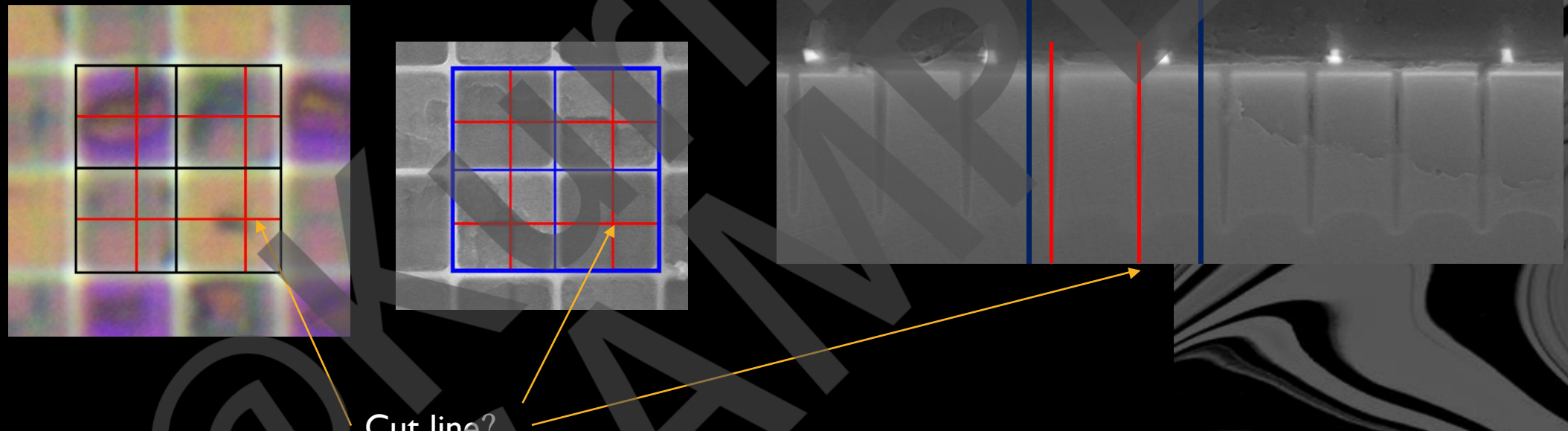
MATE70PRO+ CIS(MAIN)



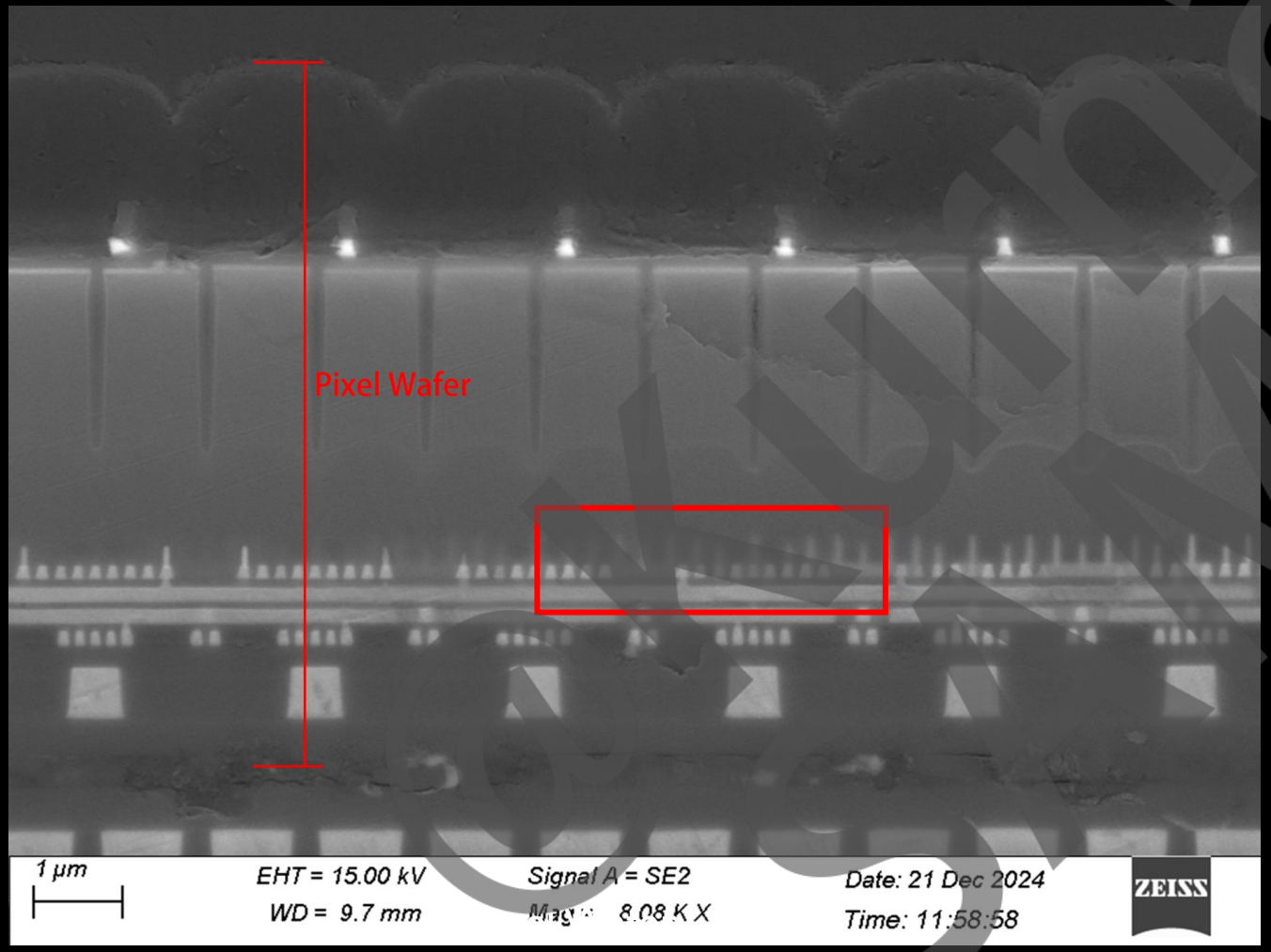
Mate70P+ Pixel Wafer

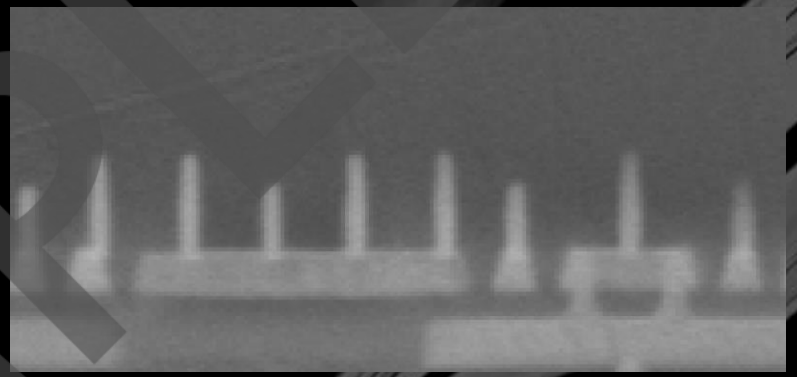
Micro lens Height:	1.46um
Color filter Height:	0.653um
Electrical isolation Depth:	2.117um
Photodiode top to M1 distance:	1.243um
Metal 1 to bond distance:	2.178um

MATE7OPRO+ CIS(MAIN)



MATE70PRO+ CIS(MAIN)

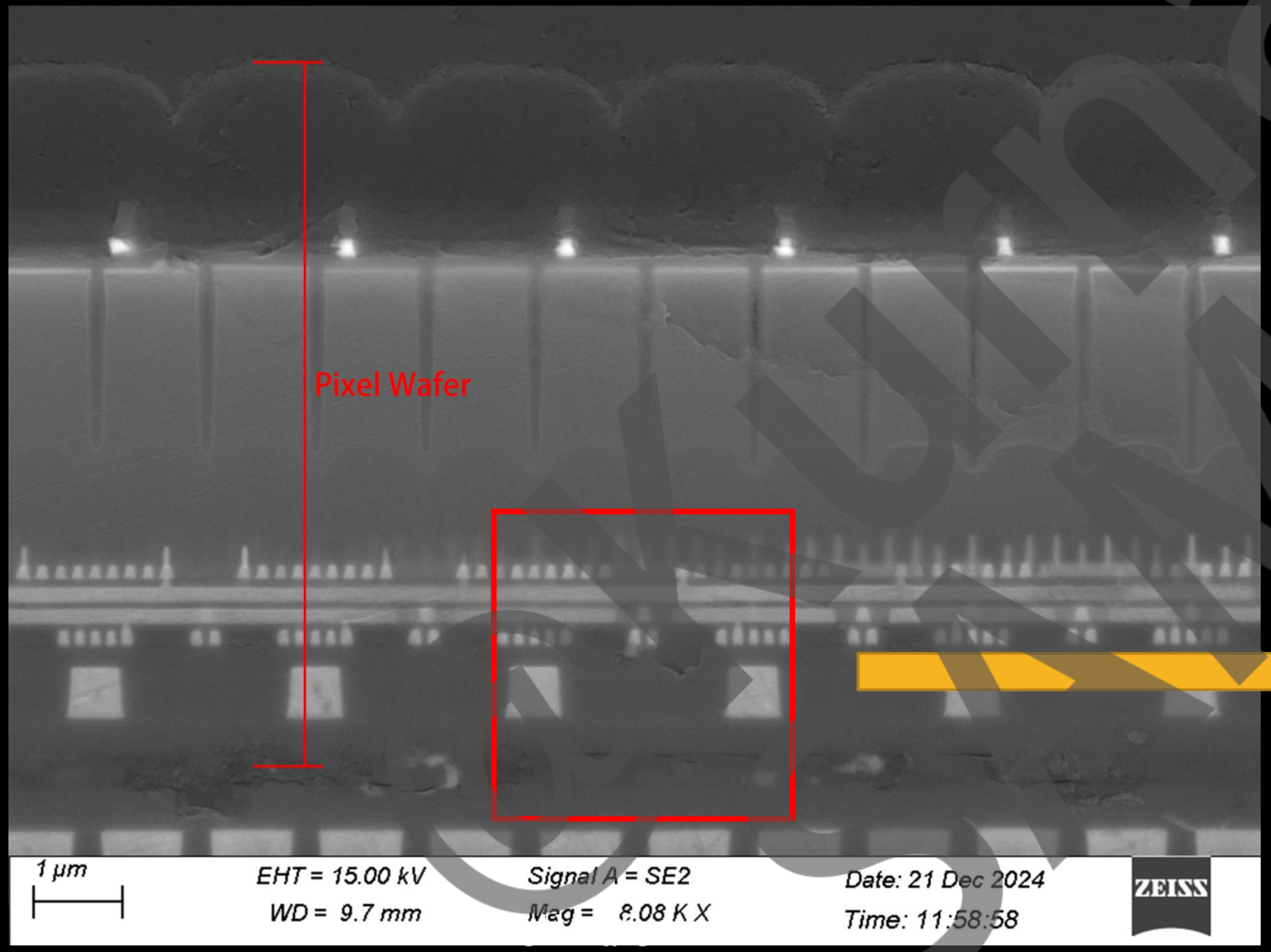




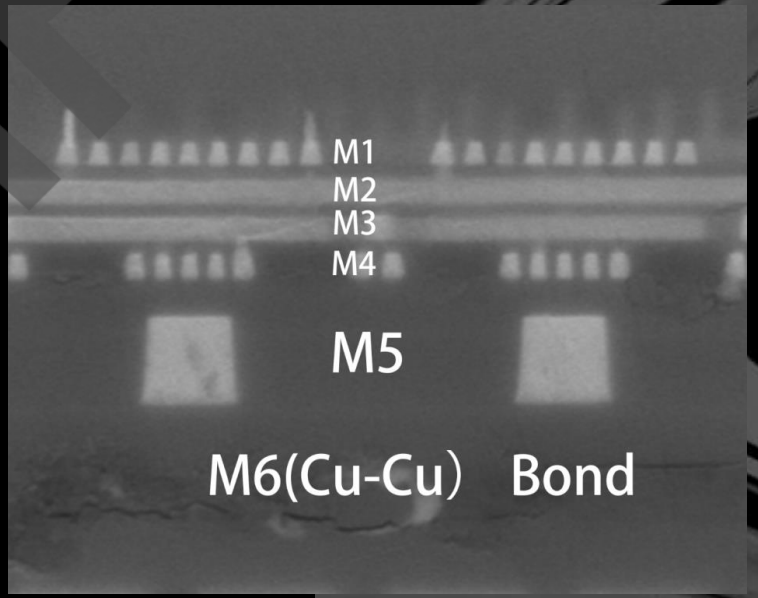
Like VTG?

Optical Layers

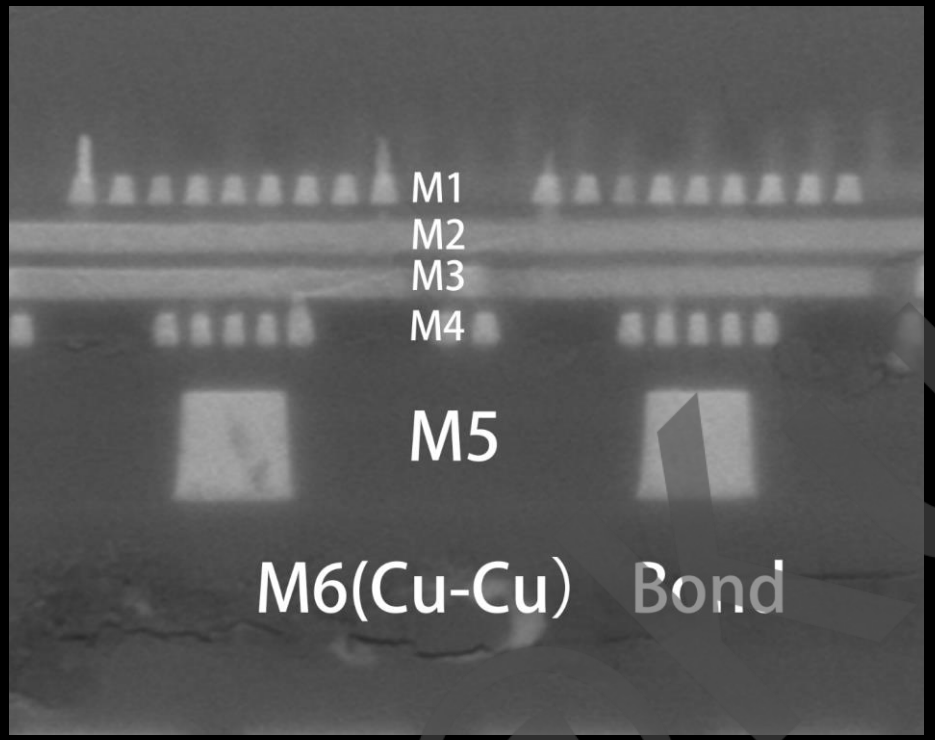
MATE70PRO+ CIS(MAIN)



Metal Layers in Pixel Wafer: 6 layers



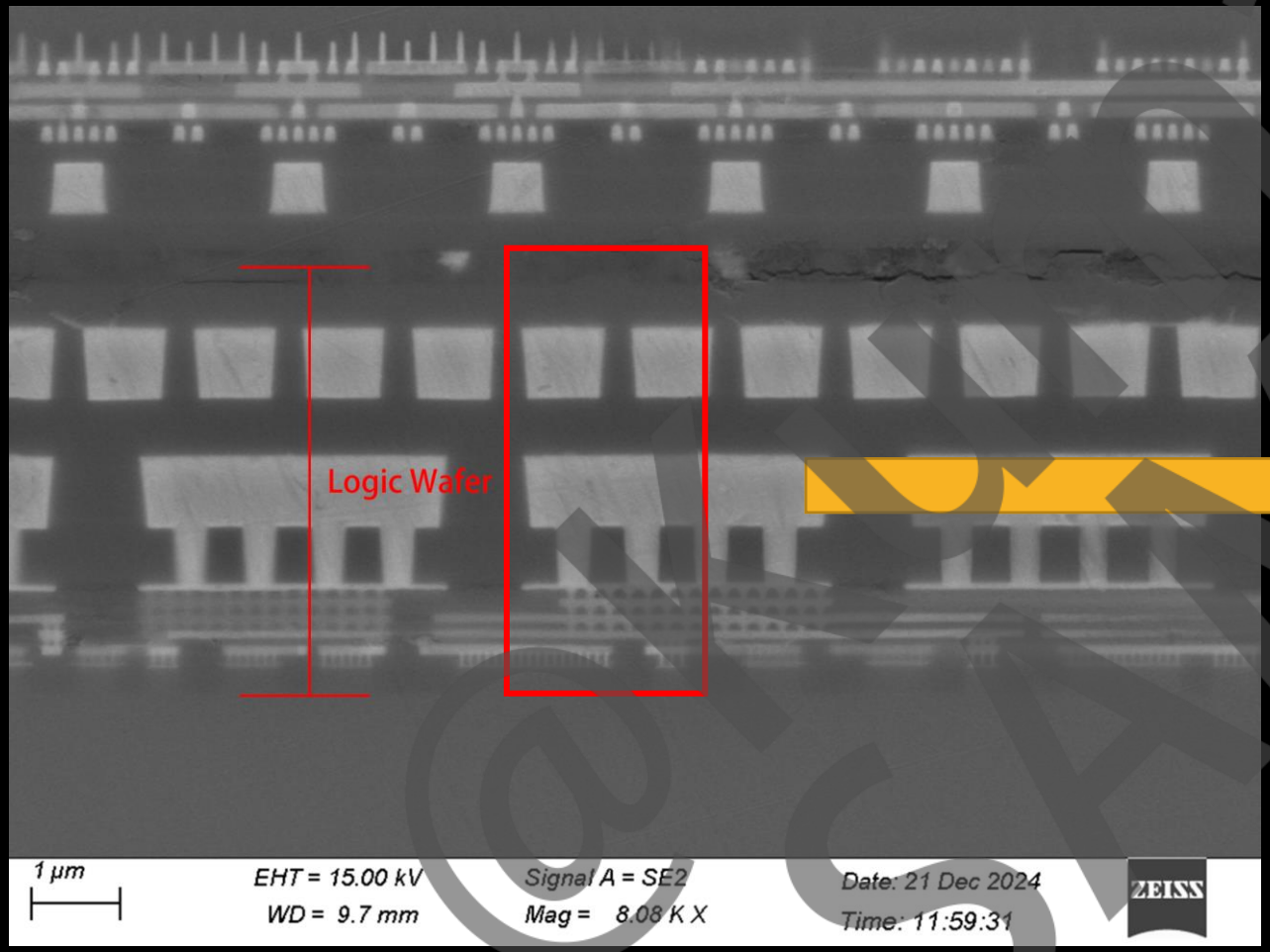
MATE70PRO+ CIS(MAIN)

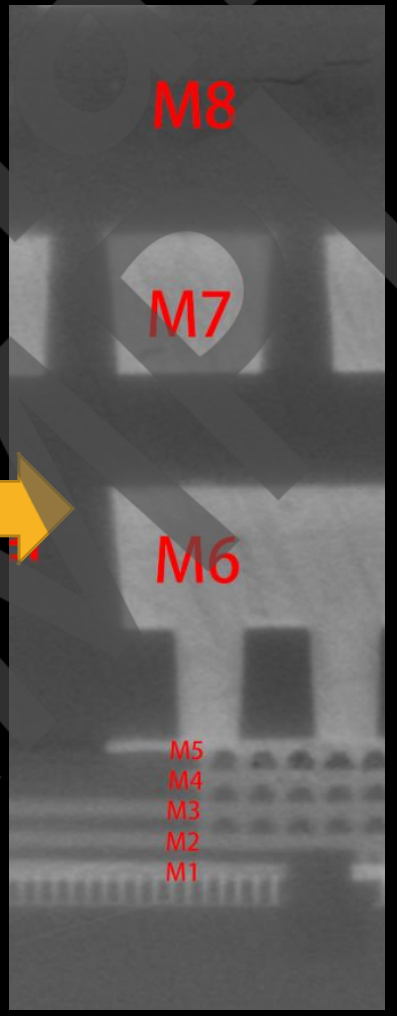


	(Just)Thickness	Pitch
M1	162nm	198.6nm
M2	162nm	x
M3	162nm	x
M4	162nm	177nm
M5	561nm	2470nm
M6	351nm	x

Mate70pro+ CIS Pixel Metal Data

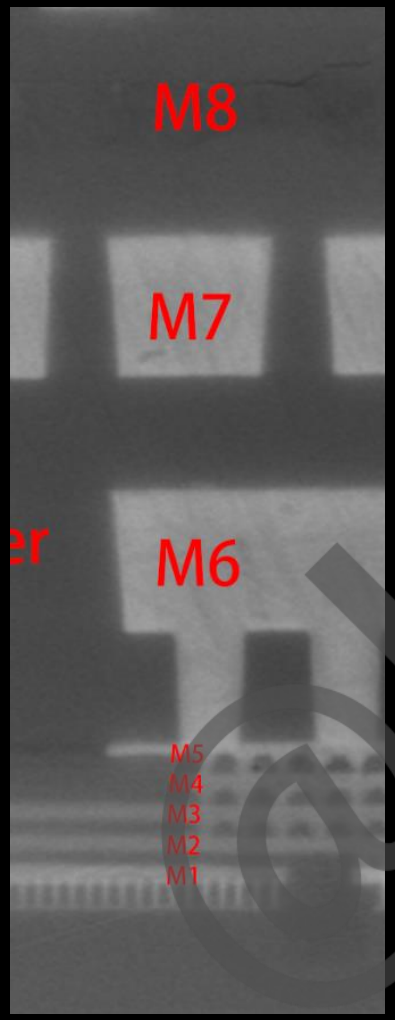
MATE70PRO+ CIS(MAIN)





Logic wafer have 8 Metal Layers

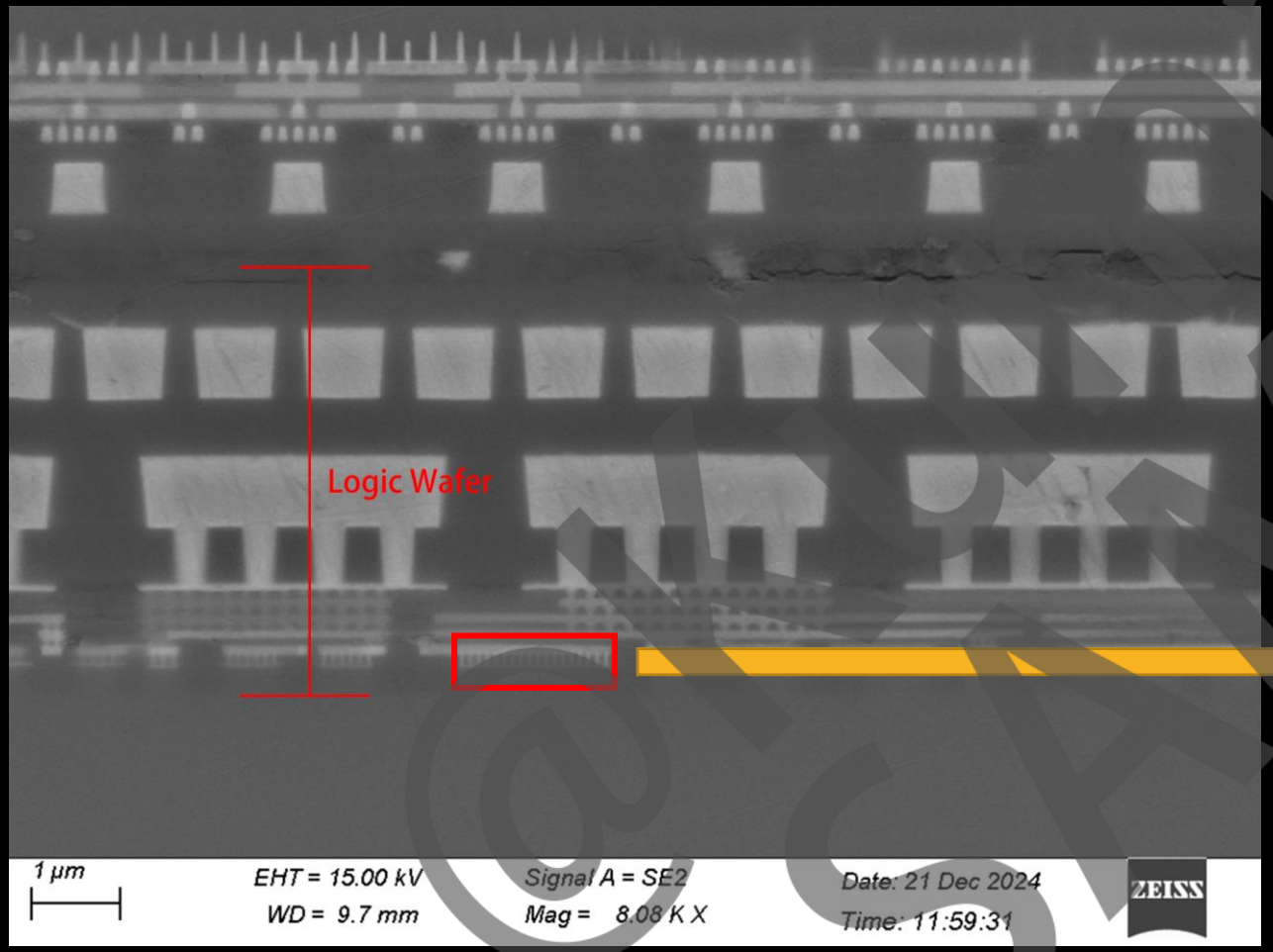
MATE70PRO+ CIS(MAIN)



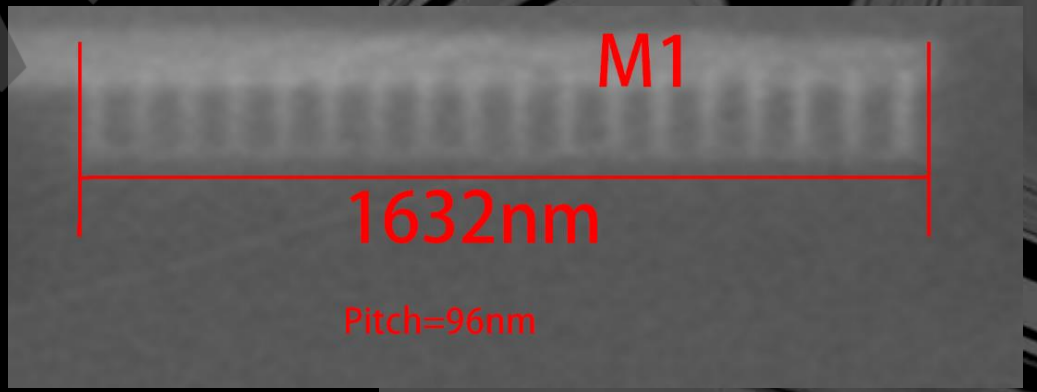
	(Just)Thickness	Pitch
M1	83nm	x
M2	83nm	x
M3	83nm	x
M4	83nm	x
M5	83nm	x
M6	802nm	x
M7	793nm	1236nm
M8	348nm	x

Mate70pro+ CIS LogicMetal Data

MATE70PRO+ CIS(MAIN)



Via Pitch 96nm

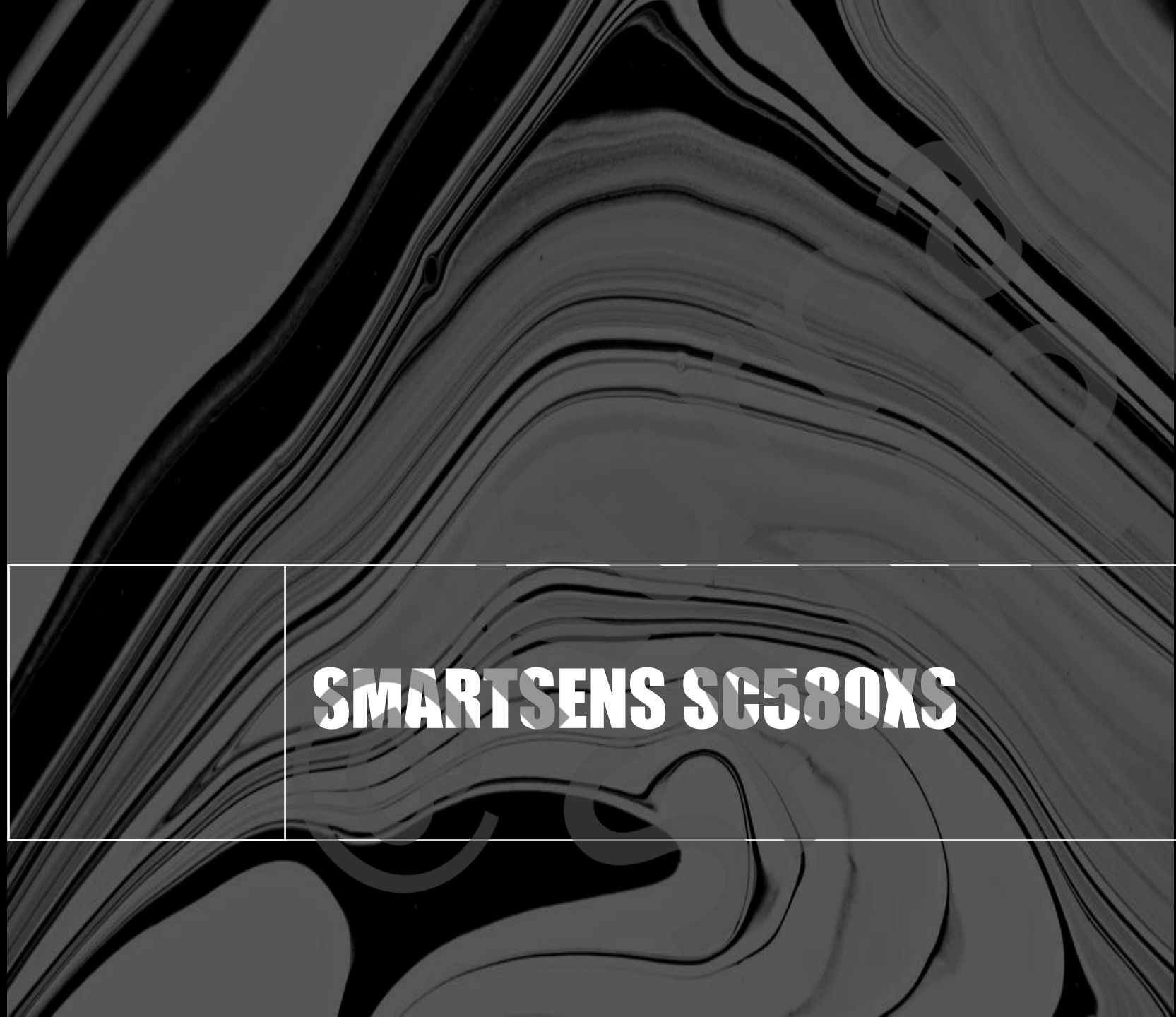


MATE70PRO+ CIS(MAIN)

Some People says this Cis is Smartsens Sc580xs

How to make sure that?

Buy it!



SMARTSENS SC580XS

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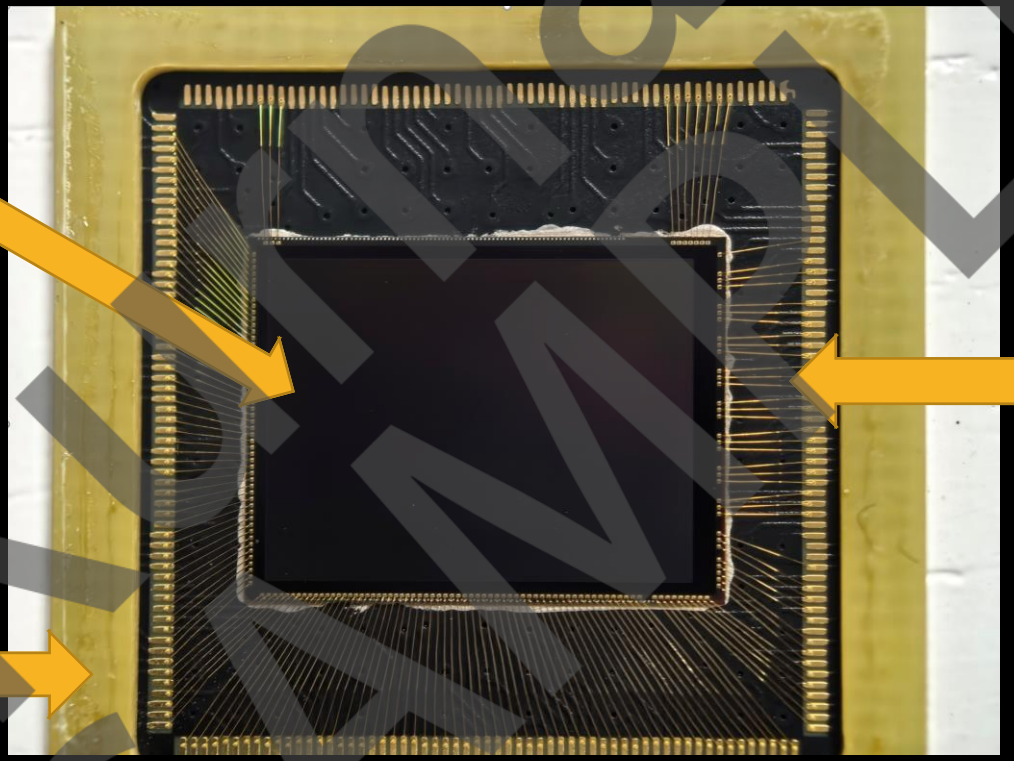
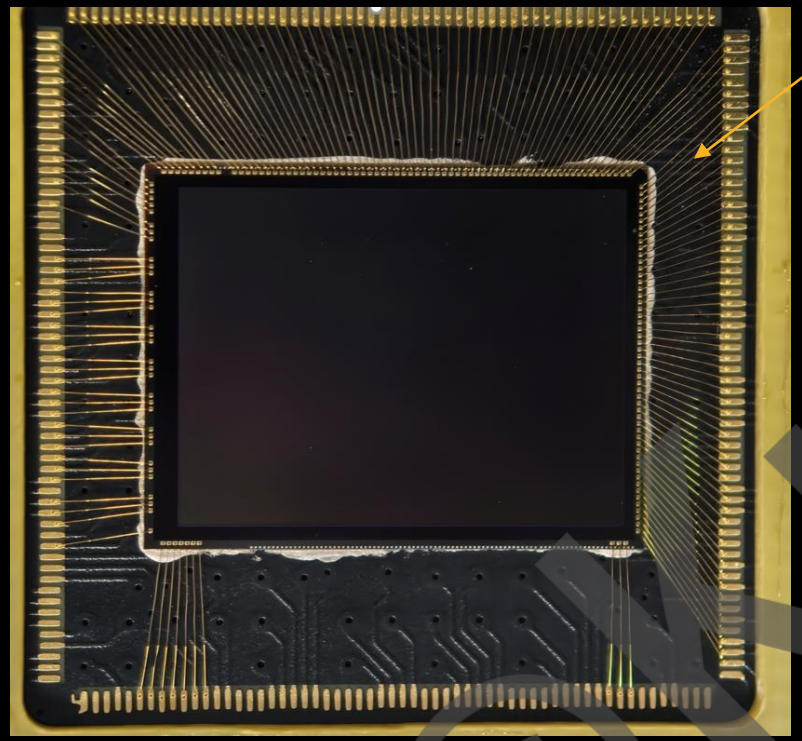
Cmos Die
50mp



Bonding Out

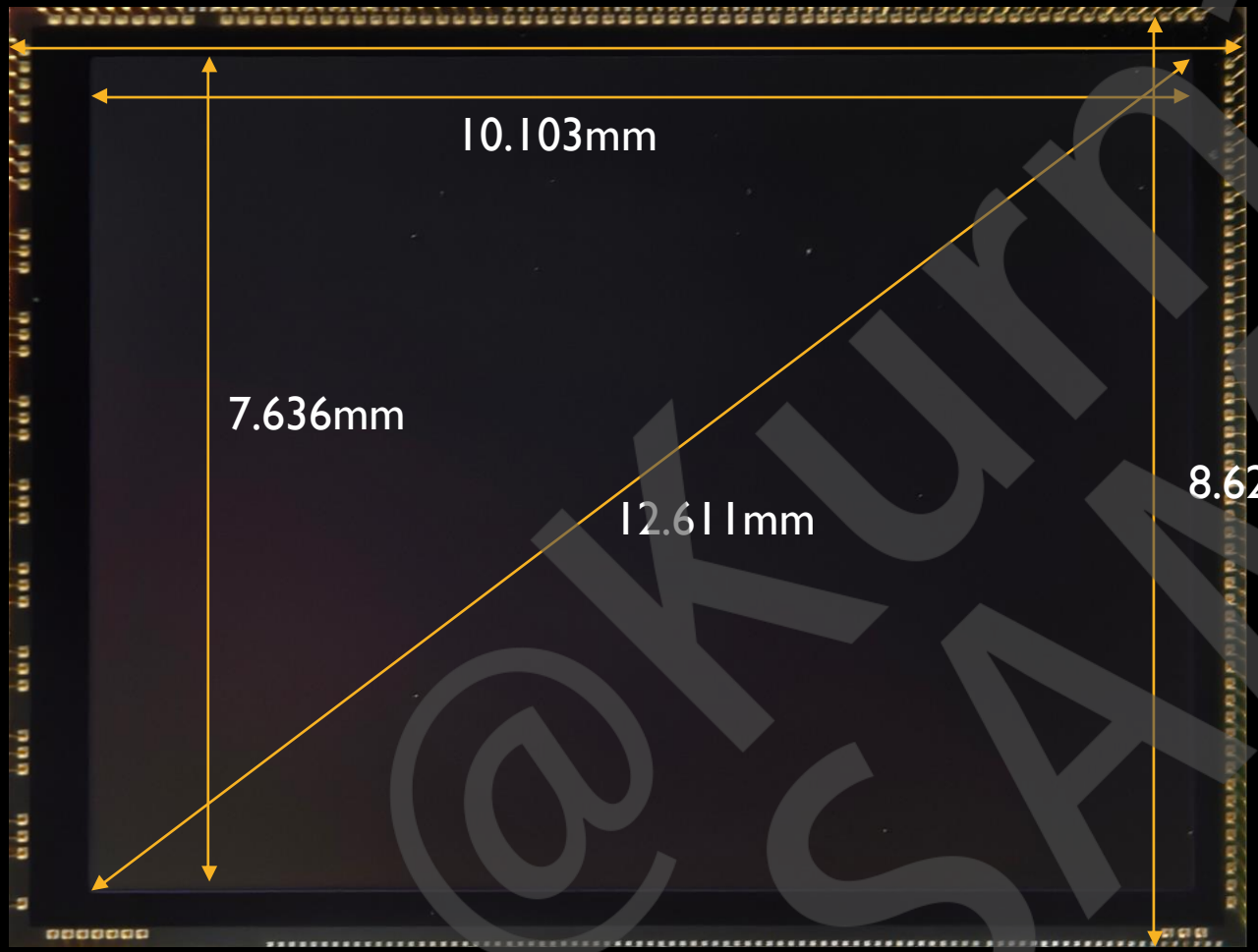
Cmos substrate & PCB

SMARTSENS SC580XS



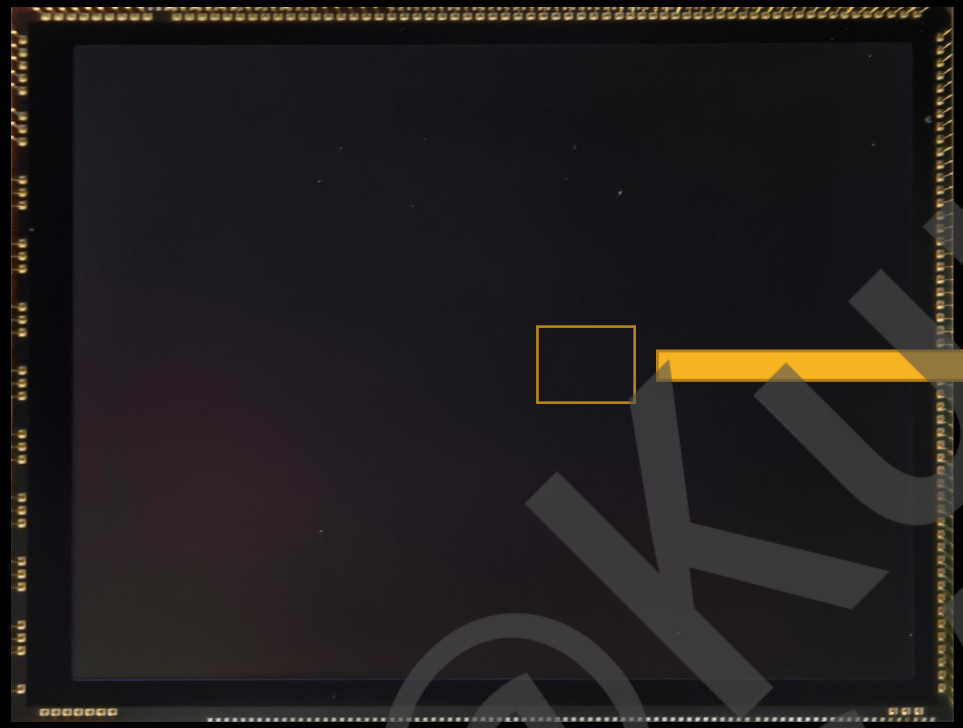
Bonding Pad number: 166
Bonding Pad in use: 166

SMARTSENS SC580XS

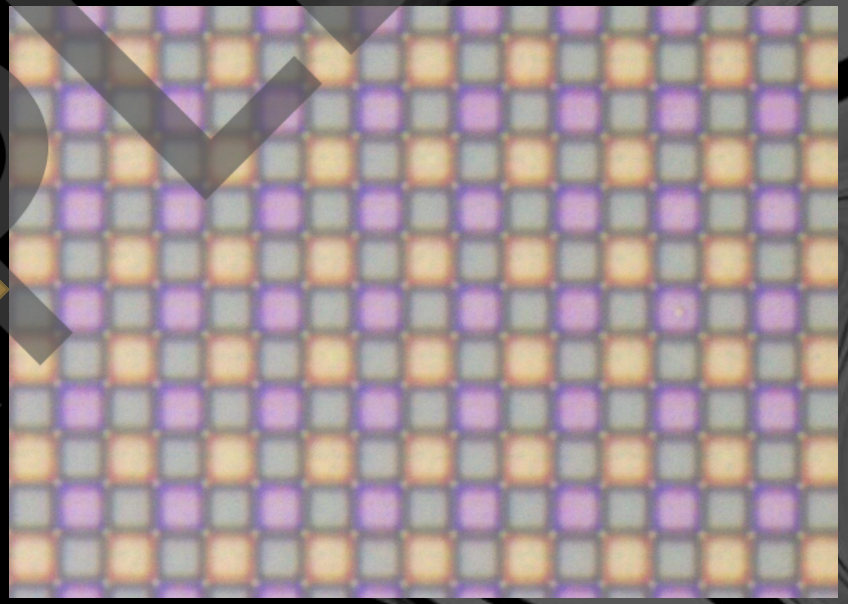


Full diesize :	97.49mm2 (11.31x8.62)
Pixel area:	77.15mm2 (10.103*7.636)
Diagonal line size:	12.611mm (Nearly 1/1.27)

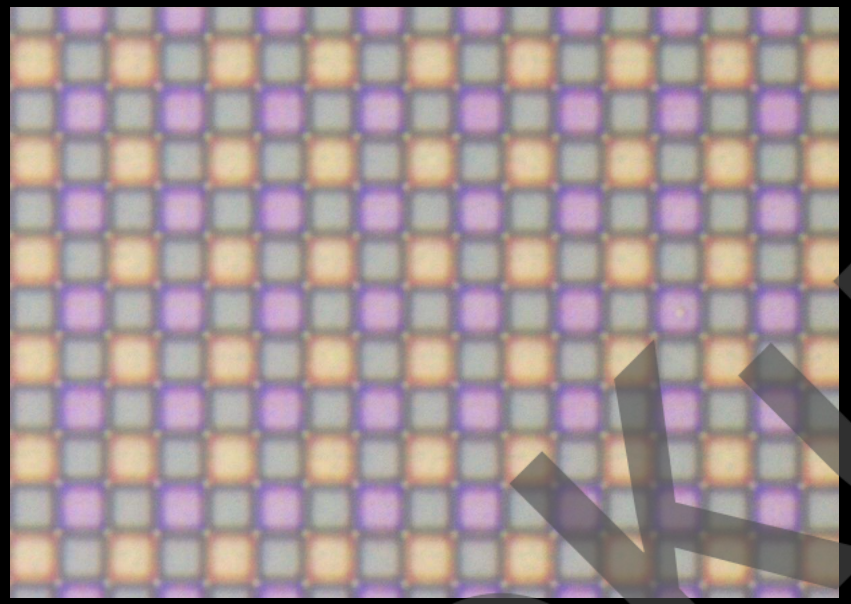
SMARTSENS SC580XS

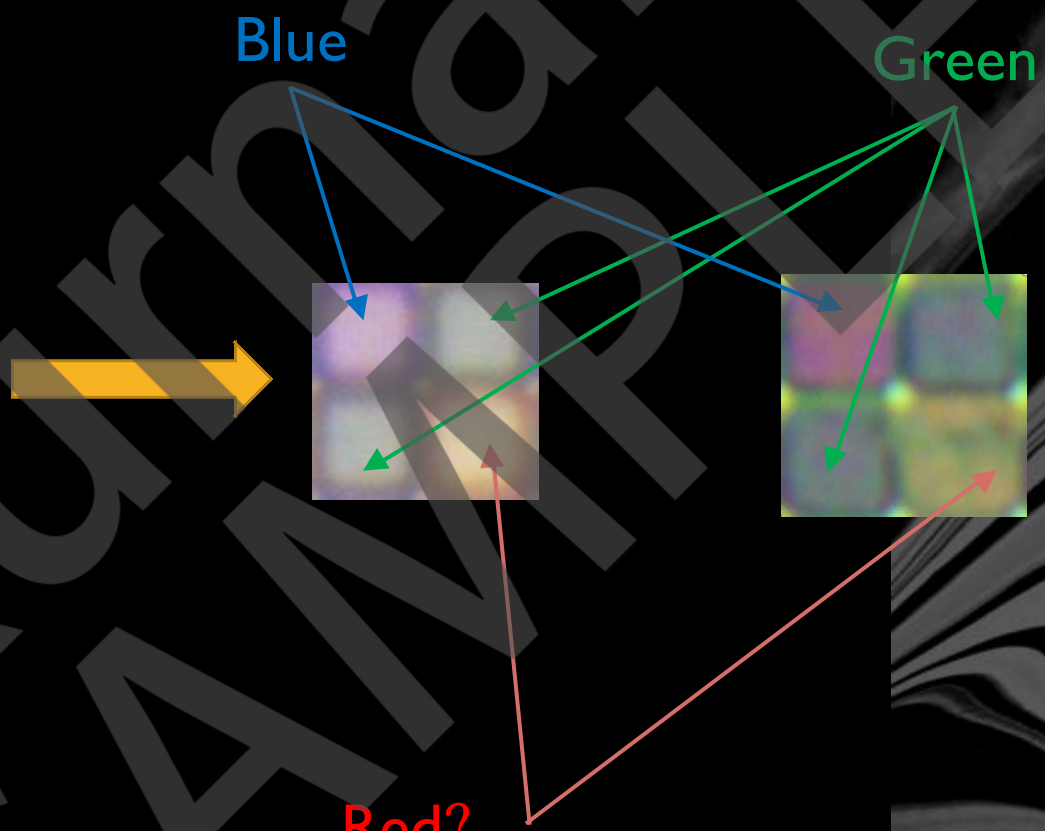


1000x in microscope



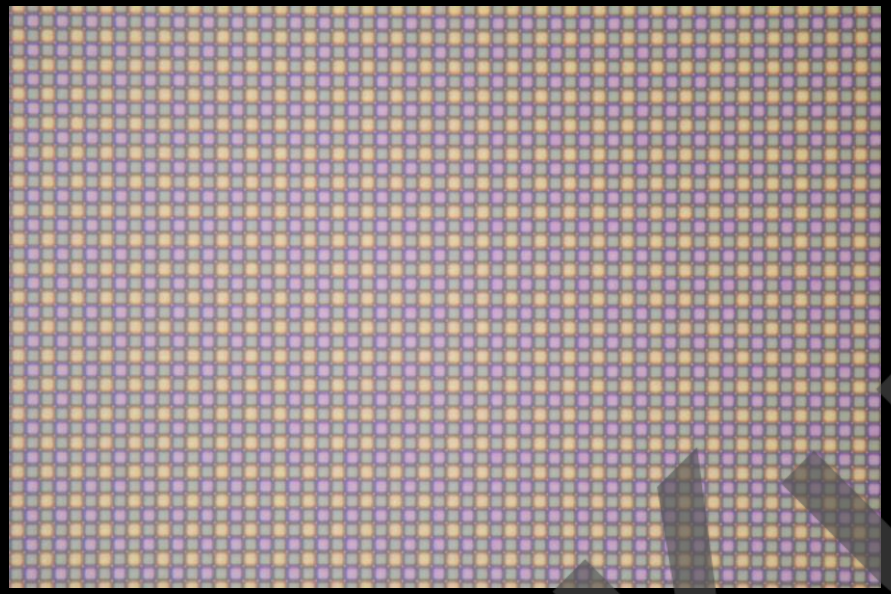
SMARTSENS SC580XS



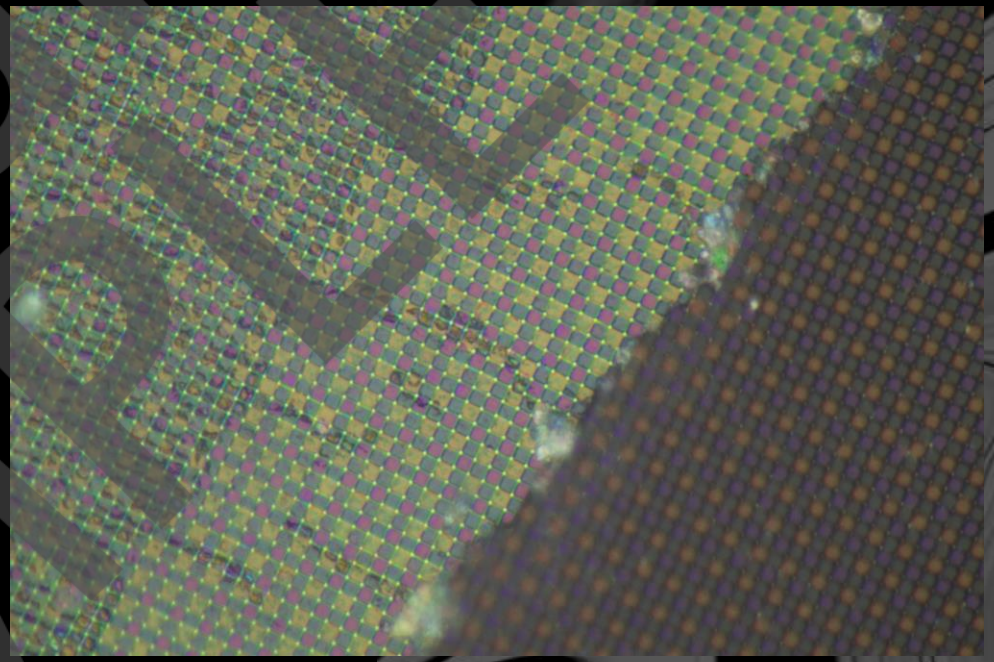


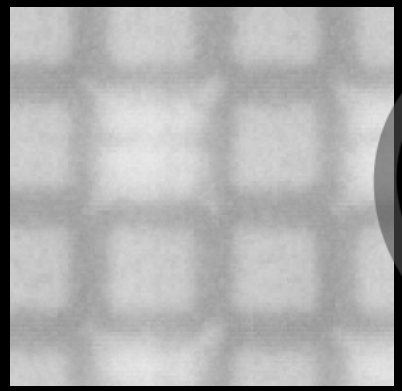
Maybe is RGGB?

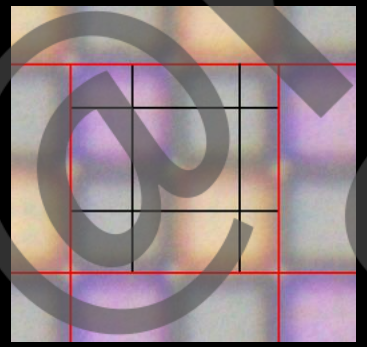
SMARTSENS SC580XS



Scrape off part of the OCL with a knife

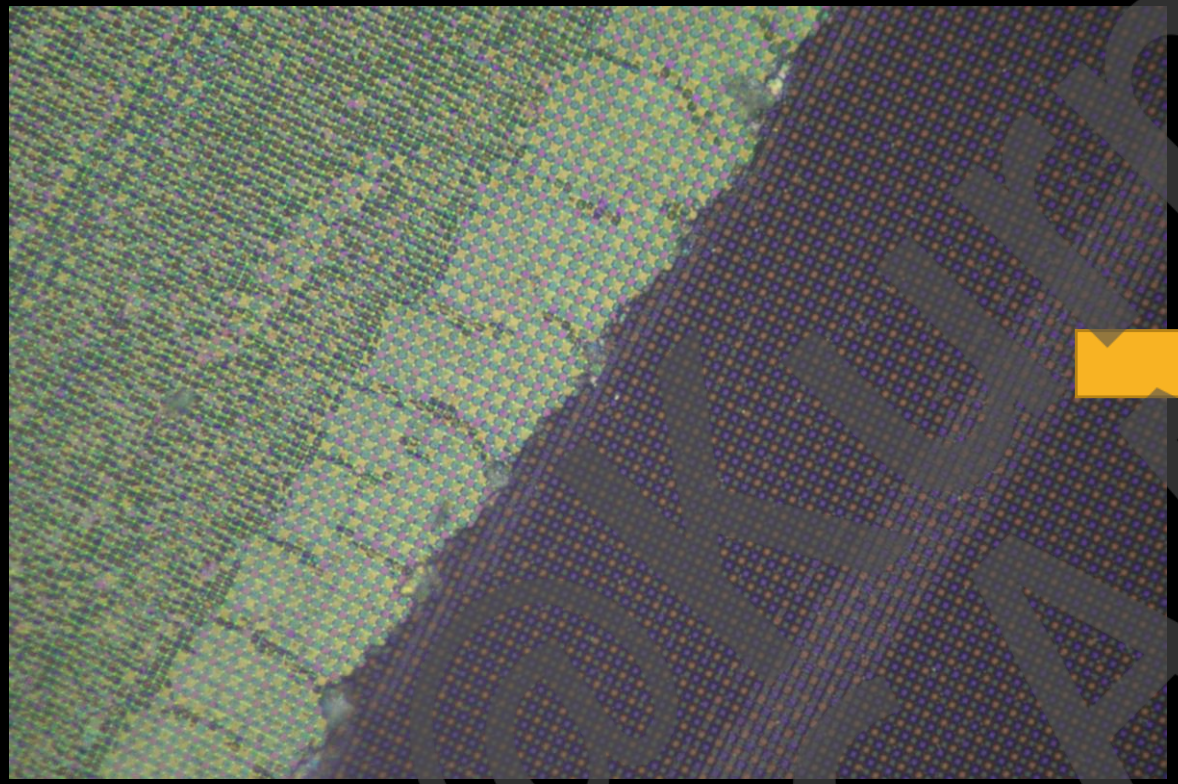




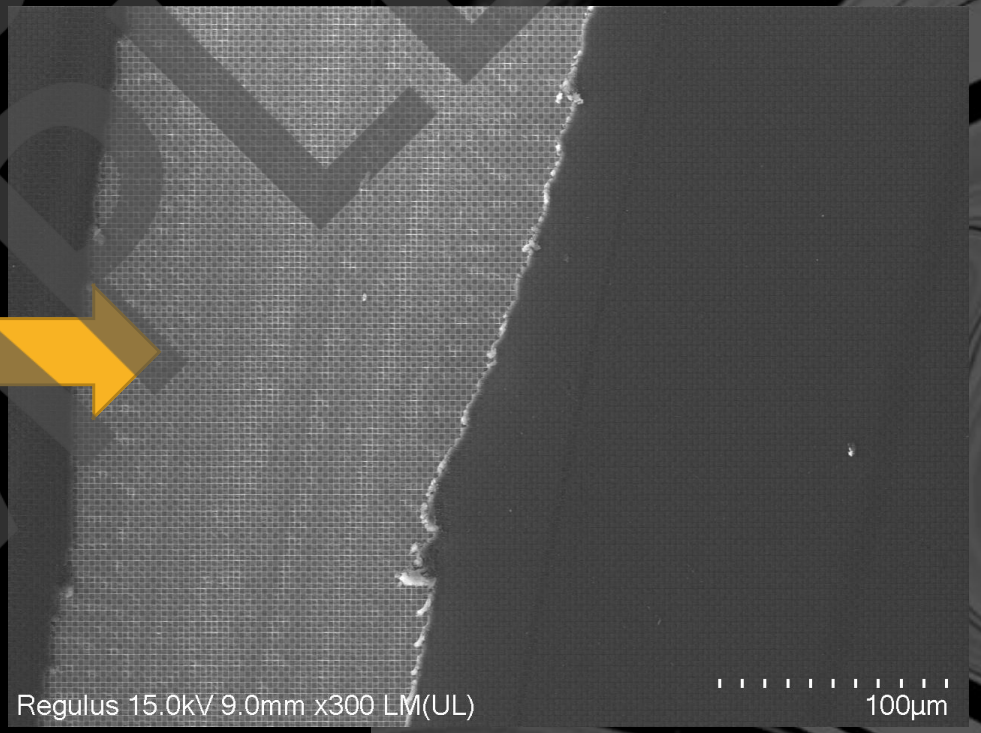


Cut line?

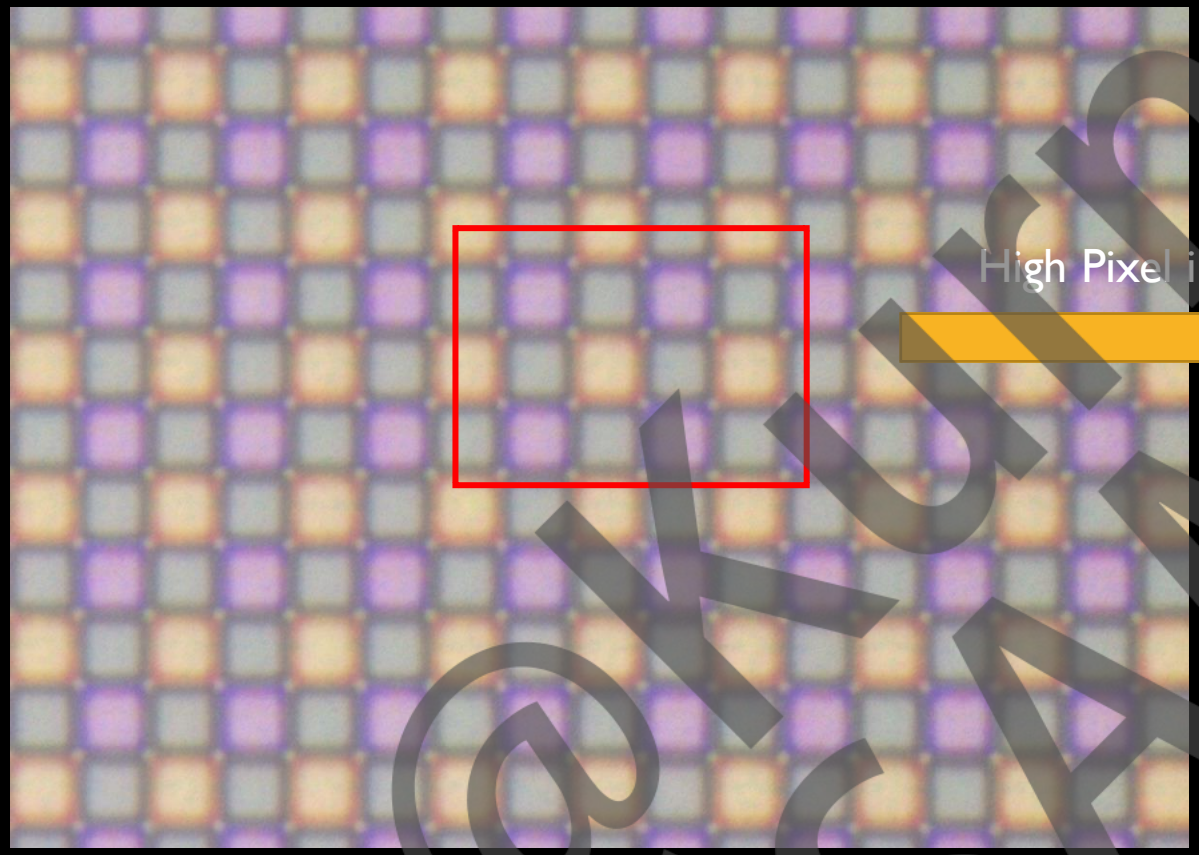
SMARTSENS SC580XS



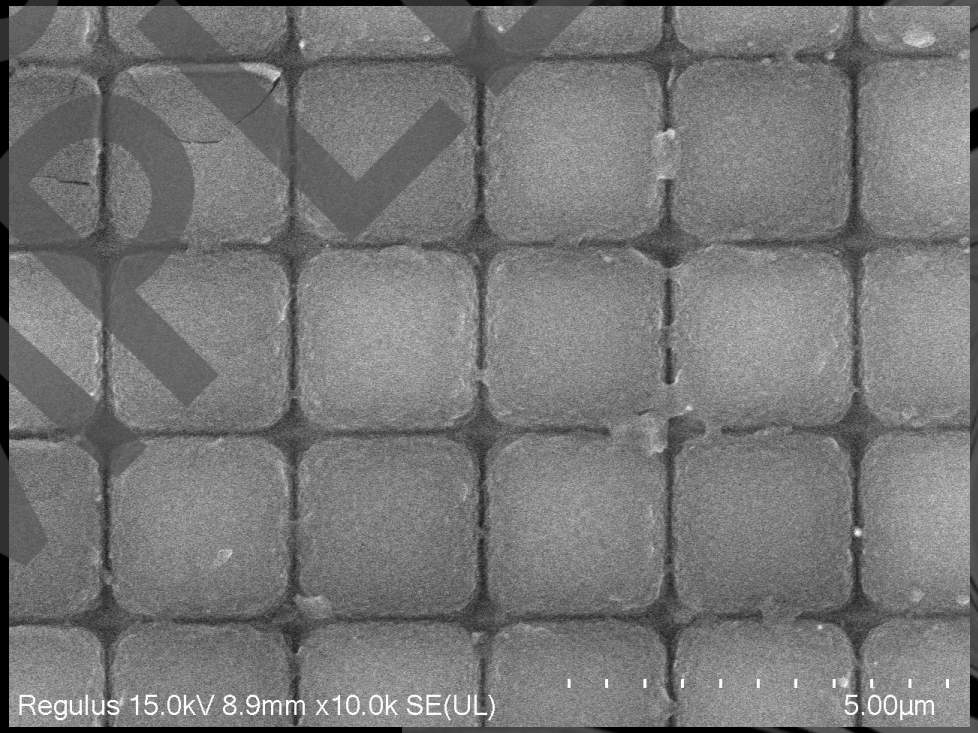
Use SEM



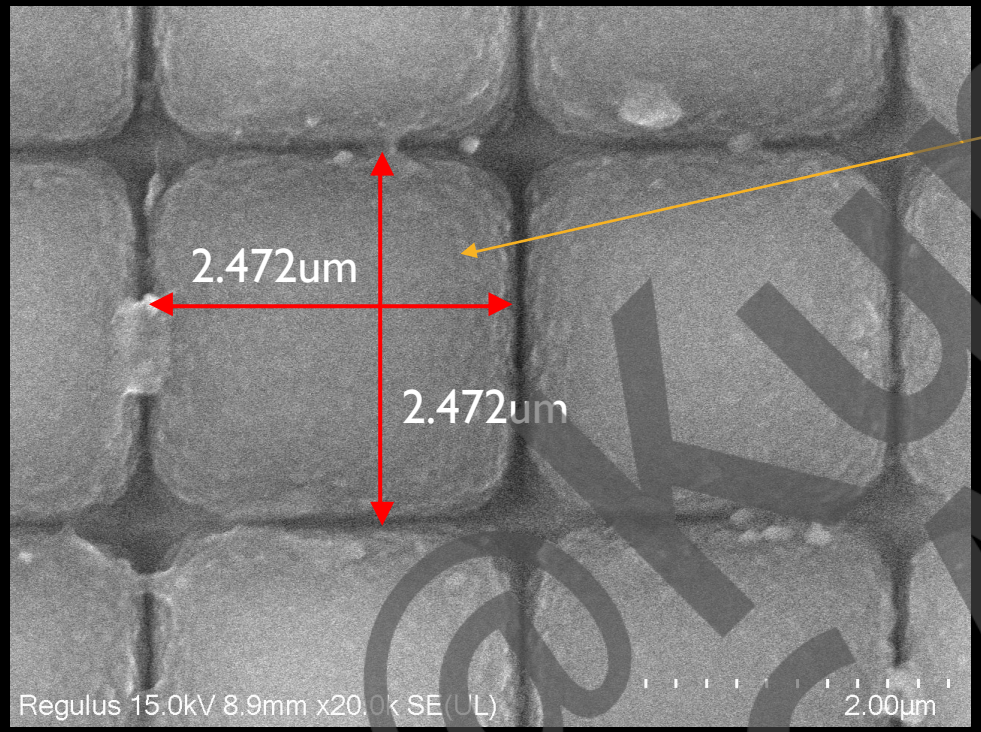
SMARTSENS SC580XS



High Pixel in SEM

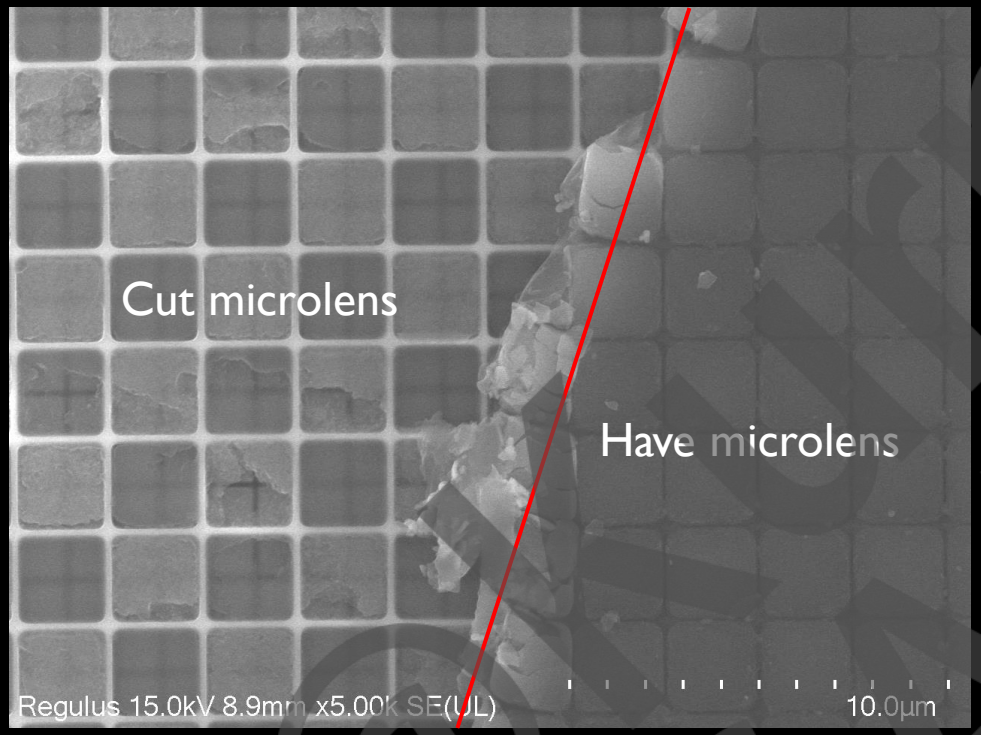


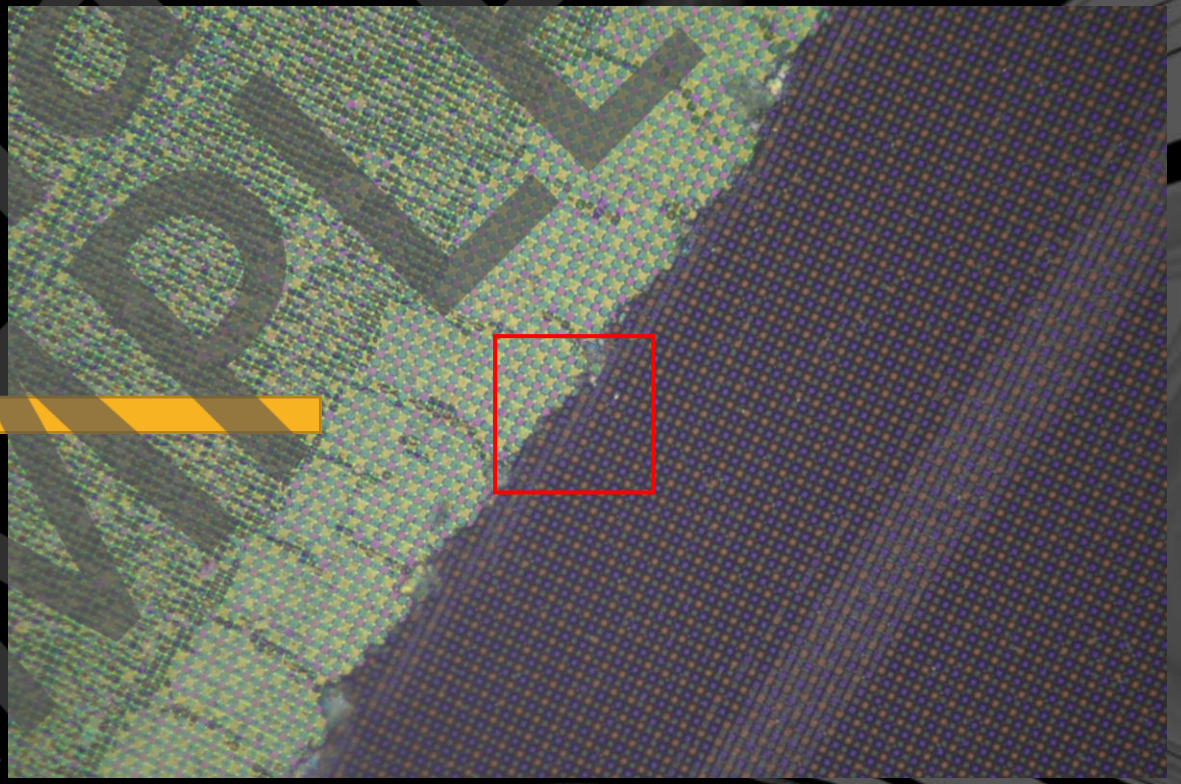
SMARTSENS SC580XS



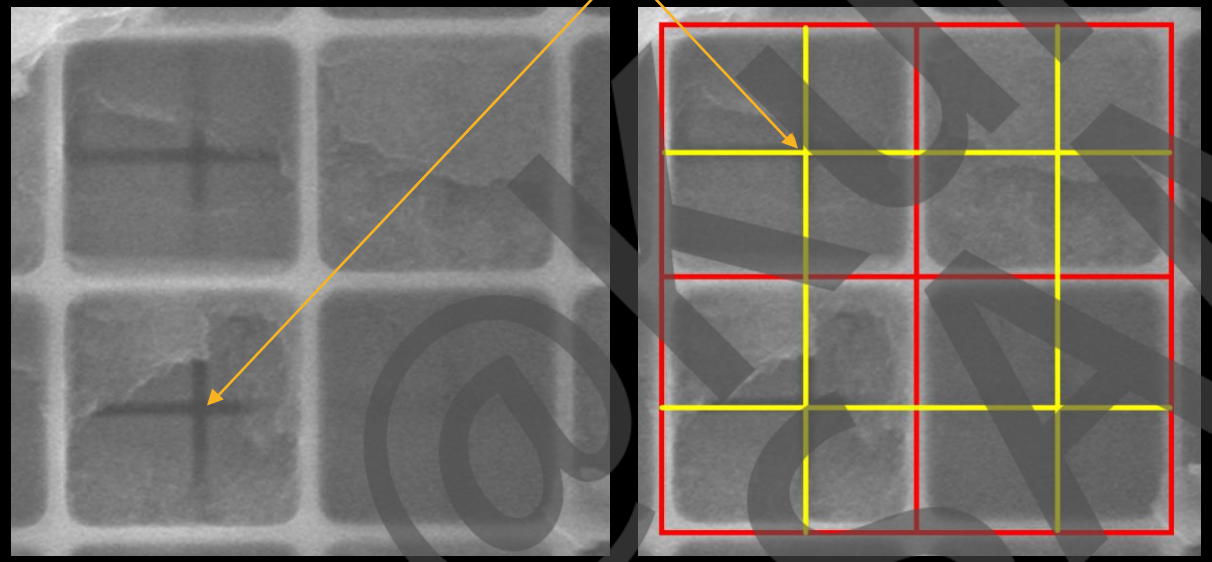
Pixel side length : 2.472um

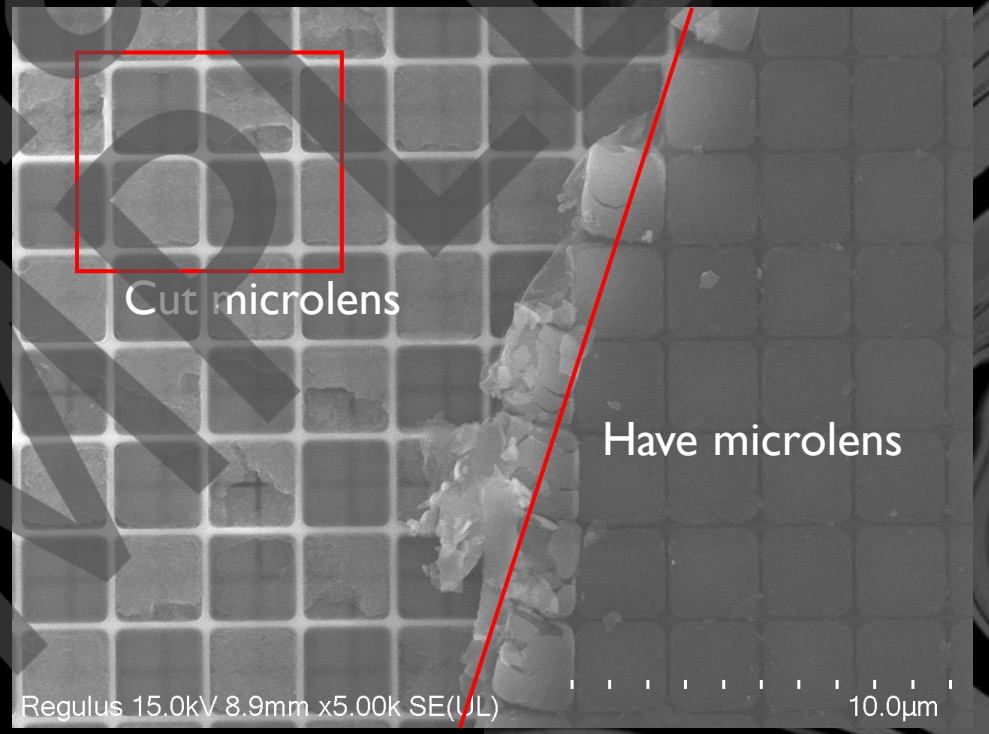
SMARTSENS SC580XS



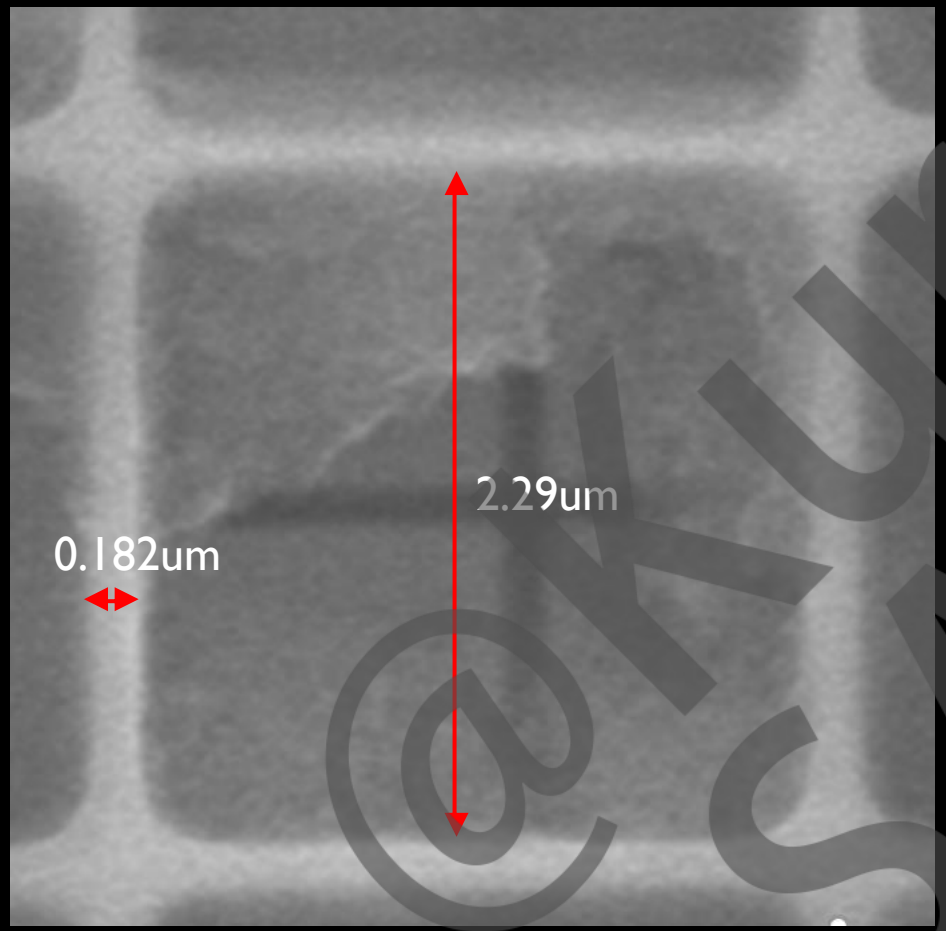


SMARTSENS SC580XS





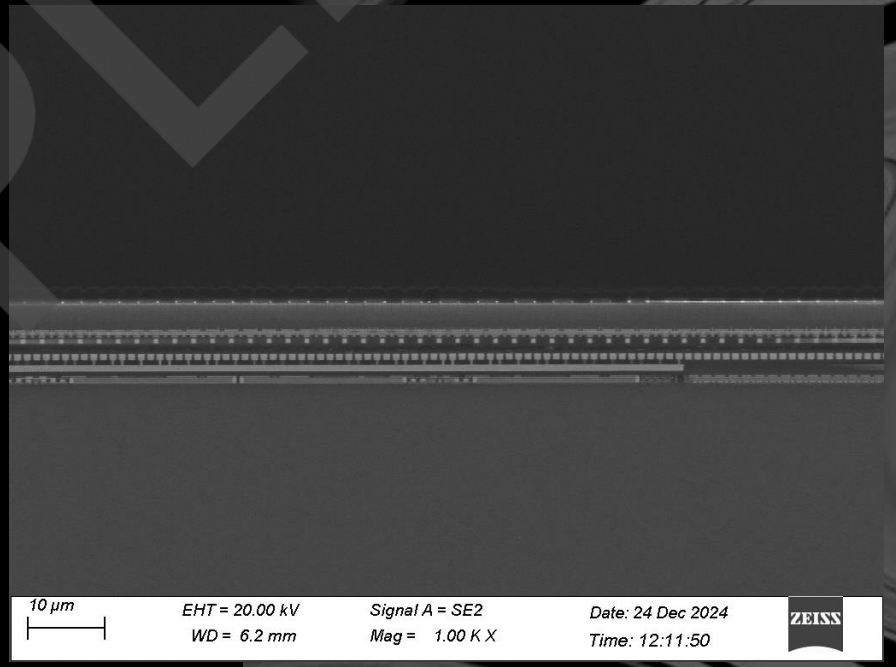
SMARTSENS SC580XS



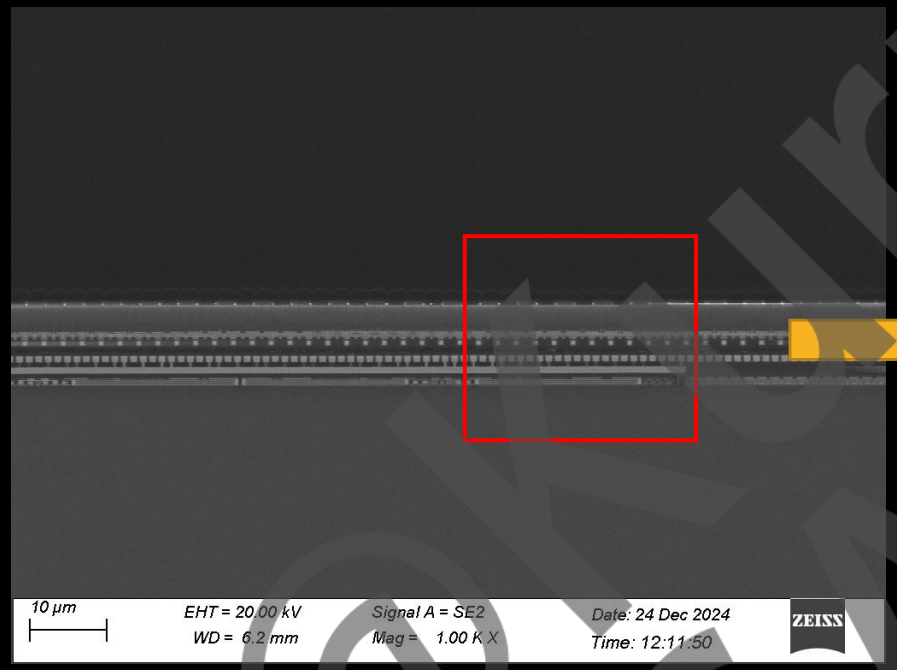
Trap size: 2.29um
Trap well size: 0.182um

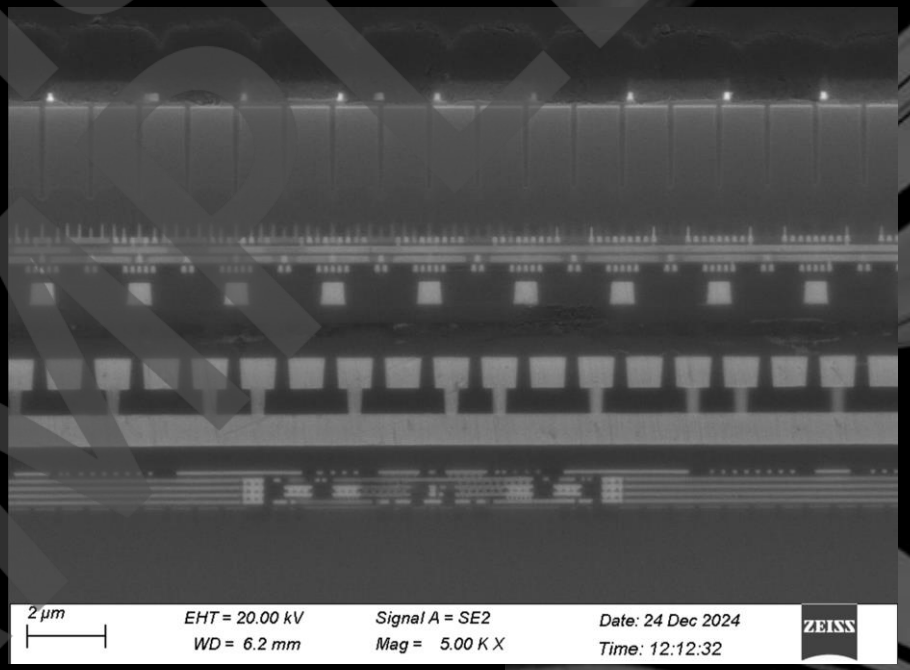
SMARTSENS SC580XS

Package in X Cut



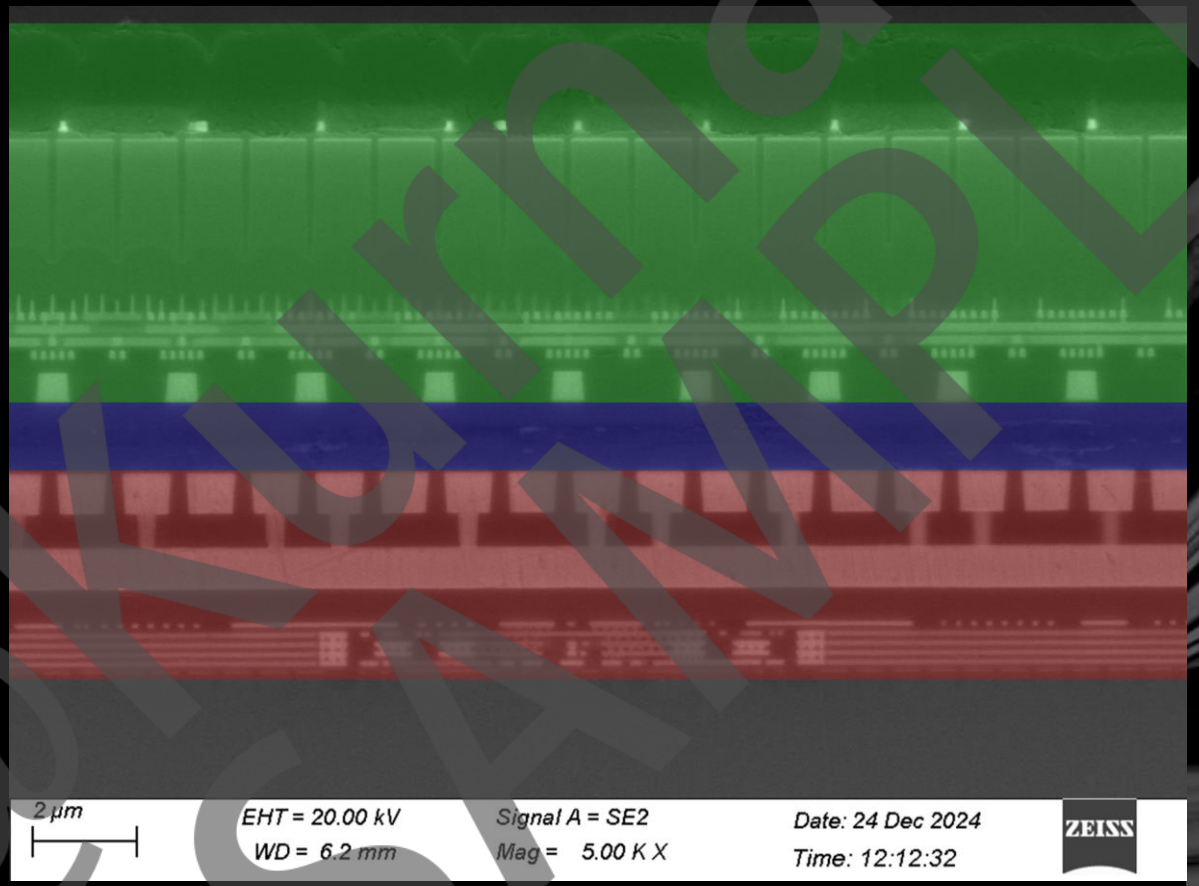
SMARTSENS SC580XS





SMARTSENS SC580XS

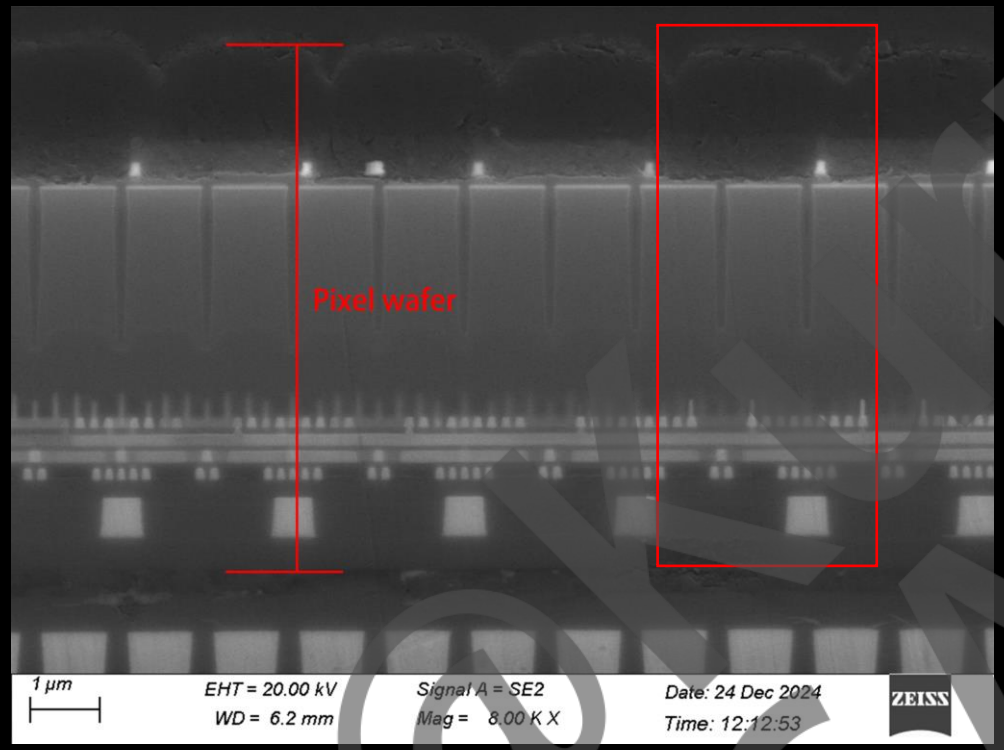
Total Height: 12.744um
Pixel wafer Height: 7.831um
Logic wafer Height: 4.913um



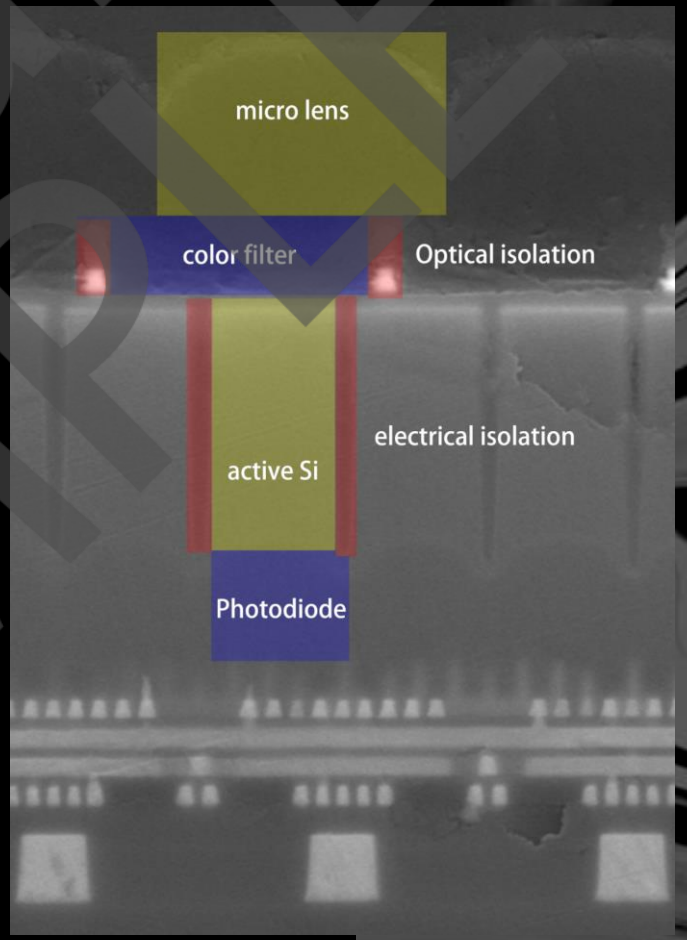
Pixel Wafer

Logic Wafer

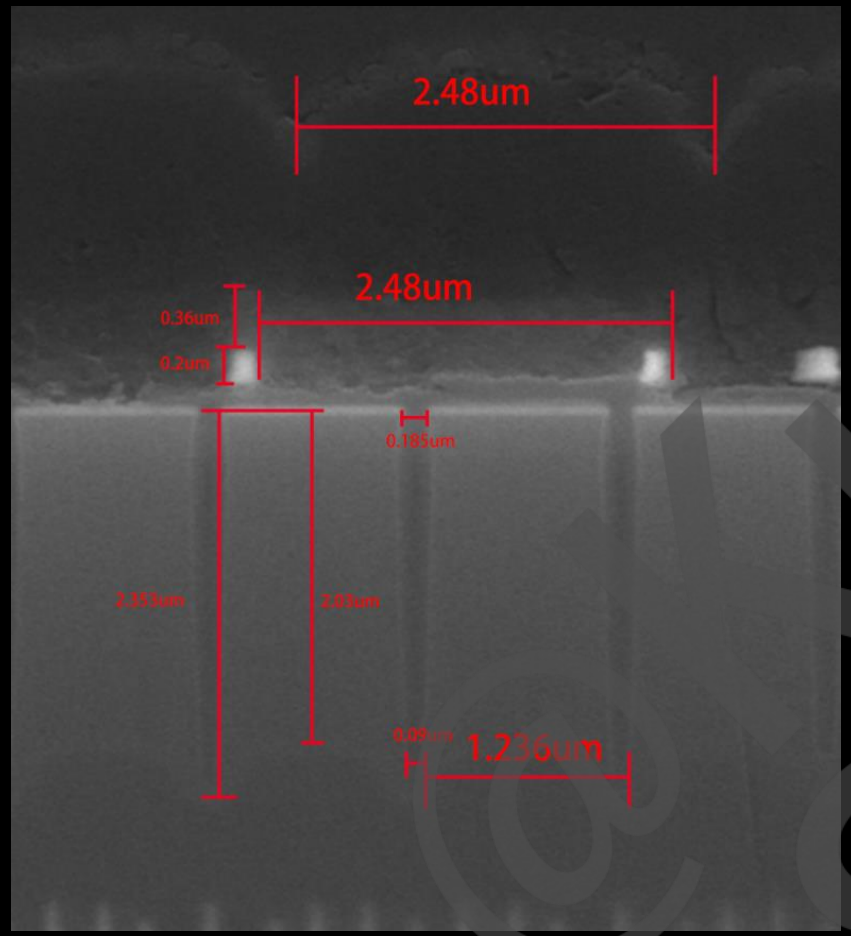
SMARTSENS SC580XS

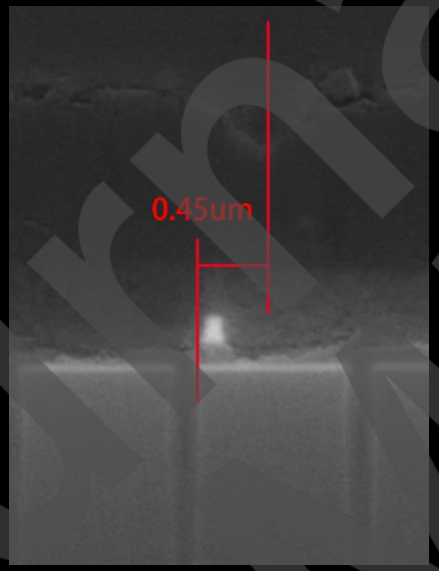


Pixel Wafer



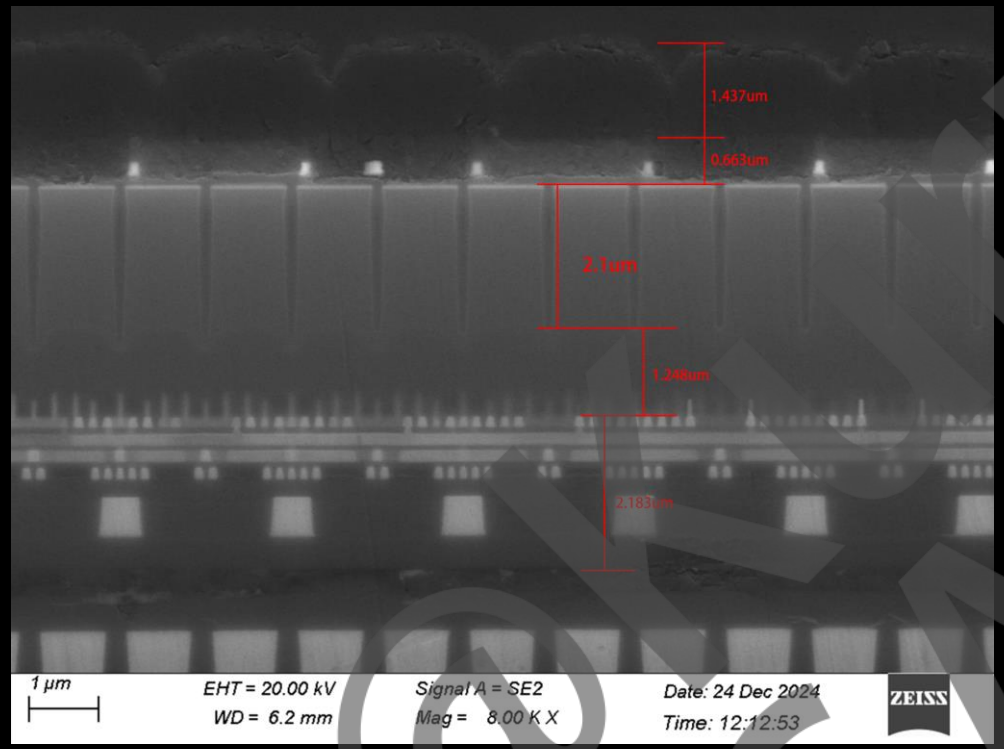
SMARTSENS SC580XS





Micro Lens size:	2.48um
Color Filter size:	2.48um
Photodiode size:	1.236um
Optical isolation deep:	0.36um+0.2um
Electrical isolation deep:	2.353um/2.03um
Electrical isolation top width:	0.185um
Electrical isolation down width:	0.09um
Micro lens- Color filter pitch:	0.45um
Optical - electrical pitch:	0?

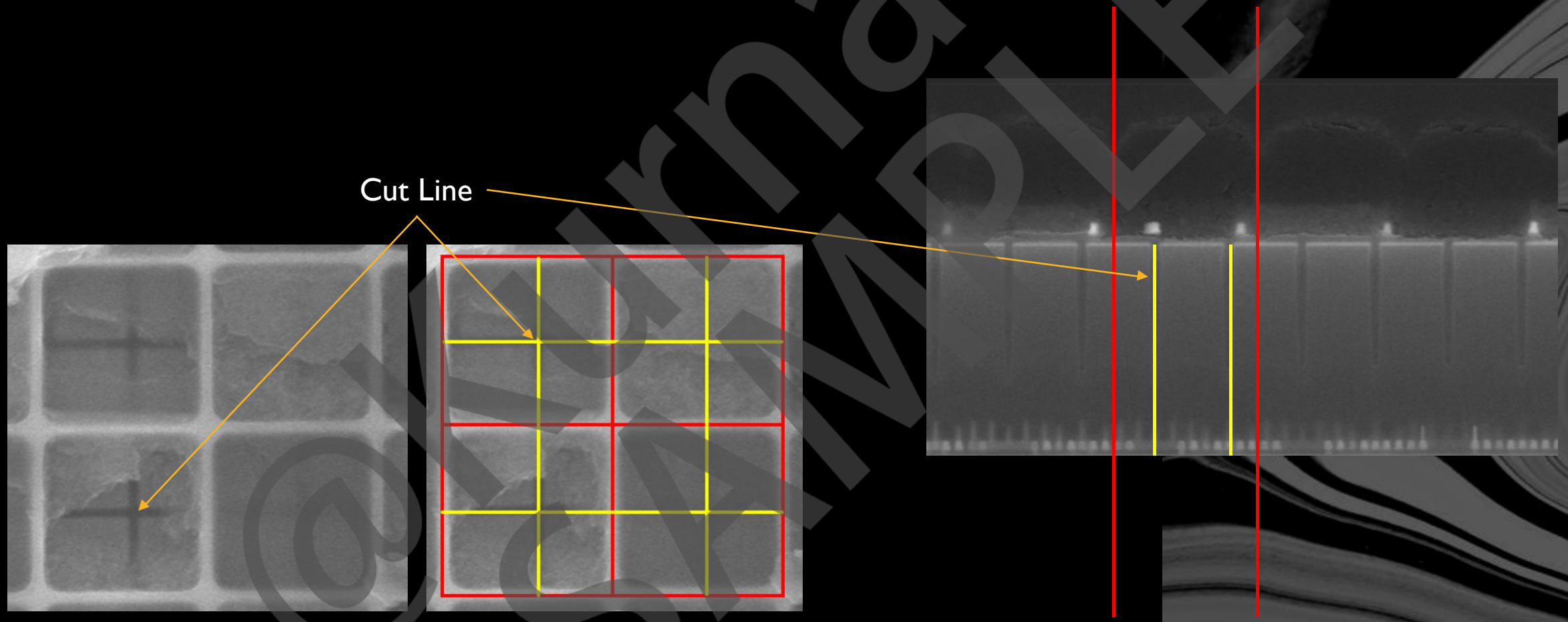
SMARTSENS SC580XS



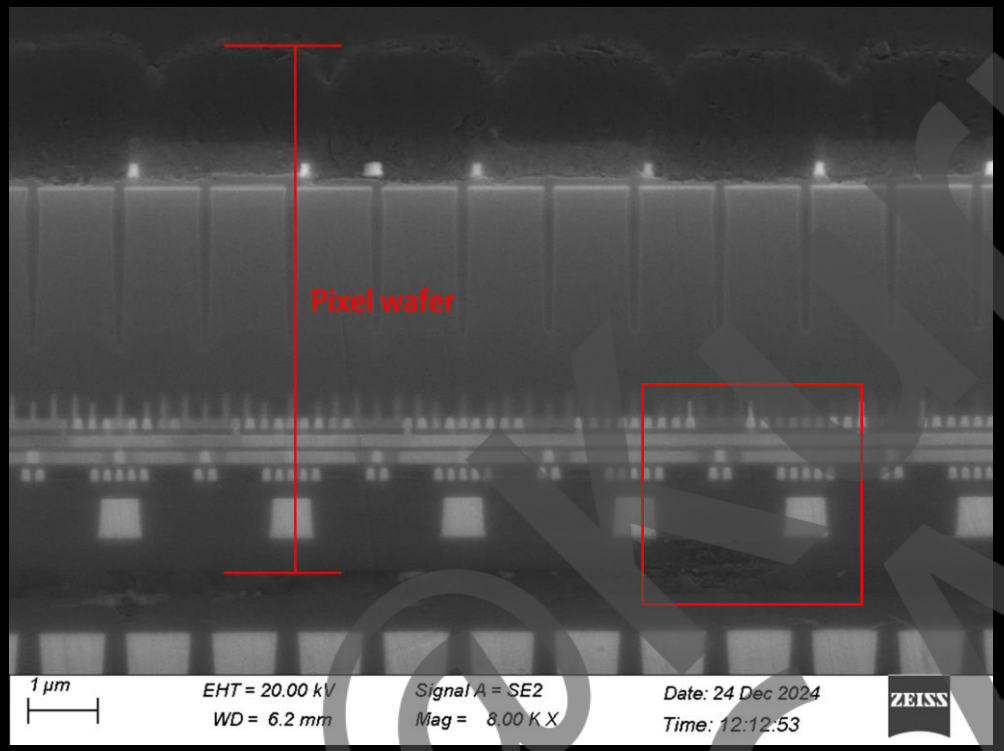
Pixel Wafer

Micro lens Height: 1.437um
Color filter Height: 0.663um
Electrical isolation Depth: 2.1um
Photodiode top to M1 distance: 1.248um
Metal 1 to bond distance: 2.183um

SMARTSENS SC580XS

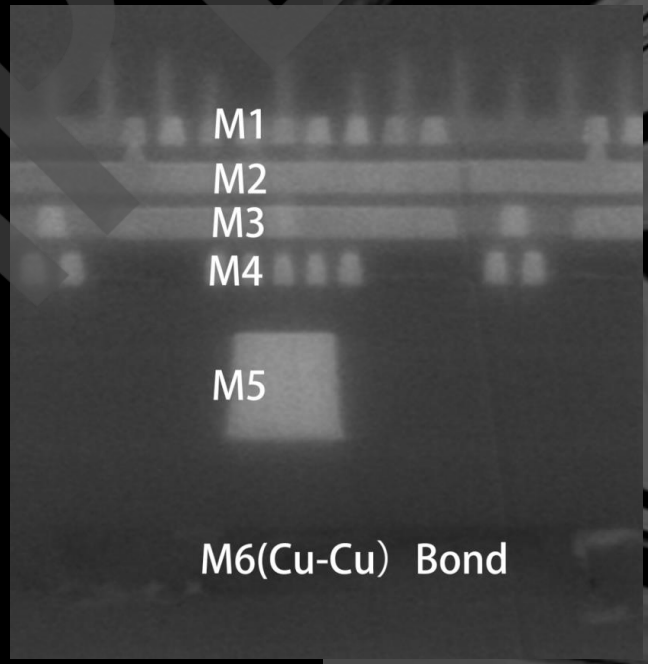


SMARTSENS SC580XS

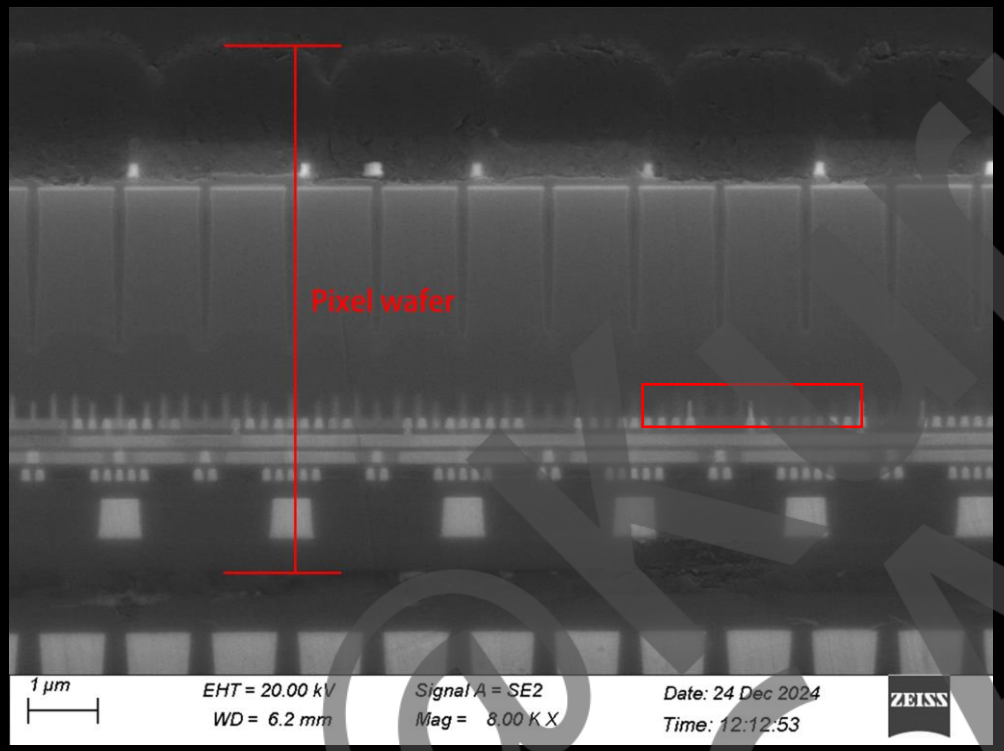


Pixel Wafer

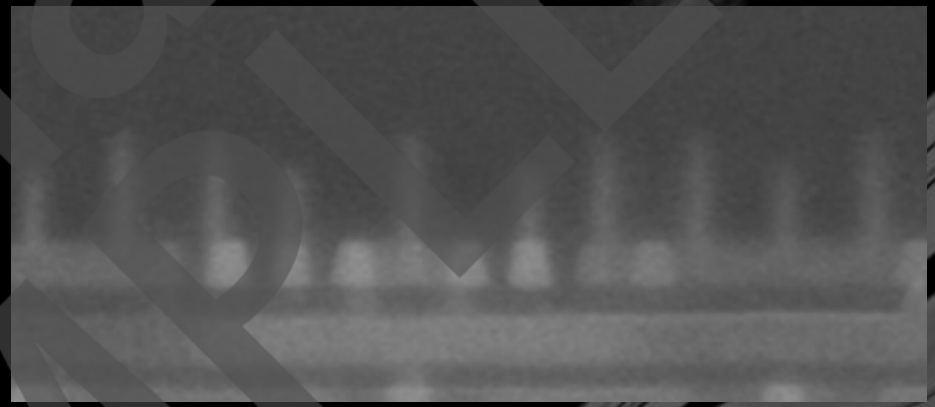
Metal Layers in Pixel Wafer: 6 layers



SMARTSENS SC580XS

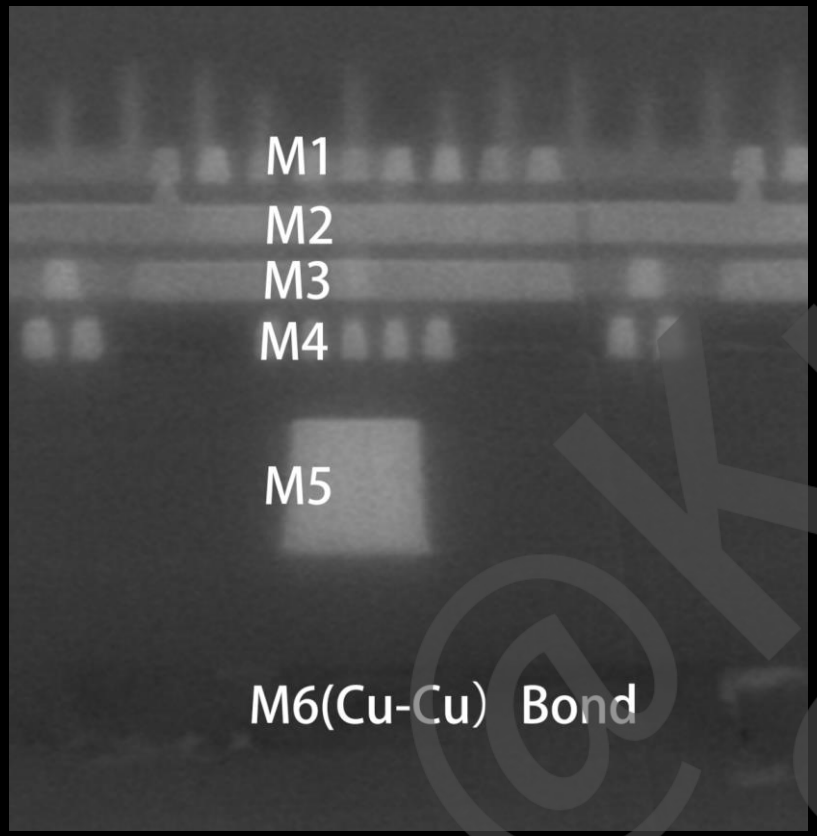


Pixel Wafer



Like VTG?

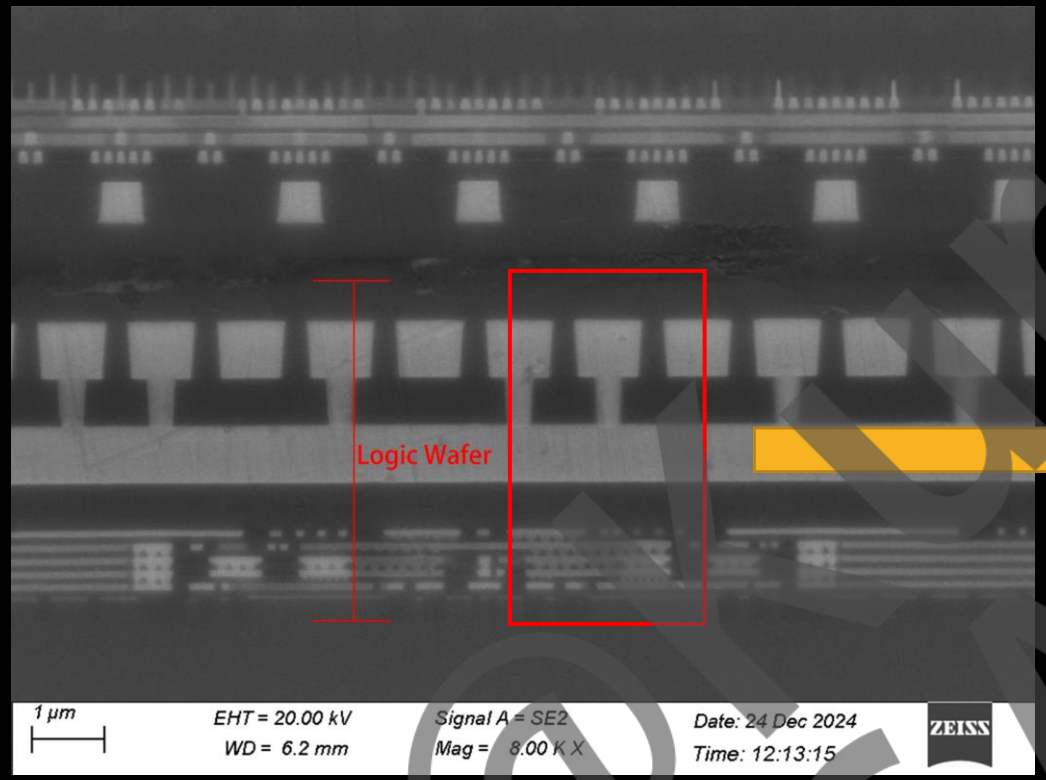
SMARTSENS SC580XS



	(Just)Thickness	Pitch
M1	165nm	198nm
M2	165nm	x
M3	165nm	x
M4	165nm	175nm
M5	561nm	2465nm
M6 （）	351nm	x

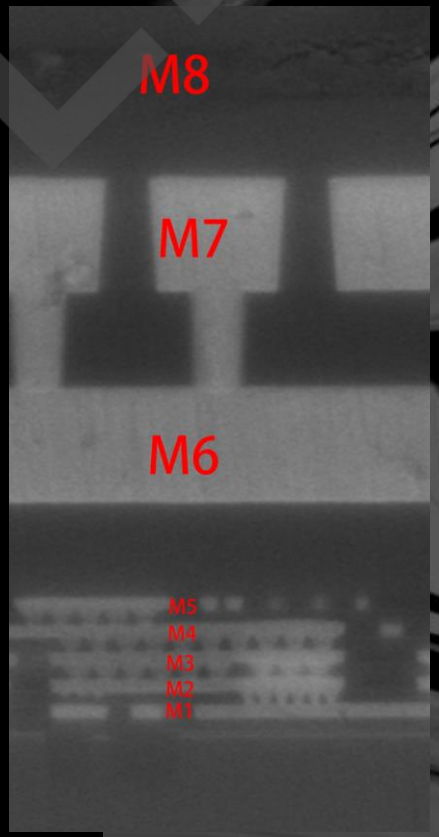
SC580XS Metal data

SMARTSENS SC580XS

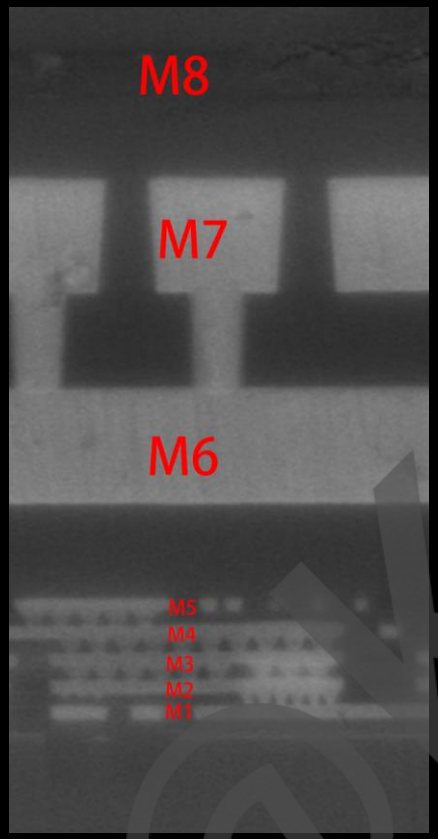


SC580XS Logic Wafer

Logic Wafer have 8 Metal Layers



SMARTSENS SC580XS



SC580XS Logic Wafer

	(Just)Thickness	Pitch
M1	82nm	x
M2	82nm	x
M3	82nm	x
M4	82nm	x
M5	82nm	x
M6	800nm	x
M7	800nm	1240nm
M8 ( )	351nm	x

IDENTIFICATION

IDENTIFICATION

Why I think Mate70pro+ use the Smartsens Sc580xs?

- CIS Package
  - Diesize/Pixel area size
  - Chip Pad
- In Front
  - Pixel size
- In Profile
  - Pixel Wafer
  - Logic Wafer

IDENTIFICATION（CIS PACKAGE）

Mate70Pro+ CIS

SC580XS

On chip pad
these two chip are same number

Different just the pad by used

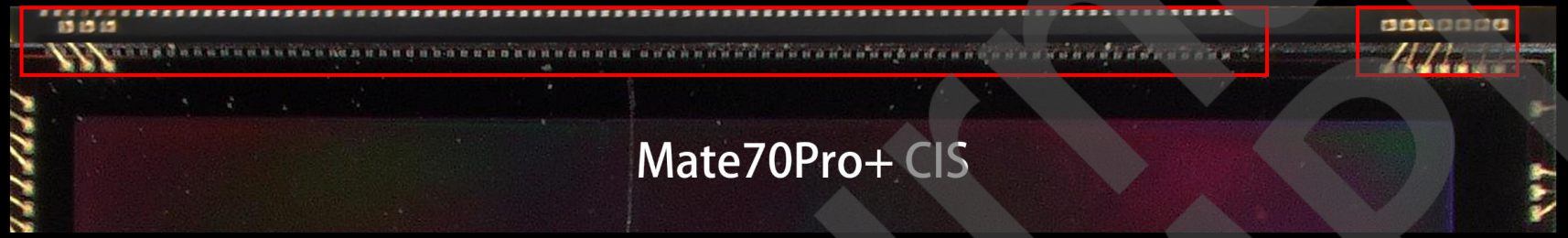
same

Bonding Pad number: 166
Bonding Pad in use: 117

Bonding Pad number: 166
Bonding Pad in use: 166

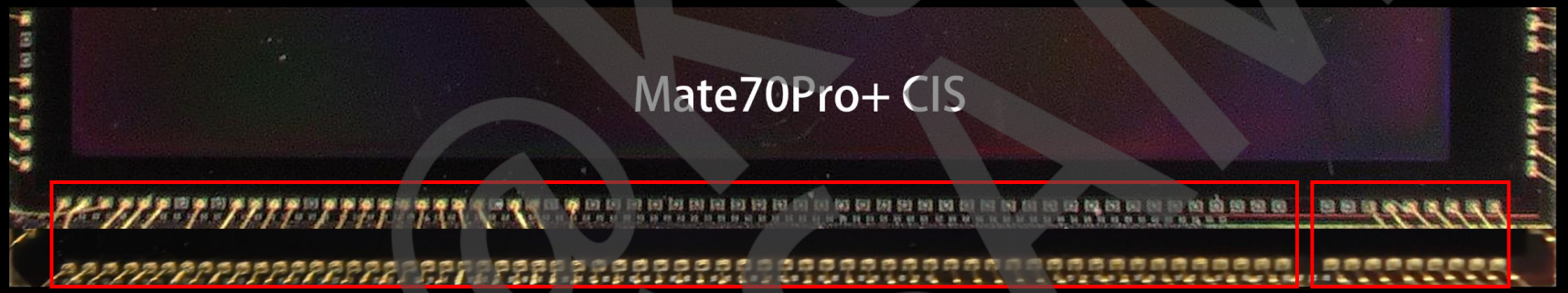
IDENTIFICATION （CIS PACKAGE）

SC580XS



Up pad area

Pad number and pad Location
All same

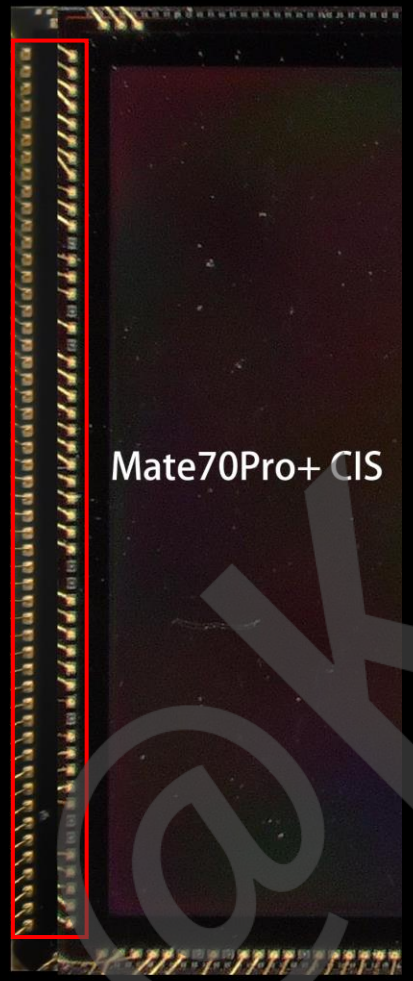


Down pad area

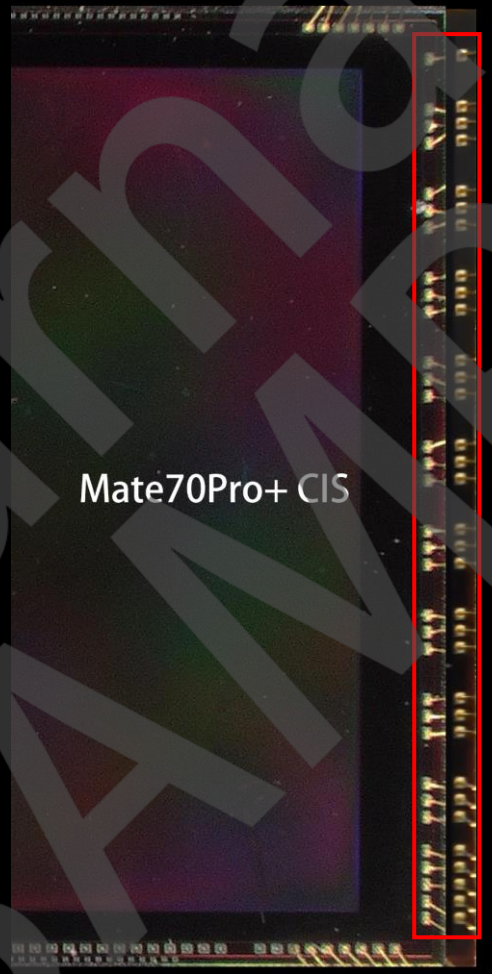
SC580XS

IDENTIFICATION （CIS PACKAGE）

SC580XS



Left Pad area



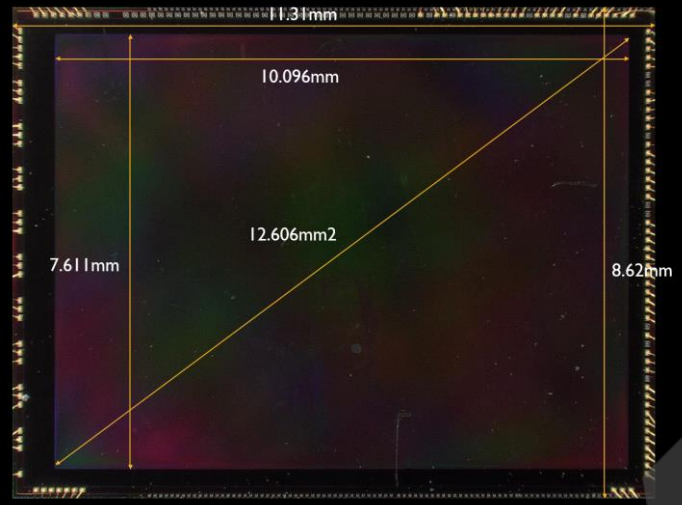
SC580XS

Right Pad area

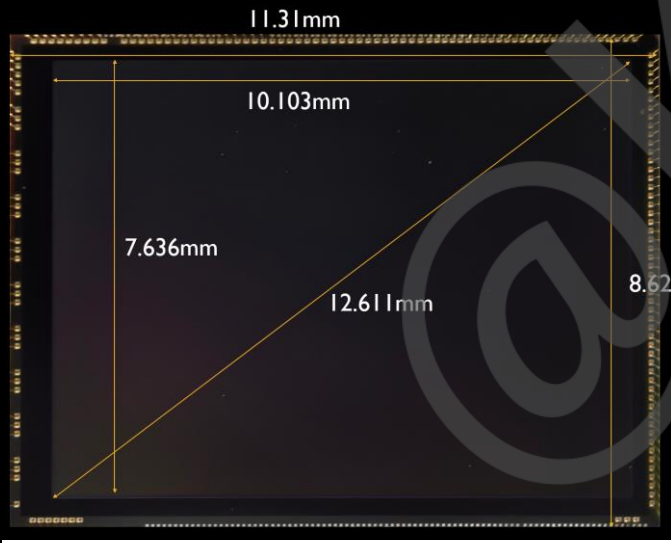
Pad number and pad Location

All same

IDENTIFICATION（CIS PACKAGE）



Mate70 Pro+ Cmos



SC580XS

	SC580XS	M70P+ cmos	
Pad number	166/166	166/117	same
Full diesize	11.31x8.62 97.49mm2	11.31x8.62 97.49mm2	same
Pixel area	10.103x7.63 6 77.15mm2	10.096x7.611 76.84mm2	same
Diagonal line size:	12.611mm (1/1.27)	12.606mm (1/1.27)	same

For package
I think these two cmos have the same package/die

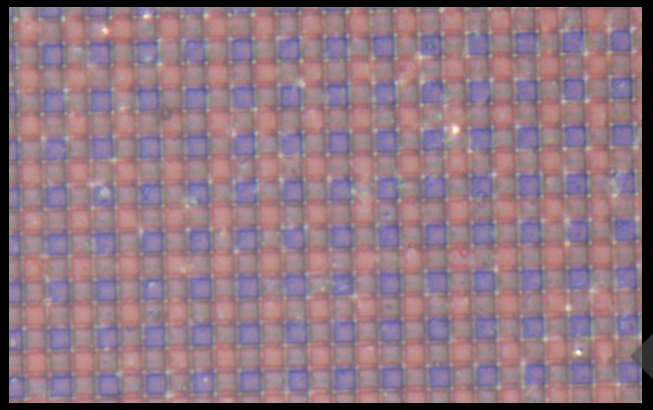
IDENTIFICATION

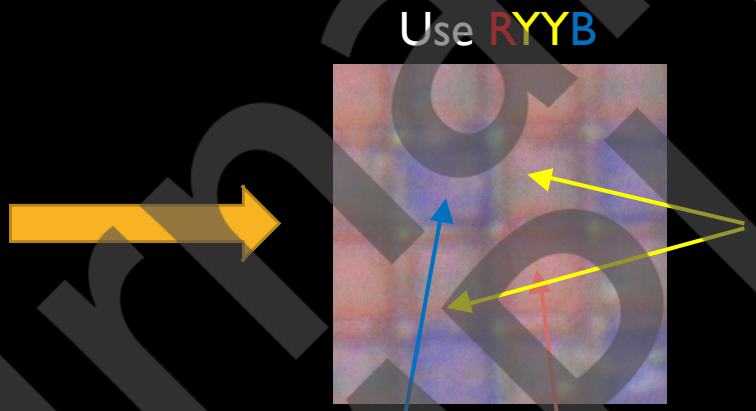
Why I think Mate70pro+ use the Smartsens Sc580xs?

- CIS Package
  - Diesize/Pixel area size
  - Chip Pad
- In Front
  - Pixel size
- In Profile
  - Pixel Wafer
  - Logic Wafer

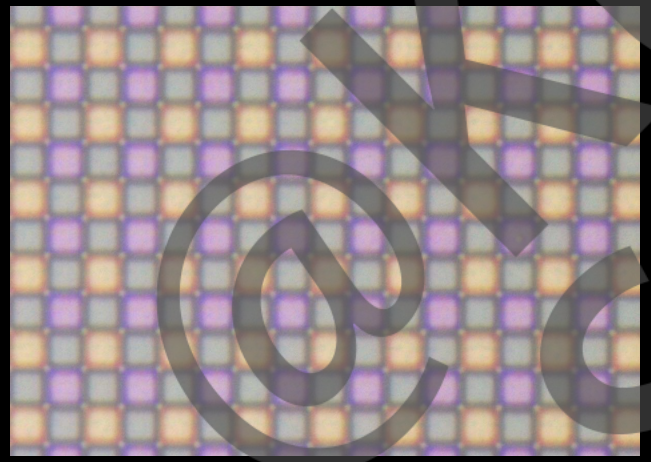
IDENTIFICATION(IN FRONT)

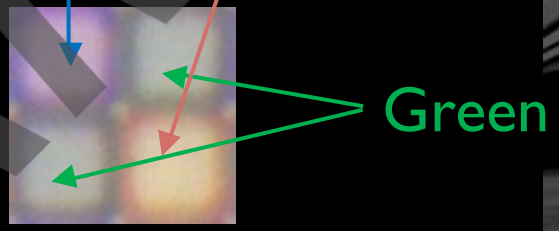
Mate70Pro+





SC580XS

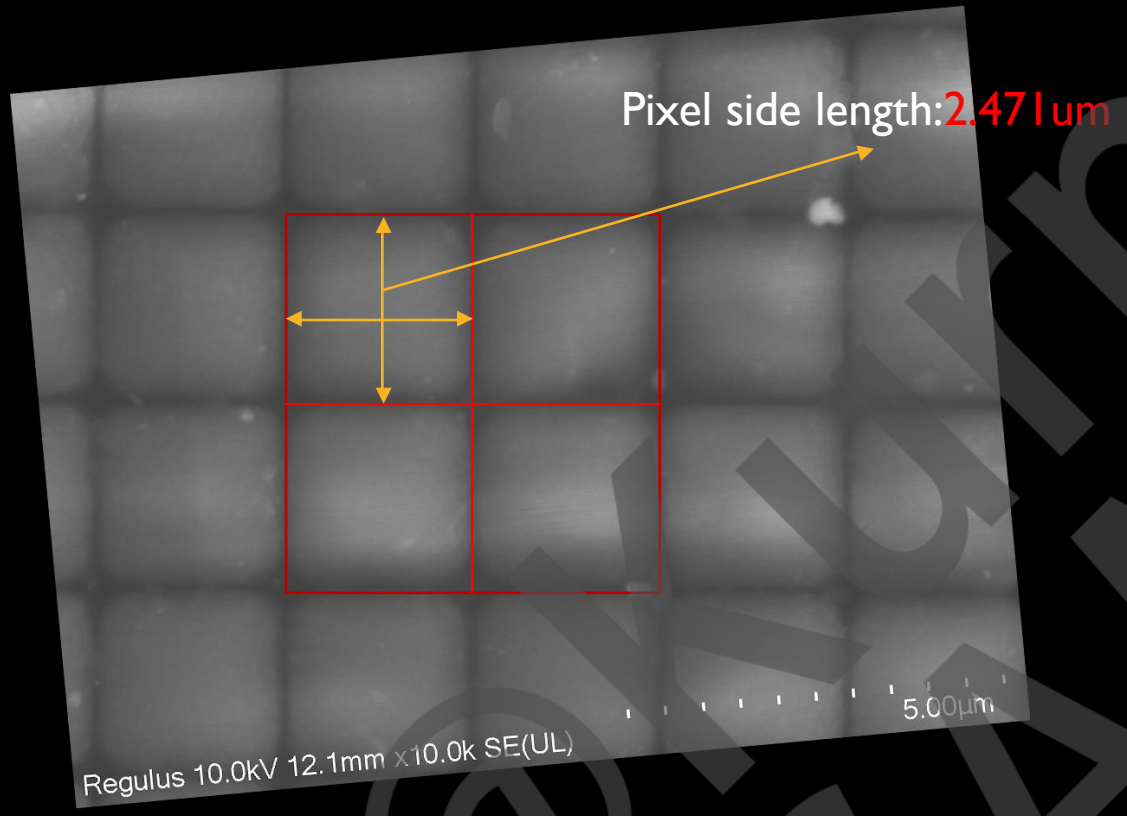




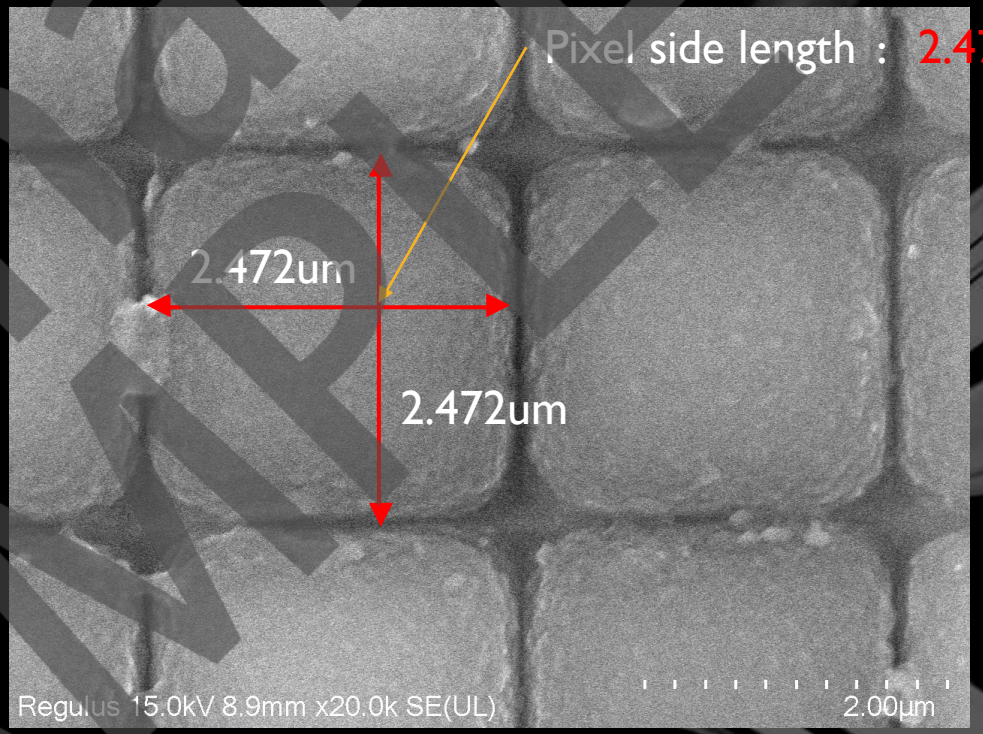
Maybe is RGGB?

In color filter
These are different
Mate70Pro+ use RYYB
SC580XS use RGGB

IDENTIFICATION(IN FRONT SEM)



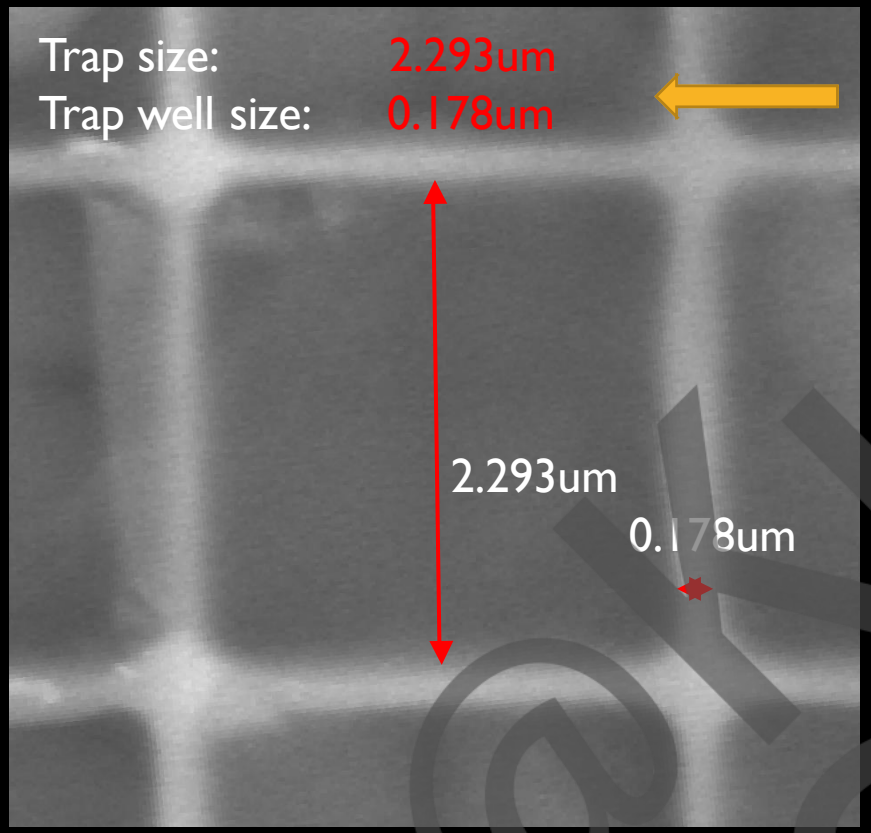
Mate70pro+ CIS



Smartsens Sc580xs

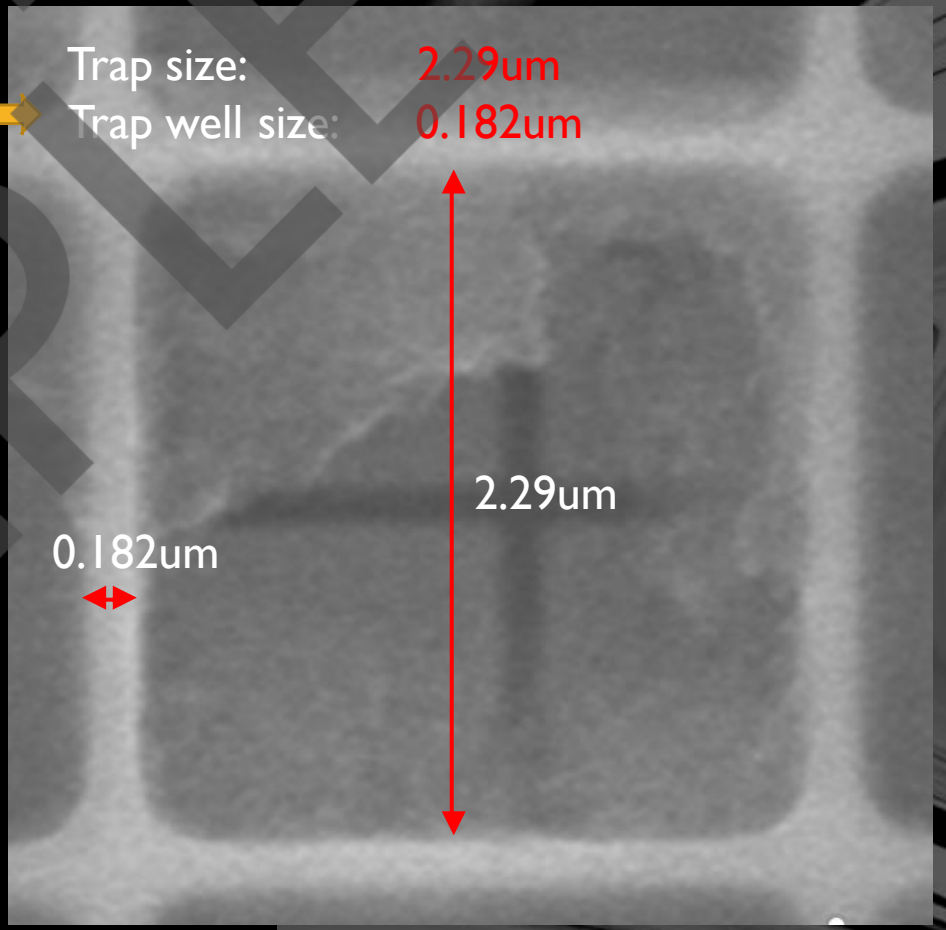
Pixel Size is the same as 2.47um

IDENTIFICATION(IN FRONT SEM)



Mate70Pro+ CIS

The Trap and Trap well size
Are the same on both sides



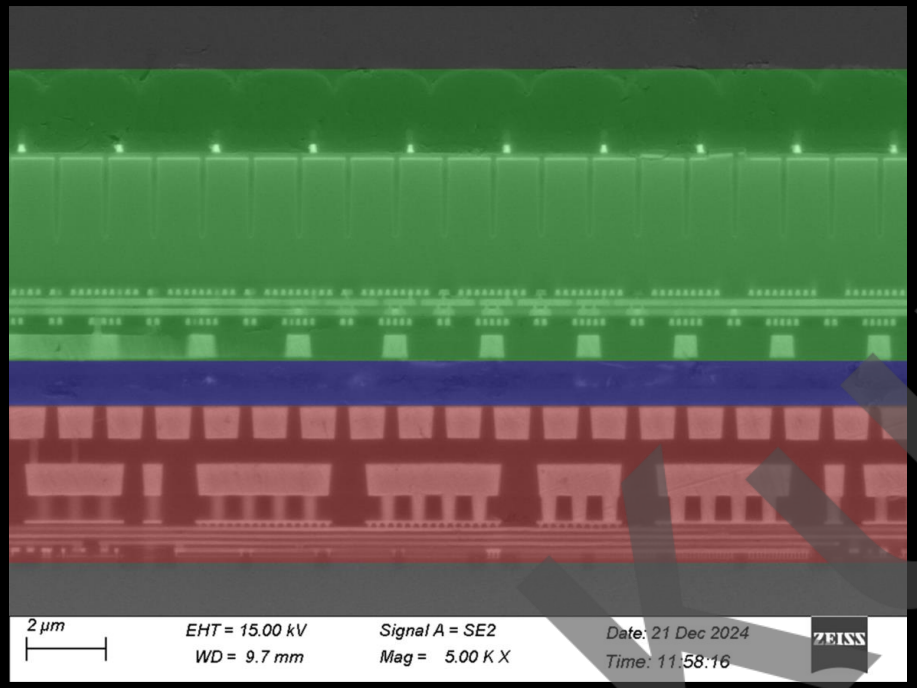
Smartsens Sc580xs CIS

IDENTIFICATION

Why I think Mate70pro+ use the Smartsens Sc580xs?

- CIS Package
  - Diesize/Pixel area size
  - Chip Pad
- In Front
  - Pixel size
- In Profile
  - Pixel Wafer
  - Logic Wafer

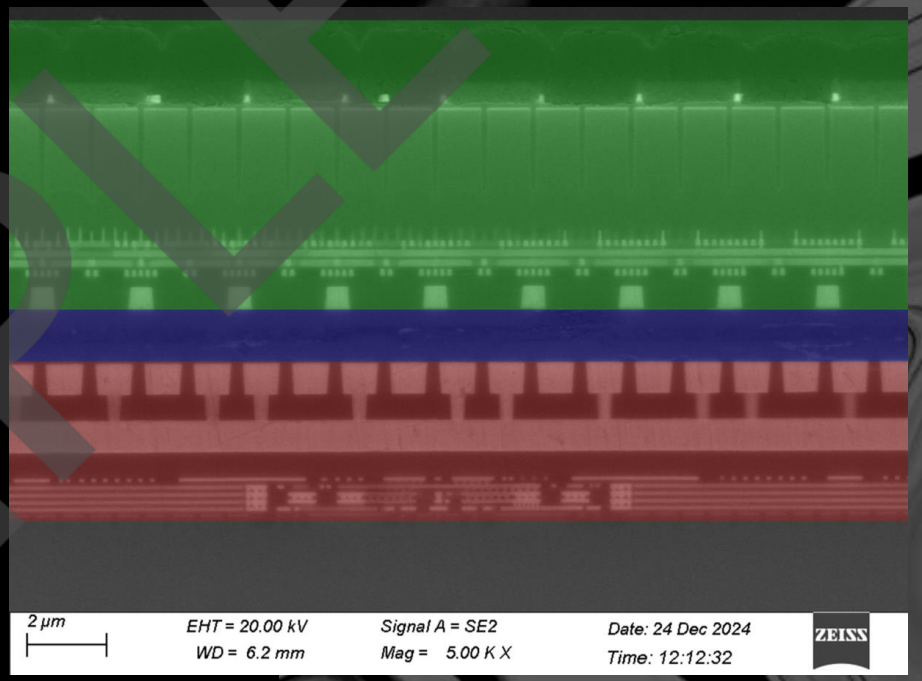
IDENTIFICATION （IN PROFILE）



Mate70Pro+ CIS

Pixel Wafer

Logic Wafer

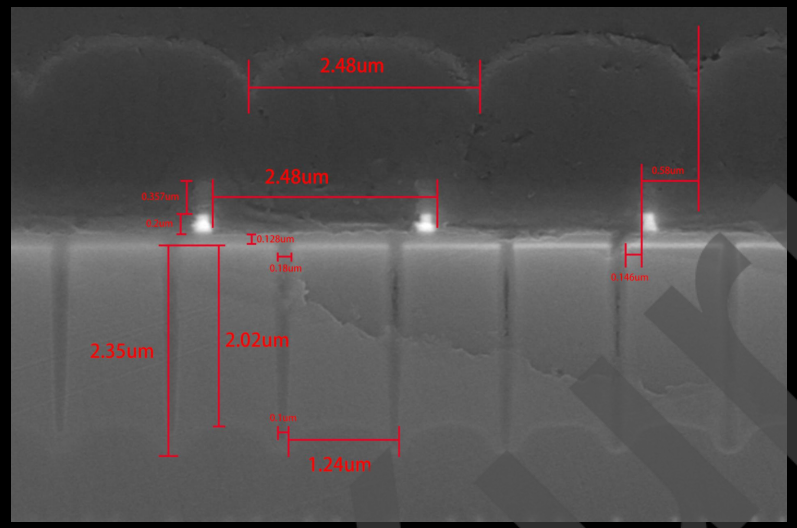


Smartsens Sc580xs CIS

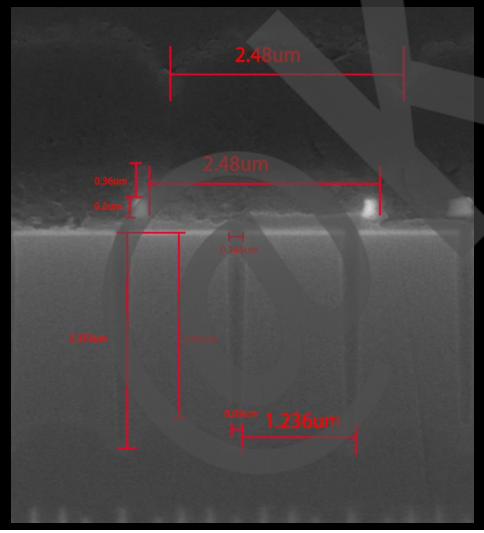
	M70P+	SC580XS	
Total height	12.741um	12.744um	Same
Pixel wafer height	7.853um	7.831um	Same
Logic wafer height	4.905um	4.913um	Same

IDENTIFICATION （IN PROFILE） （PIXEL WAFER）

Mate70P+



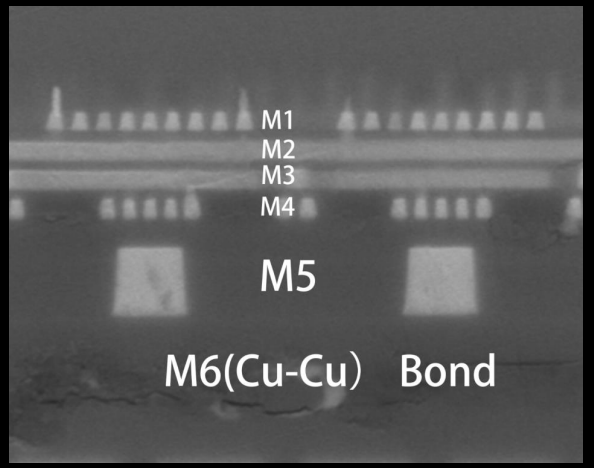
SC580XS

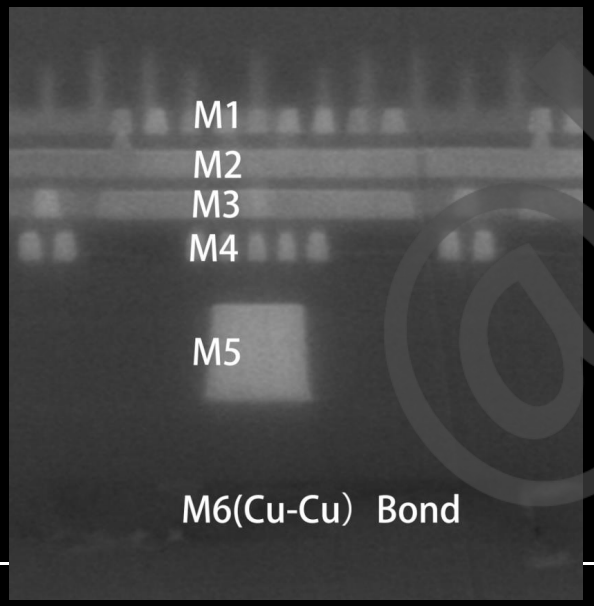


	M70P+	SC580XS	
Micro Lens size	2.48um	2.48um	Same
Color Filter size	2.48um	2.48um	Same
Photodiode size	1.24um	1.236um	Same
Optical isolation deep	0.357+0.2	0.36+0.2	Same
Electrical isolation deep	2.35/2.02	2.353/2.03	Same

For the Pixel wafer-Pixel layers
These are the same things in the data

IDENTIFICATION（IN PROFILE）（PIXEL METAL LAYERS）





Mate70pro+ CIS
Pixel Metal layers

Both
6 Metal Layers

SC580XS
Pixel Metal layers

	(Just)Thickness		Pitch	
	M70P+	SC580XS	M70P+	SC580XS
M1	162nm	165nm	198.6nm	198nm
M2	162nm	165nm	x	x
M3	162nm	165nm	x	x
M4	162nm	165nm	177nm	175nm
M5	561nm	561nm	2470nm	2465nm
M6	351nm	351nm	x	x

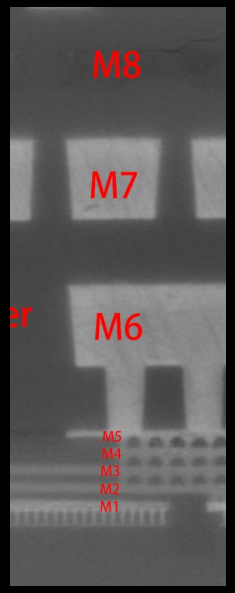
Although there are some mapping errors,
The number/spacing/thickness of metal layers
in both products are the same

IDENTIFICATION

Why I think Mate70pro+ use the Smartsens Sc580xs?

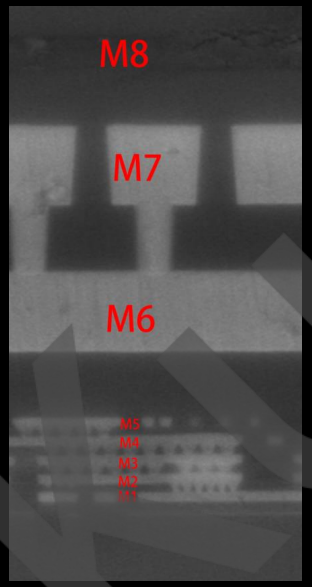
- CIS Package
  - Diesize/Pixel area size
  - Chip Pad
- In Front
  - Pixel size
- In Profile
  - Pixel Wafer
  - Logic Wafer

IDENTIFICATION



Mate70pro+ CIS
Logic Metal layers

Both
8 Metal Layers



SC580XS
Logic Metal layers

	(Just) Thickness		Pitch	
	M70P+	SC580XS	M70P+	SC580XS
M1	83nm	82nm	x	x
M2	83nm	82nm	x	x
M3	83nm	82nm	x	x
M4	83nm	82nm	x	x
M5	83nm	82nm	x	x
M6	802nm	800nm	x	x
M7	793nm	800nm	1236nm	1240nm
M8	348nm	351nm	x	x

Although there are some mapping errors,
The number/spacing/thickness of metal layers
in both products are the same

IDENTIFICATION END

Why I think Mate70pro+ use the Smartsens Sc580xs?

- CIS Package
  - Diesize/Pixel area size
  - Chip Pad
- In Front
  - Pixel size
- In Profile
  - Pixel Wafer
  - Logic Wafer

So that, despite some mapping errors,
I still believe that： the Huawei Mate 70 Pro + uses the same Sc580xs as Smartsens
They only change is the color filter on its surface,
which is customized from RGGB to RYYB

IDENTIFICATION END

	SC580XS data
Package	COB/RW
structure	BSI/WoW()
Pixel area	1/1.27
Pixel size	1.24um/2.48um
Pixel mode	4 in 1
Pixel number	50MP/12.5MP
Pixel wafer Metal layers	6
Logic wafer Metal layers	8

This analyze SC580XS get data

1.5MP RED MAPLE COLOR CIS

@Kurnal

1.5MP RED MAPLE COLOR CIS

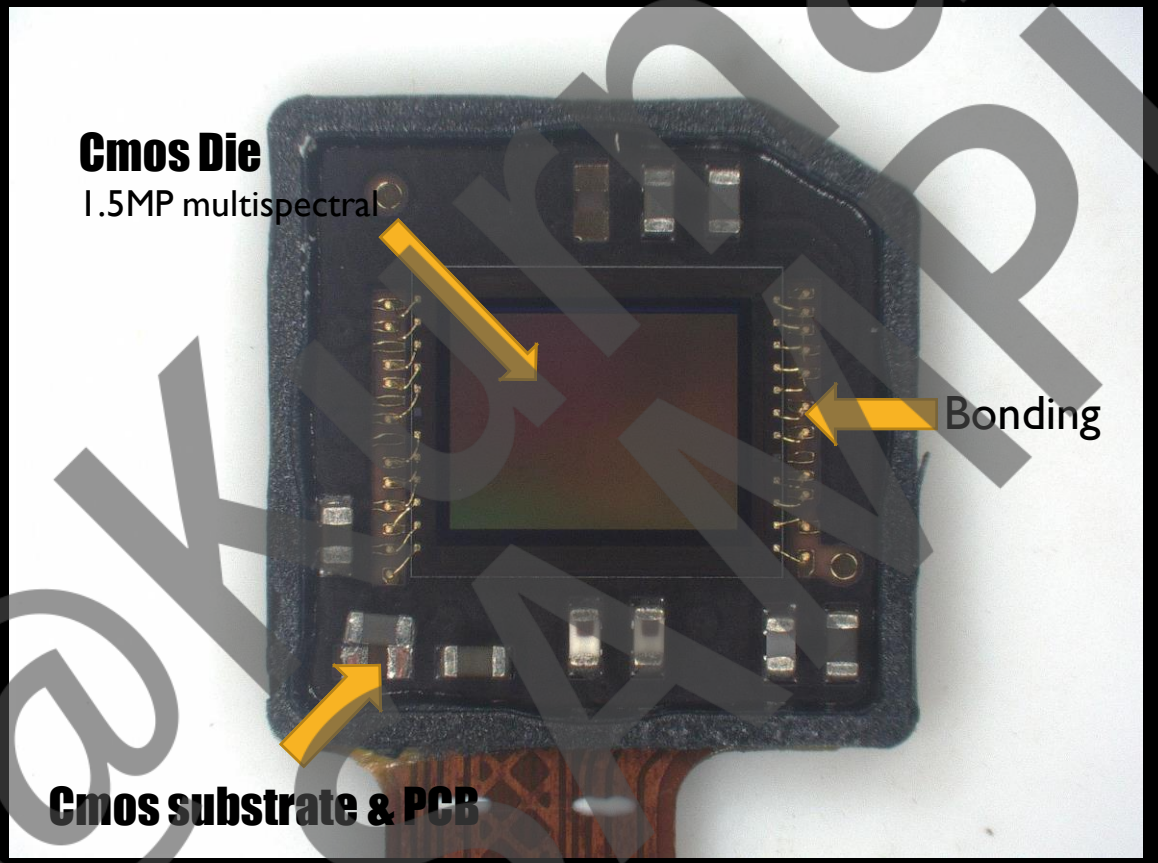
1.5MP red maple color cis

红枫原色影像
还原真实色彩

1.5MP RED MAPLE COLOR CIS

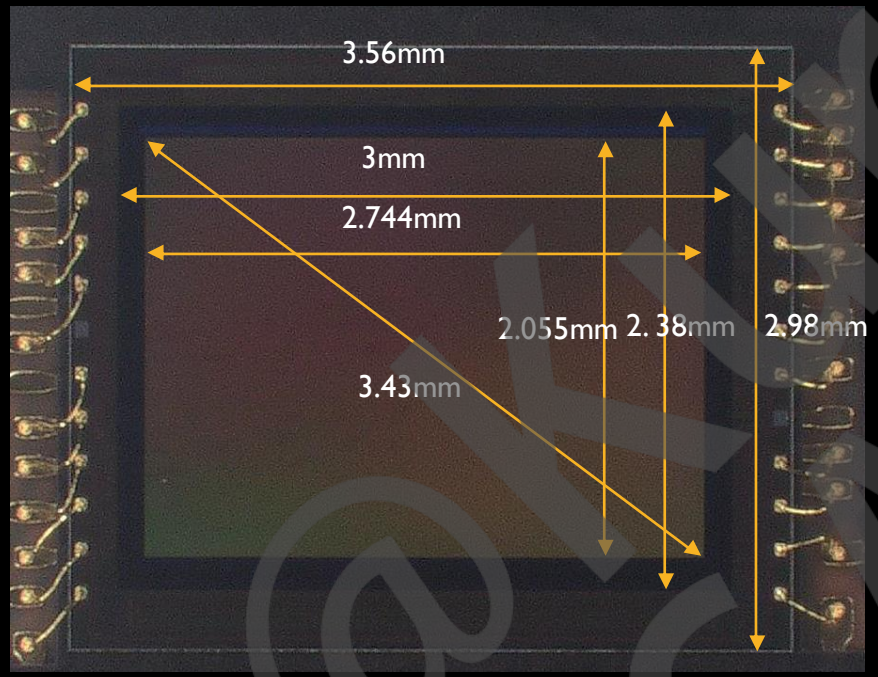
Pad number: 24
Pad in use: 22

Sub pad number: 26
Sub pad in use: 22



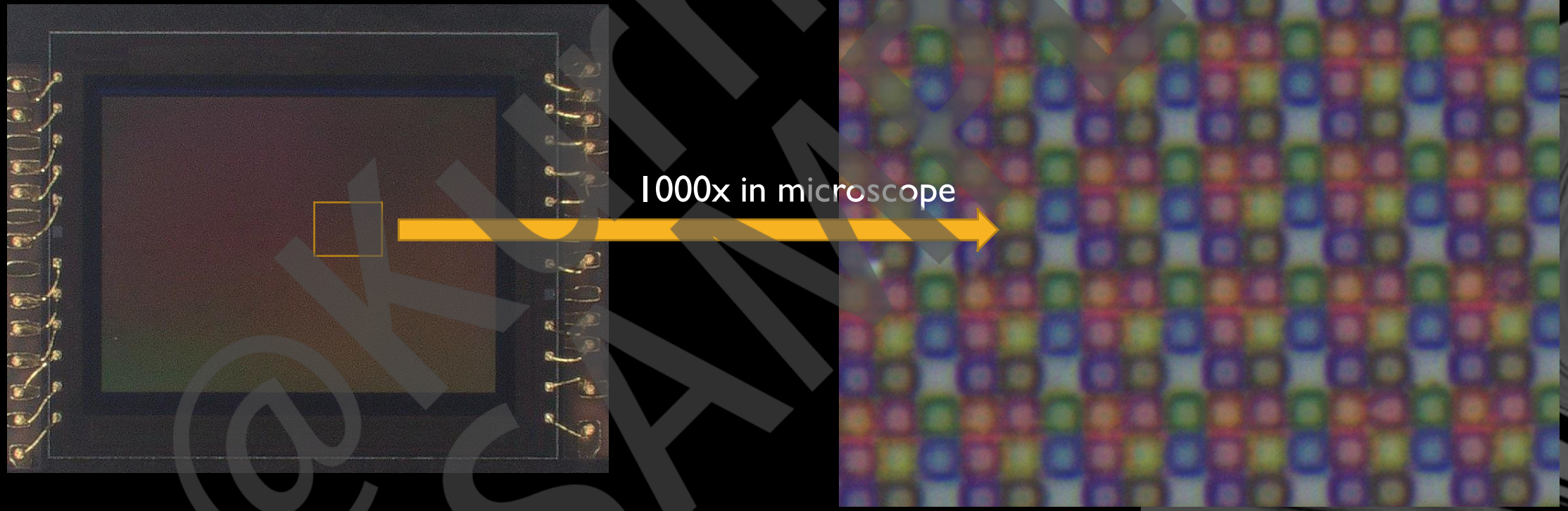
Mark:C42F03

1.5MP RED MAPLE COLOR CIS

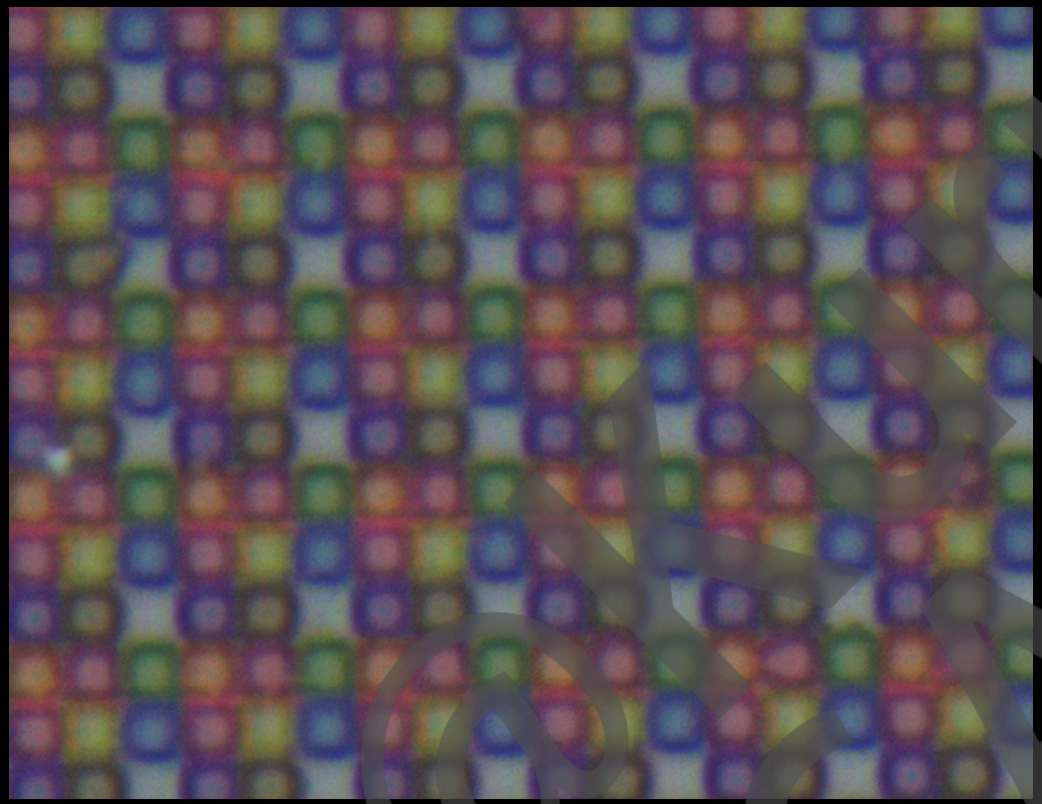


Full Diesize:	10.61mm2 (3.56mmx2.98mm)
Pixel area:	6.53mm2 (2.744mmx2.38mm)
Diagonal line size:	3.43mm (Nearly 1/4.67)

1.5MP RED MAPLE COLOR CIS



1.5MP RED MAPLE COLOR CIS



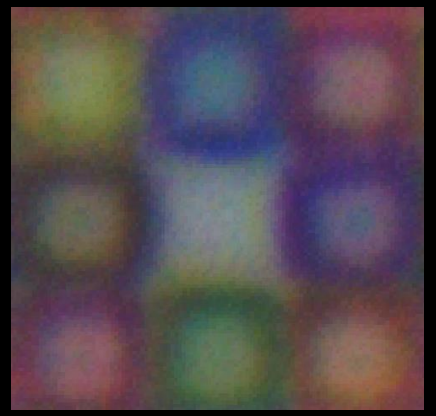
yellow Blue Red

Brown Clear Purple

Red Green Orange

Maybe?

1.5MP RED MAPLE COLOR CIS



yellow Blue Red

Brown Clear Purple

Red Green Orange

Why they have a Non OCL Pixel?

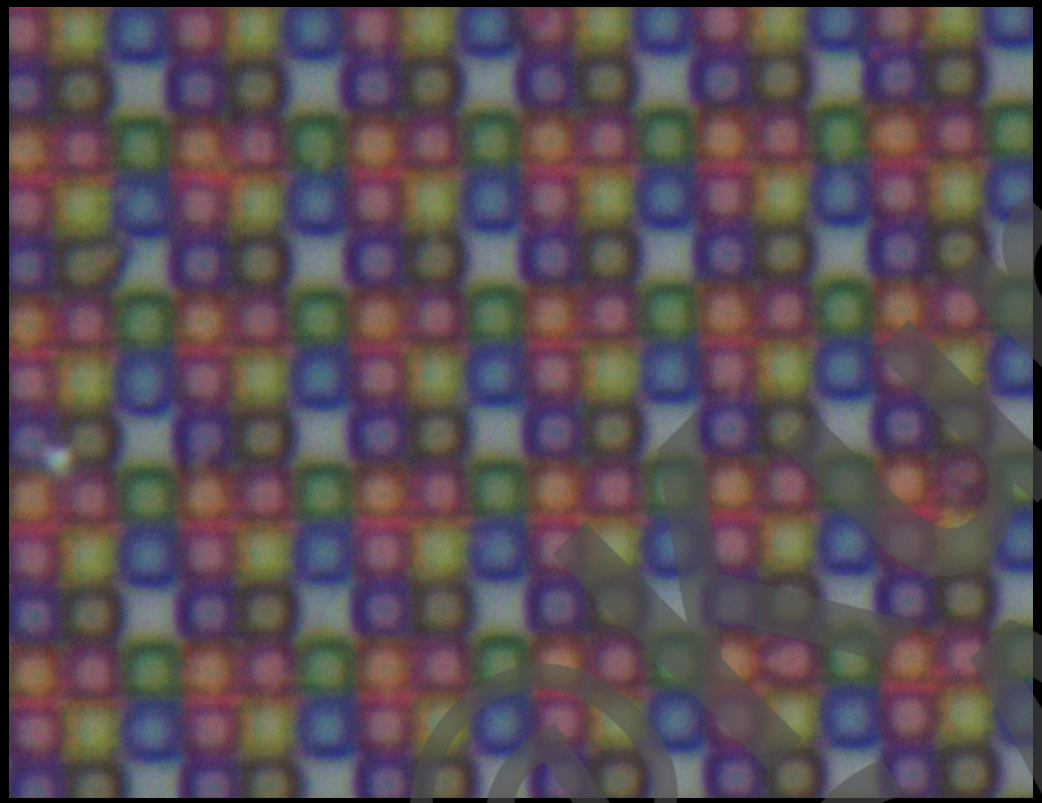
Answer is

The clear pixel is used as an intermediate pixel

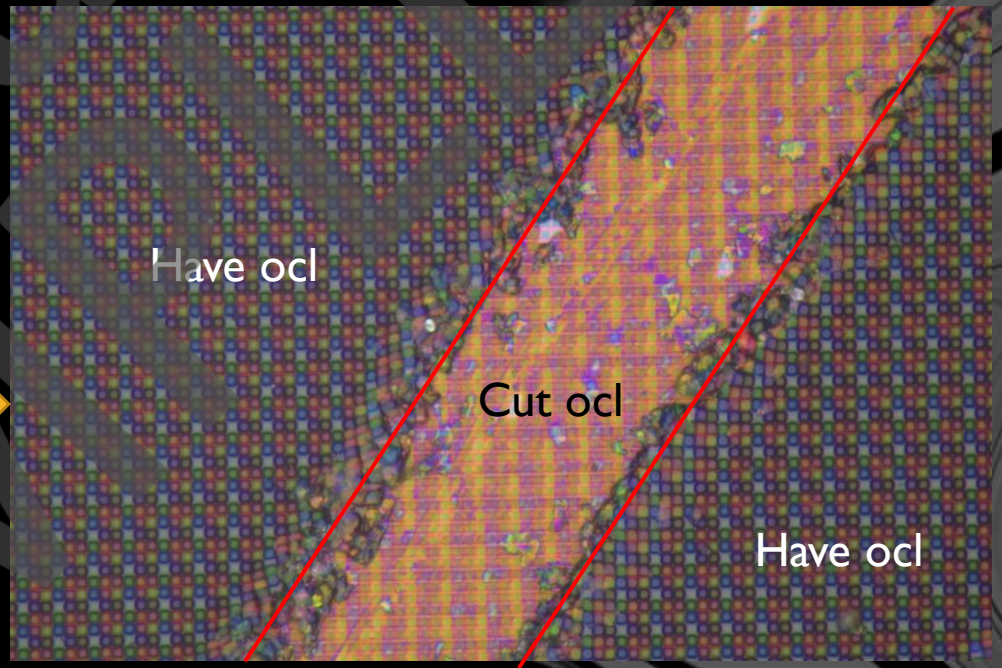
Accurate ambient color temperature can be obtained by combining with surrounding pixel information

And the algorithm can obtain color information far more than 8 color channels

1.5MP RED MAPLE COLOR CIS



Cut ocl



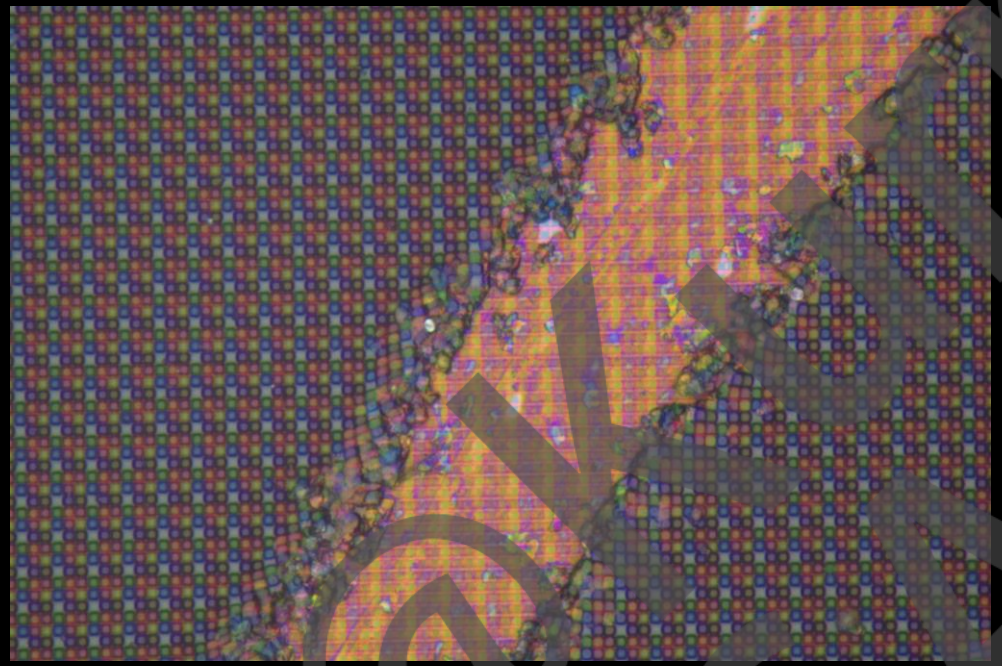
1.5MP RED MAPLE COLOR CIS

The no OCL pixel in the centre,
there is still have a trap underneath.

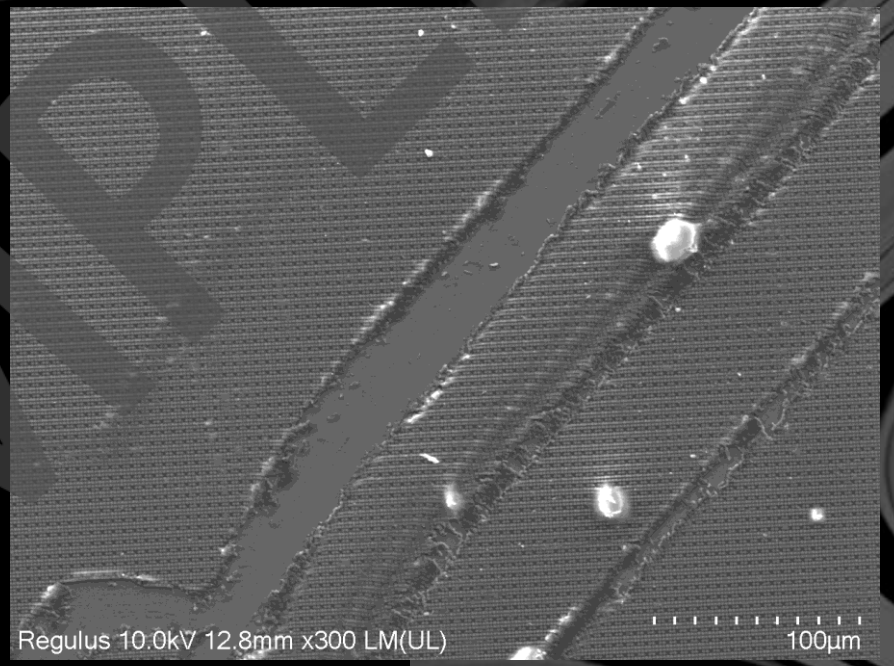
Have OCL

Cut OCL

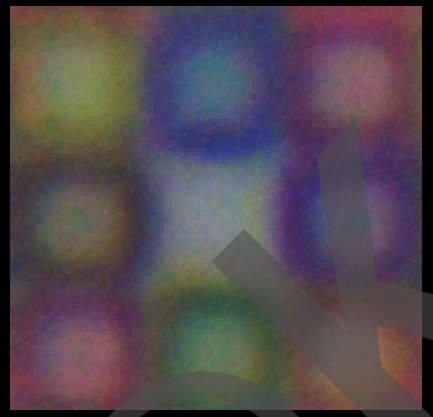
1.5MP RED MAPLE COLOR CIS

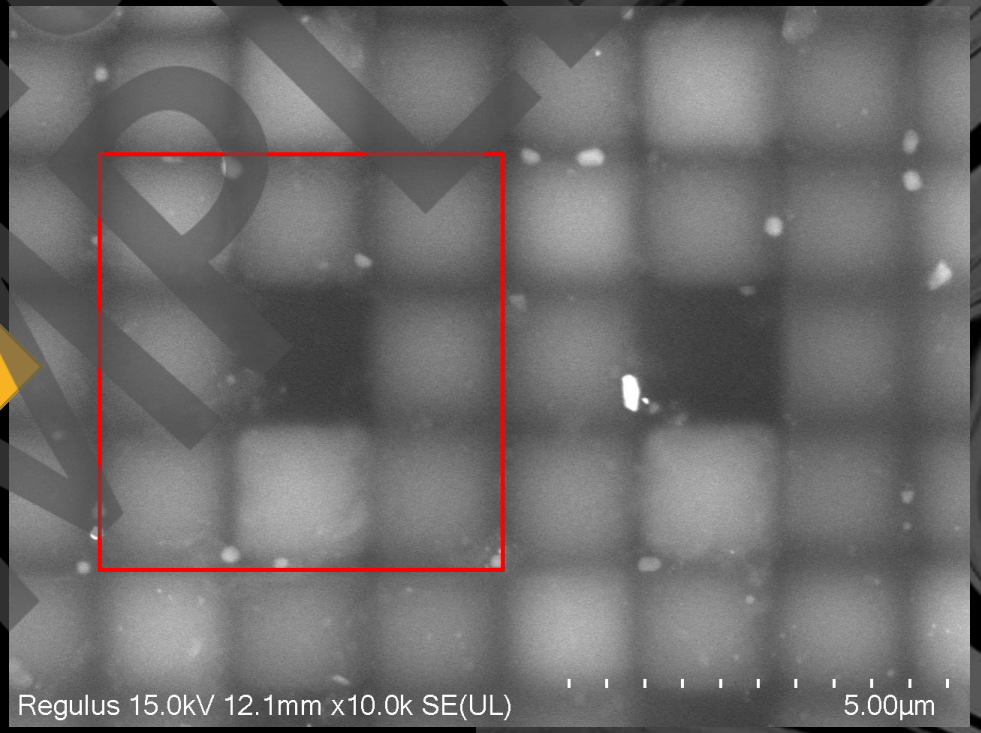


Use SEM

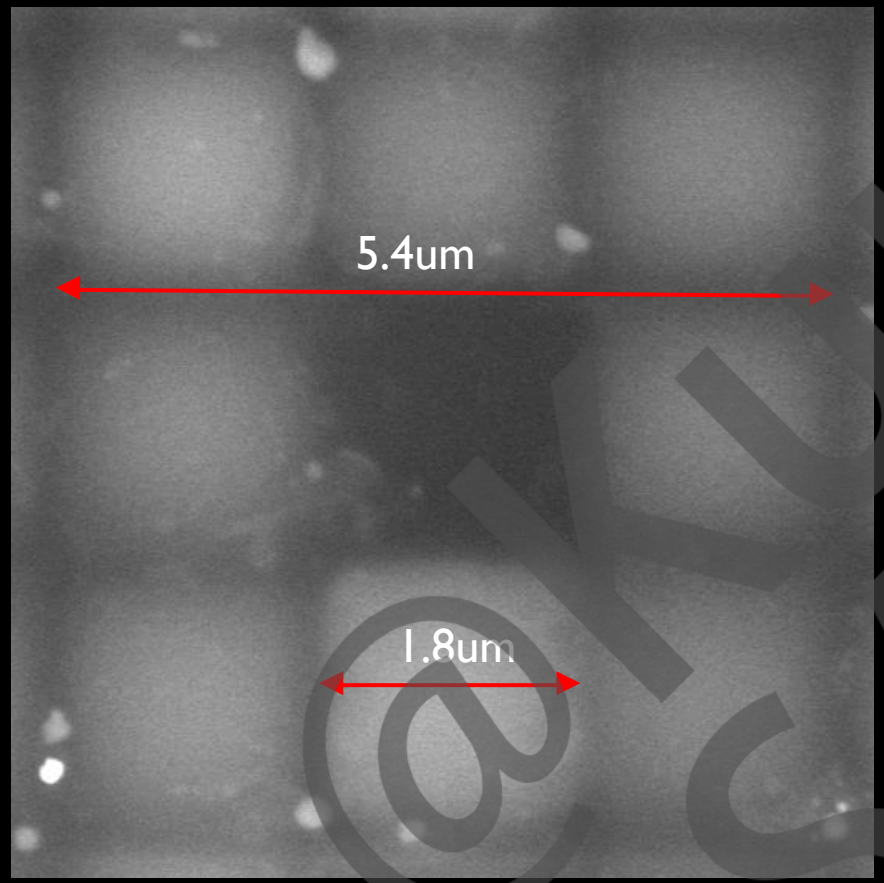


1.5MP RED MAPLE COLOR CIS





1.5MP RED MAPLE COLOR CIS



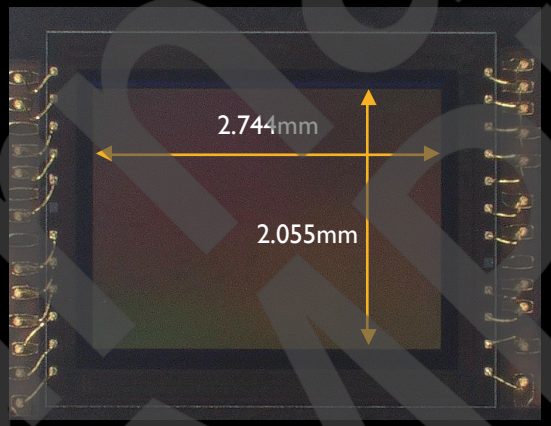
Pixel size: 1.8um
Pixel cluster size: 5.4um x 5.4um

1.5MP RED MAPLE COLOR CIS

So
Why Huawei Says
They have
1.5 million multi-spectral channels

1.5MP RED MAPLE COLOR CIS

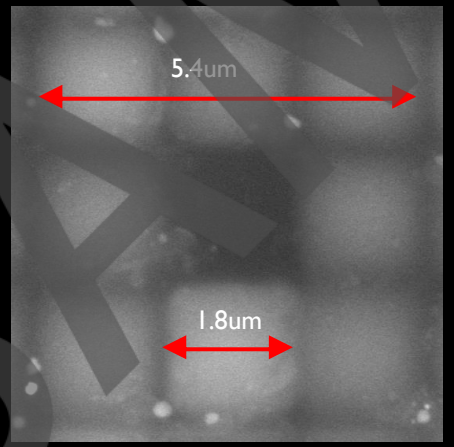
We know:
Pixel area size:2.744mmx2.055mm



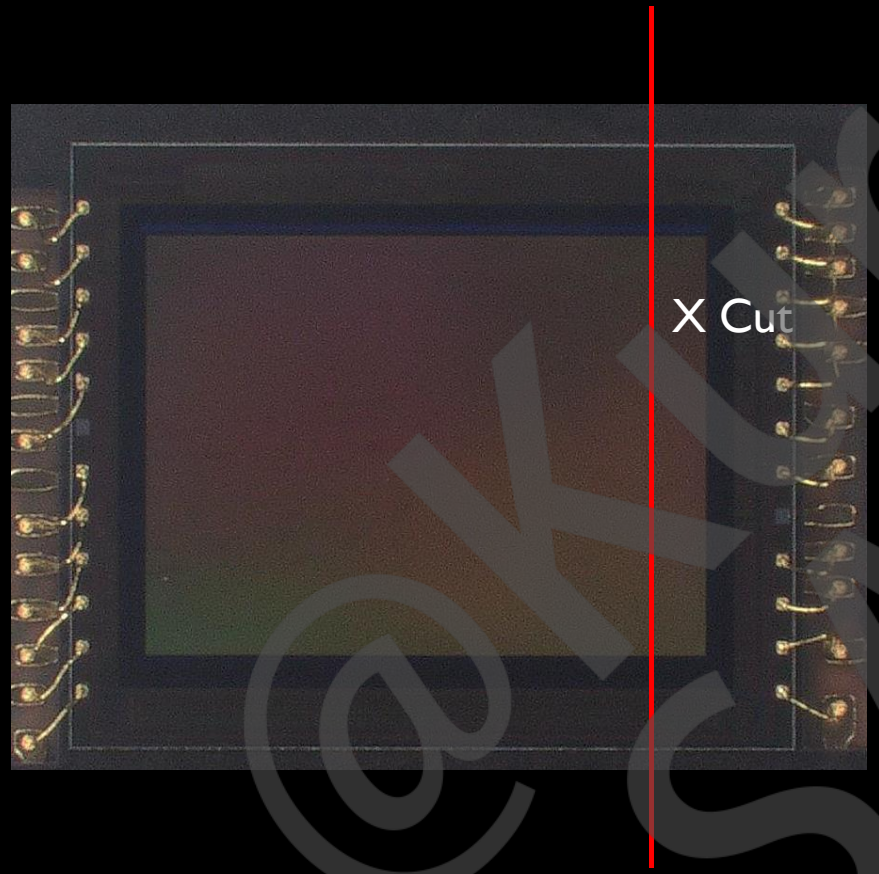
And
Pixel Size=1.8um

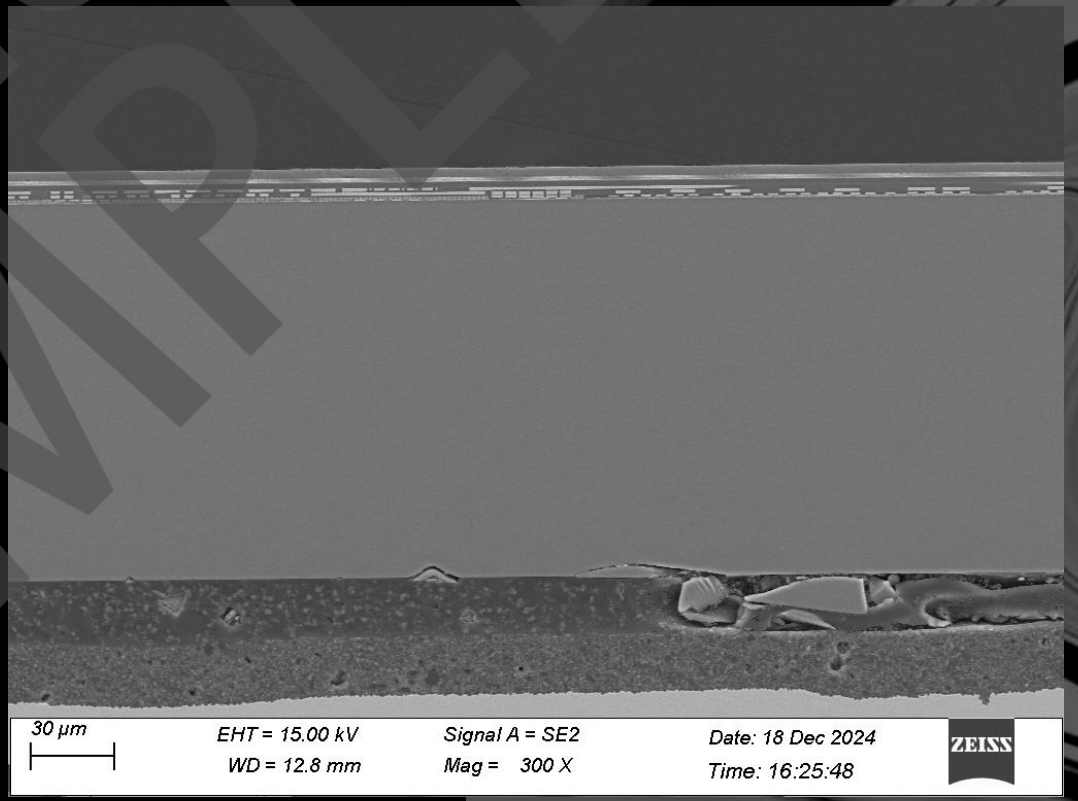
Then
we can compute how many Pixel they have

Maybe they have 1.74MP Pixel (1141x1524)
And maybe have 128x170 Pixel array

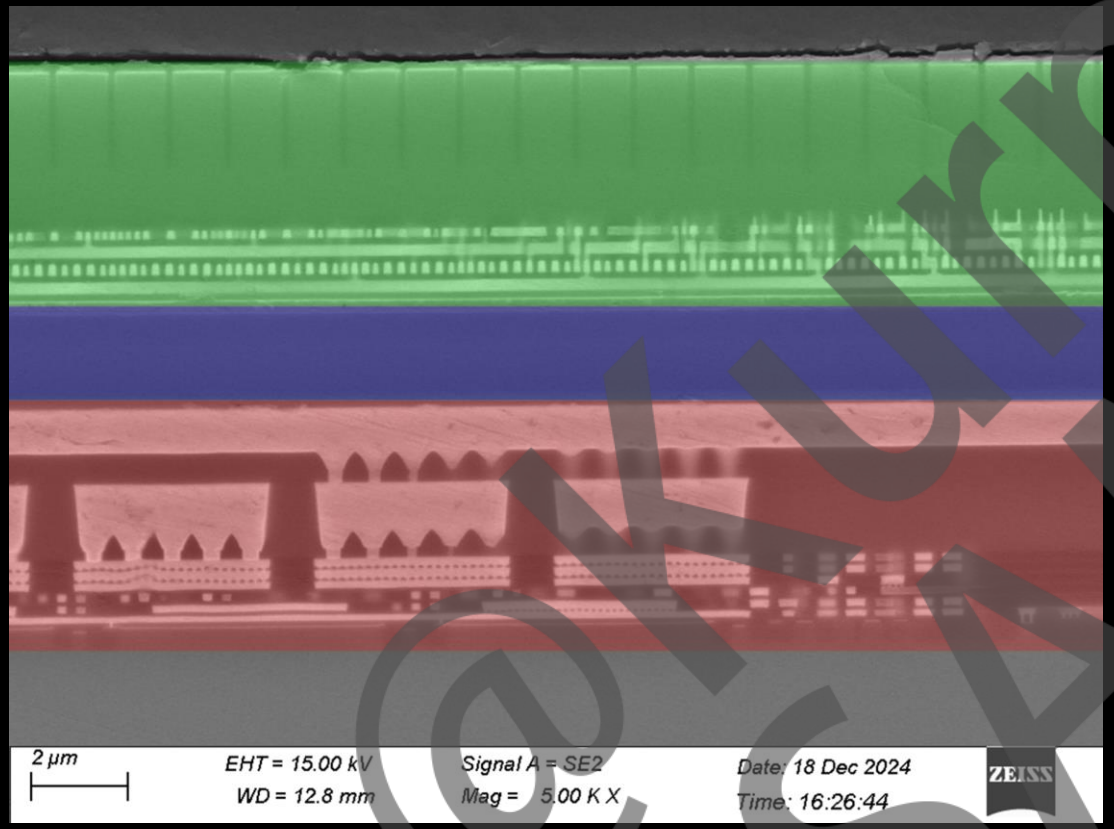


1.5MP RED MAPLE COLOR CIS





1.5MP RED MAPLE COLOR CIS



Cut OCL…sad

Pixel Wafer

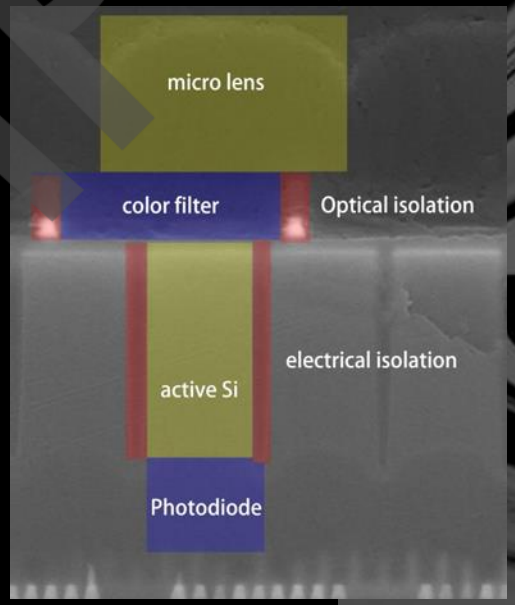
Filling Layer

Logic Wafer

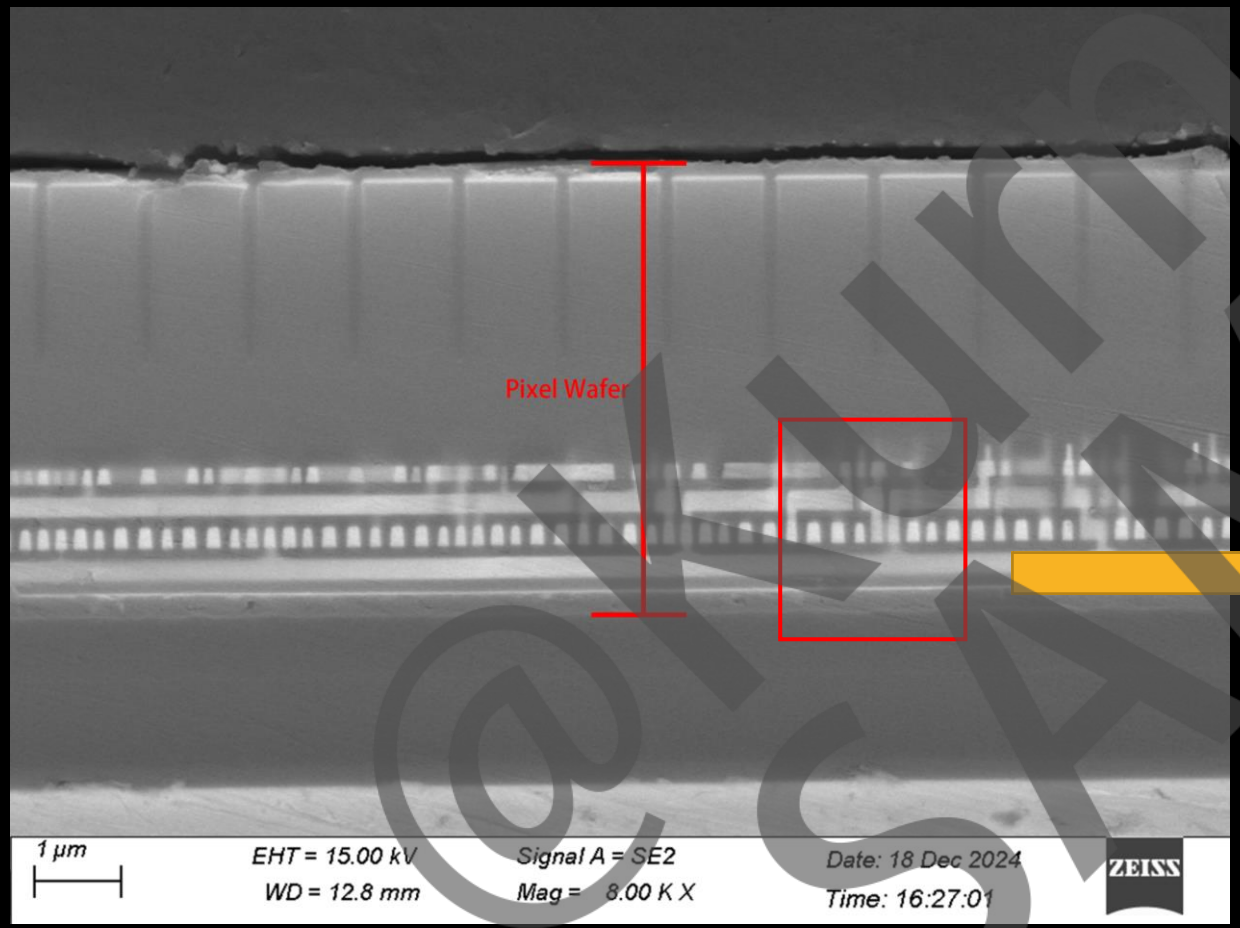
Total (no OCL) Height:	12.358um
Pixel wafer(no OCL) Height:	5.3um
Filling Layer Height:	2.023um
Logic wafer Height:	5.0um

1.5MP RED MAPLE COLOR CIS

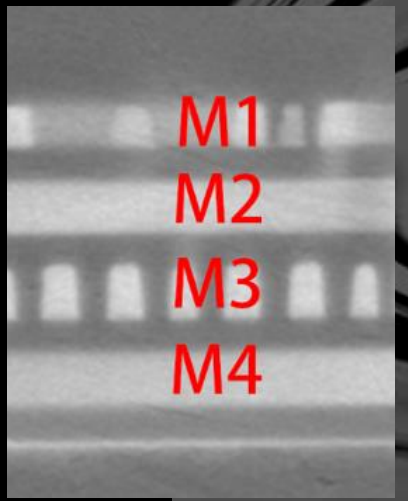
Color filter to Metal 1 Depth: 3.4um
Electrical isolation Depth: 2.178um



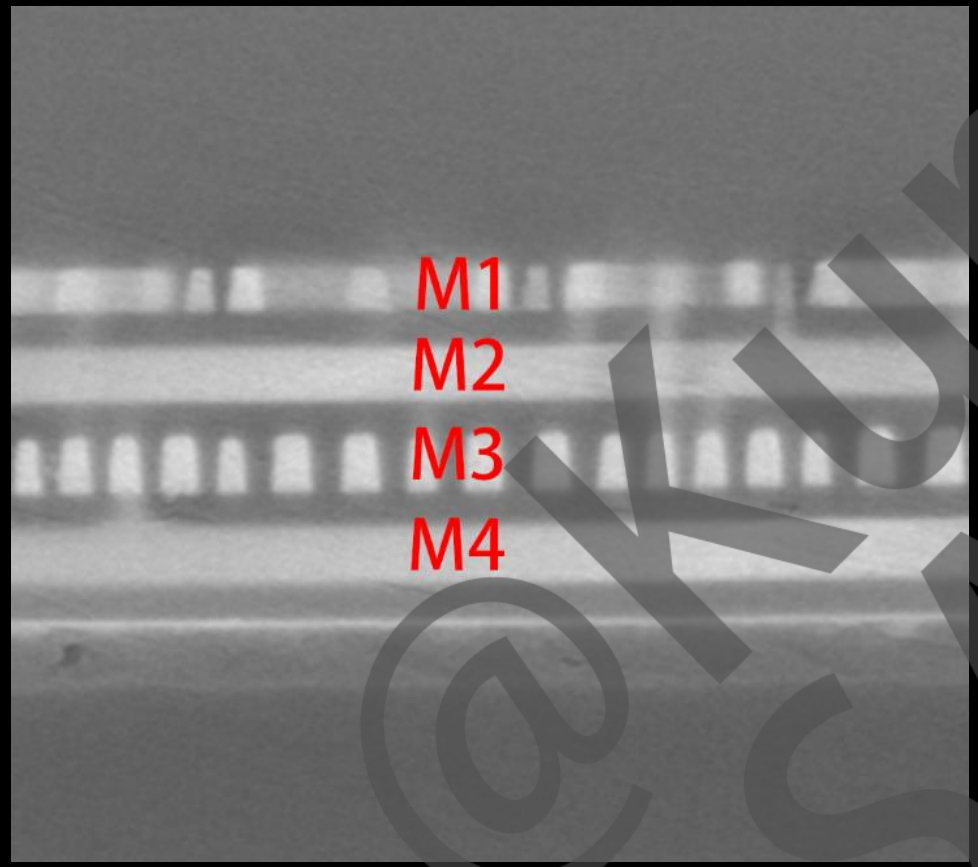
1.5MP RED MAPLE COLOR CIS



Metal Layers in Pixel Wafer: 4 layers



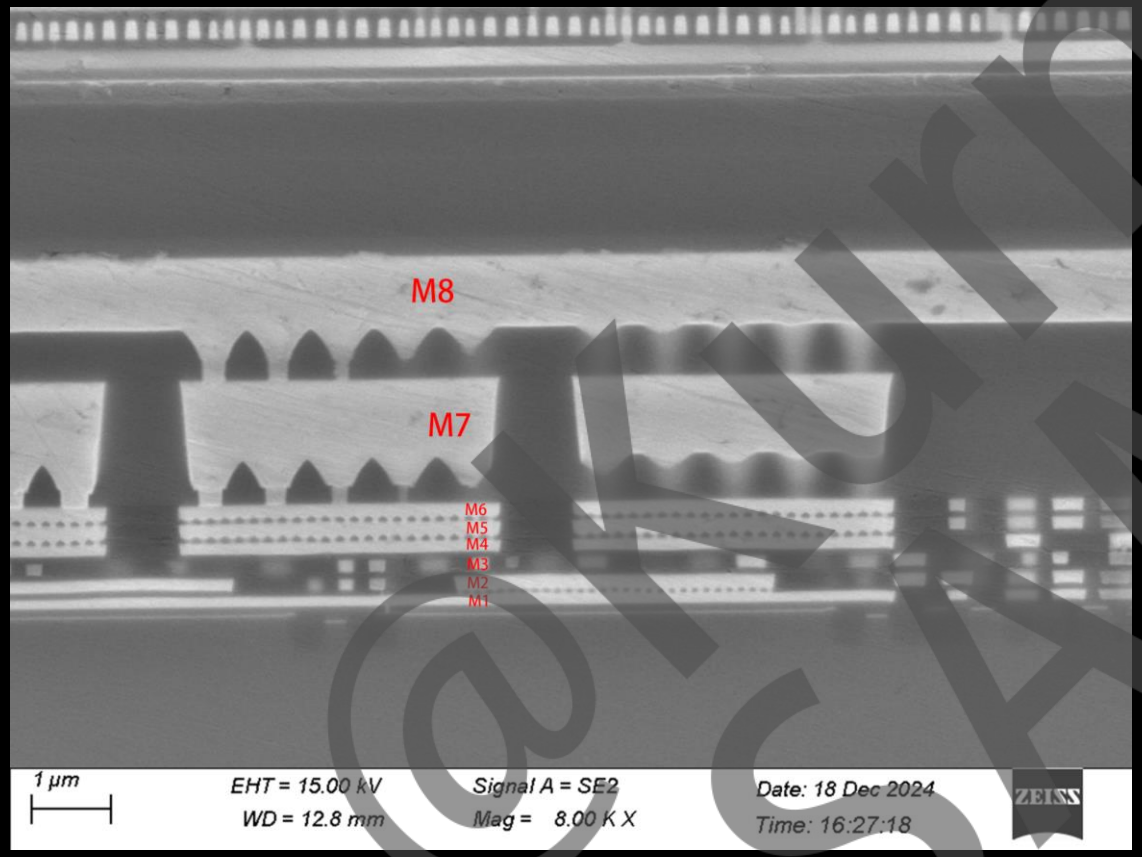
1.5MP RED MAPLE COLOR CIS



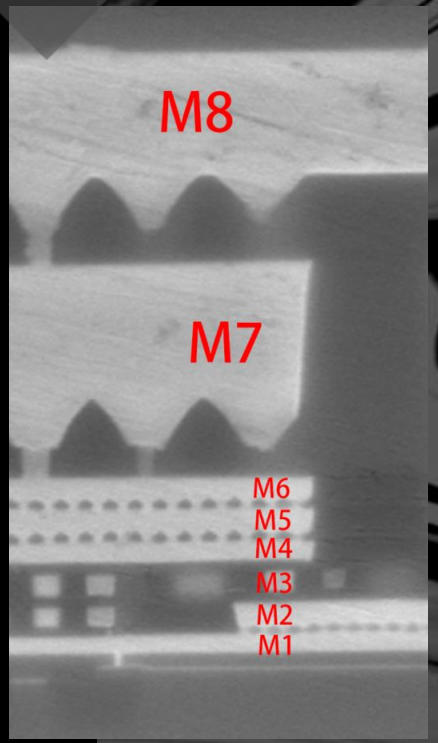
	(Just)Thickness	Pitch
M1	181nm	170nm
M2	220nm	x
M3	220nm	248nm
M4	220nm	x

1.5mp red maple Pixel Metal data

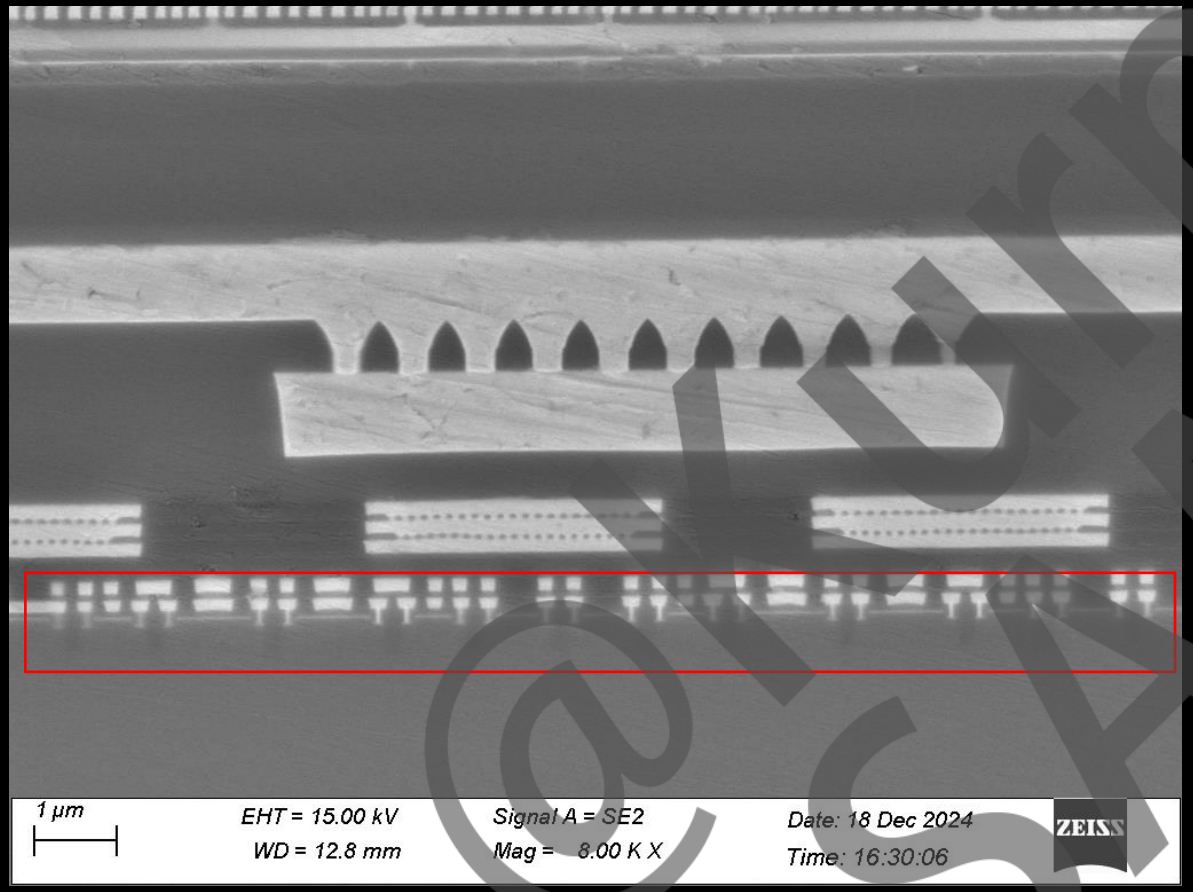
1.5MP RED MAPLE COLOR CIS



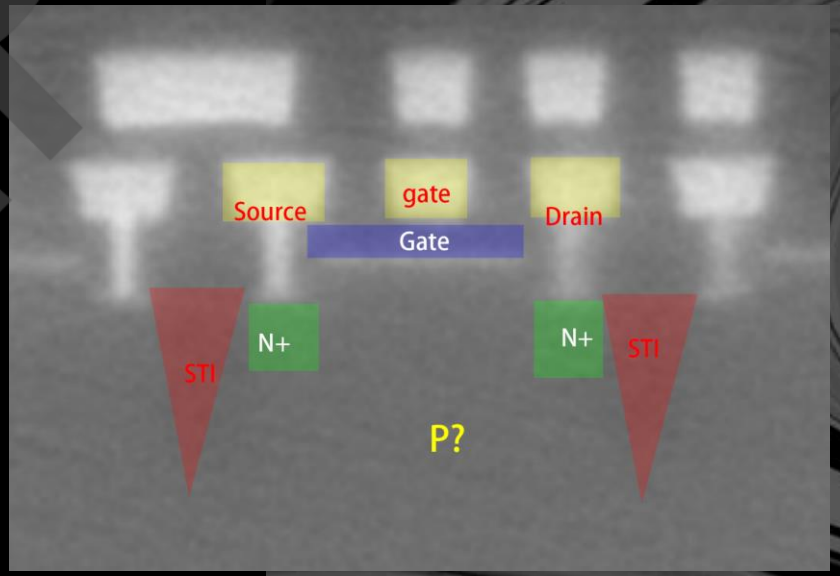
Metal Layers in Logic Wafer: 1P 8M



1.5MP RED MAPLE COLOR CIS

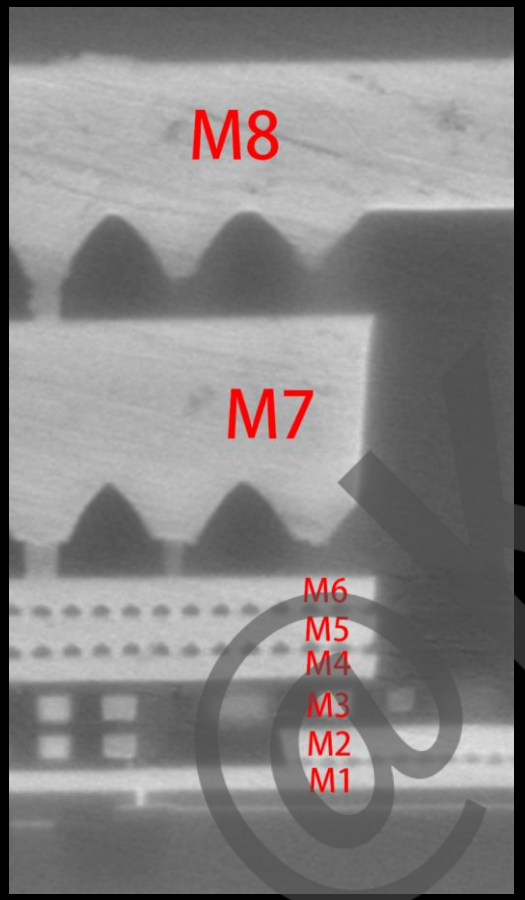


MosFET



Logic wafer Mosfet

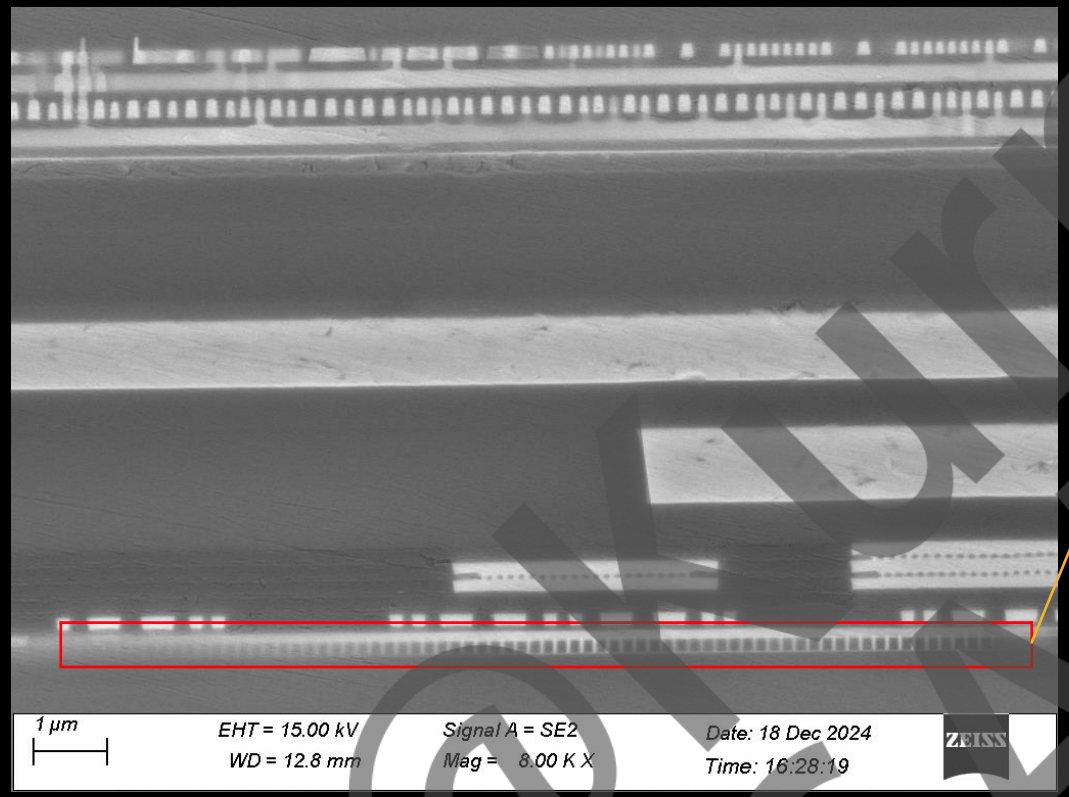
1.5MP RED MAPLE COLOR CIS



	(Just)Thickness	Pitch
M1	120nm	X
M2	150nm	X
M3	150nm	X
M4	150nm	X
M5	150nm	X
M6	150nm	X
M7	1000nm	X
M8	900nm	x

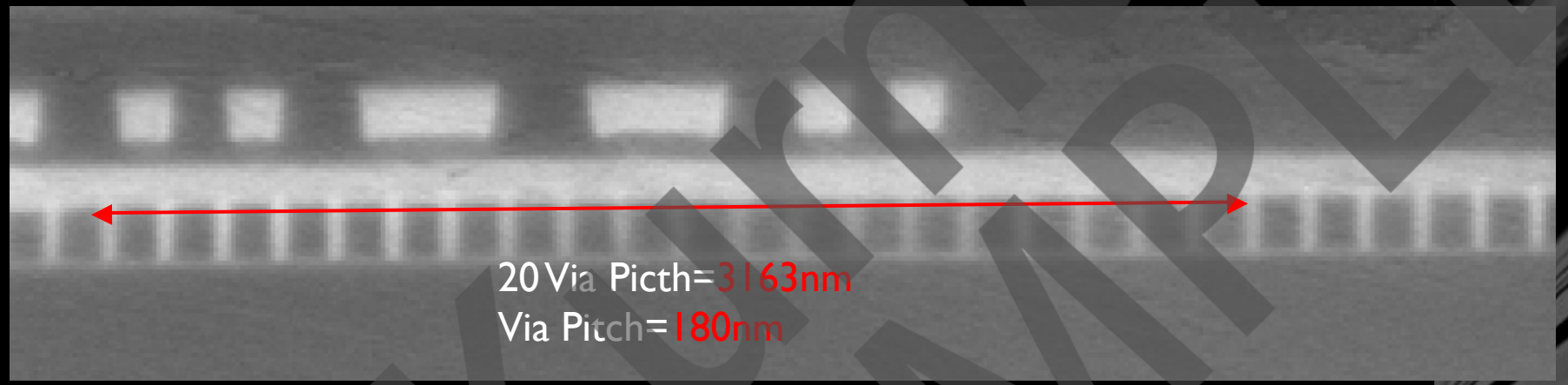
1.5mp red maple Logic Metal data

1.5MP RED MAPLE COLOR CIS



For this Photo
We can see the dense lines in the Via 1
Then we can know the Via 1 Pitch,
Then Estimating process

1.5MP RED MAPLE COLOR CIS

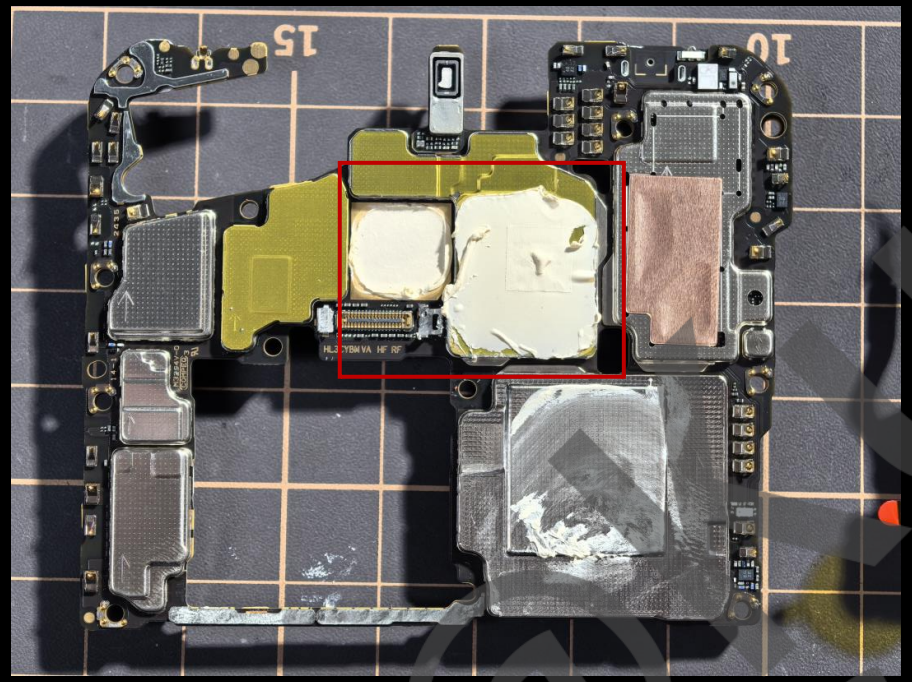


for Metal data and Via data and Mosfet data
I think this chip Logic wafer Like TSMC 65nm?

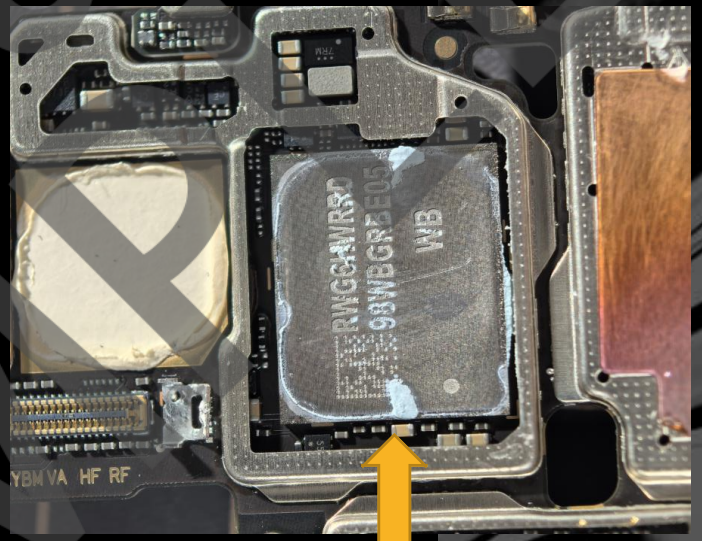
NAND(UFS)

@Kurnal

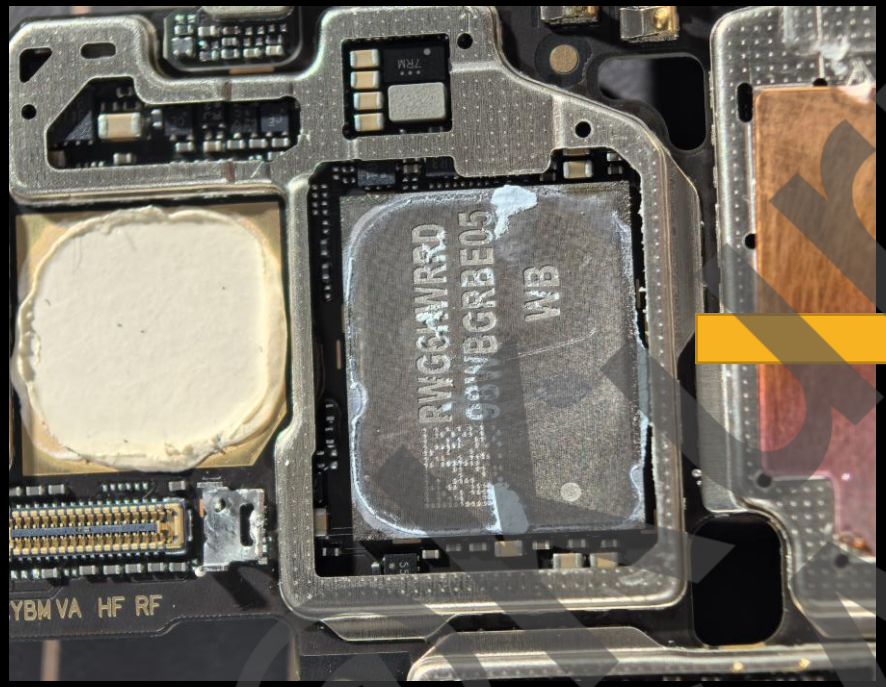
MATE70PRO+ NAND

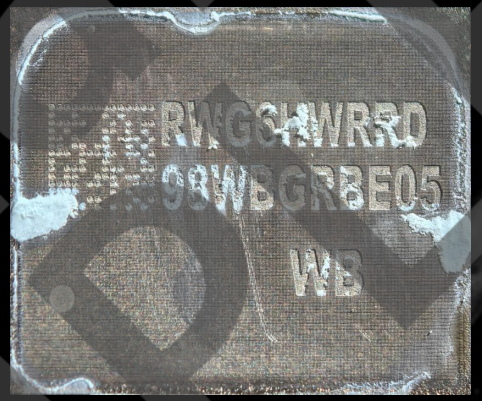


Remove the shield



MATE70PRO+ NAND





Front

Back

MATE70PRO+ NAND

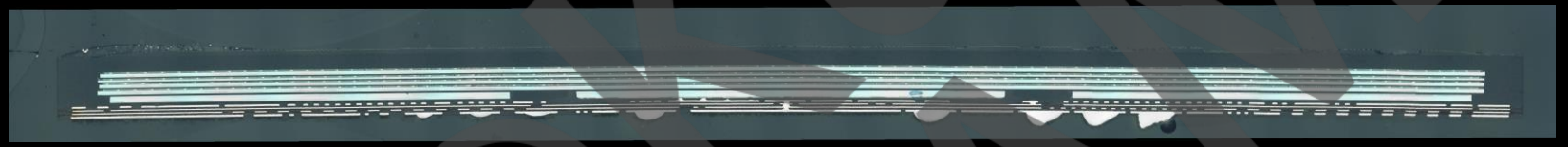
RWG6HWRRD
98WBGRBE05
WB

Encrypted Topmark

BGA133

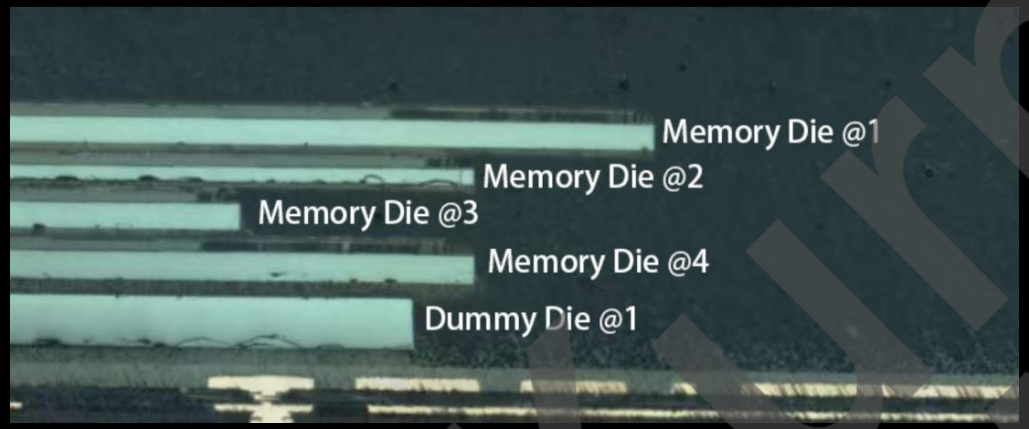
MATE70PRO+ NAND

Package in X Cut



Package in Y Cut

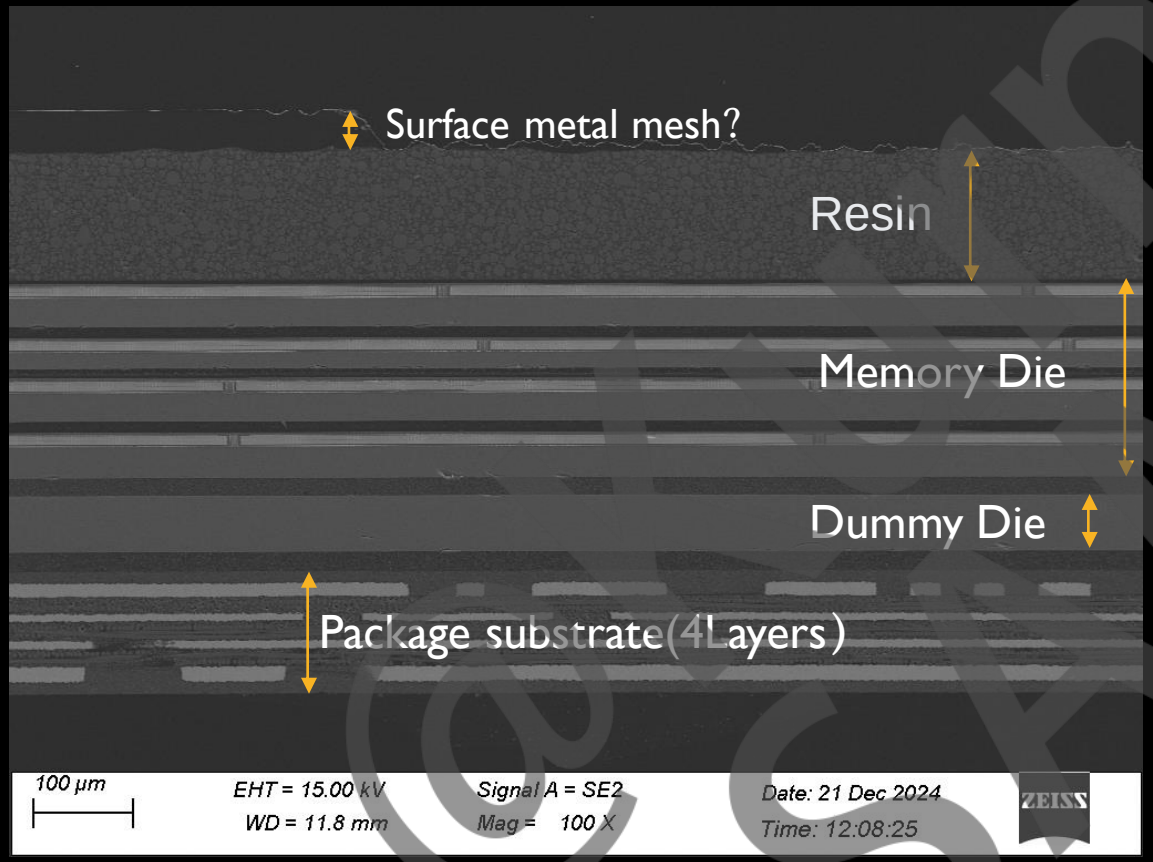
MATE70PRO+ NAND

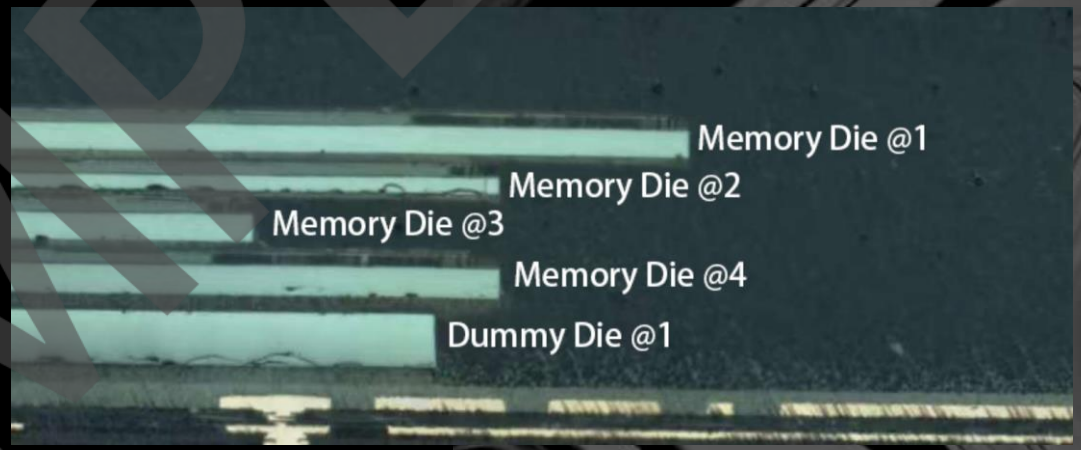


The memory package integrates a total of 4 memory chips

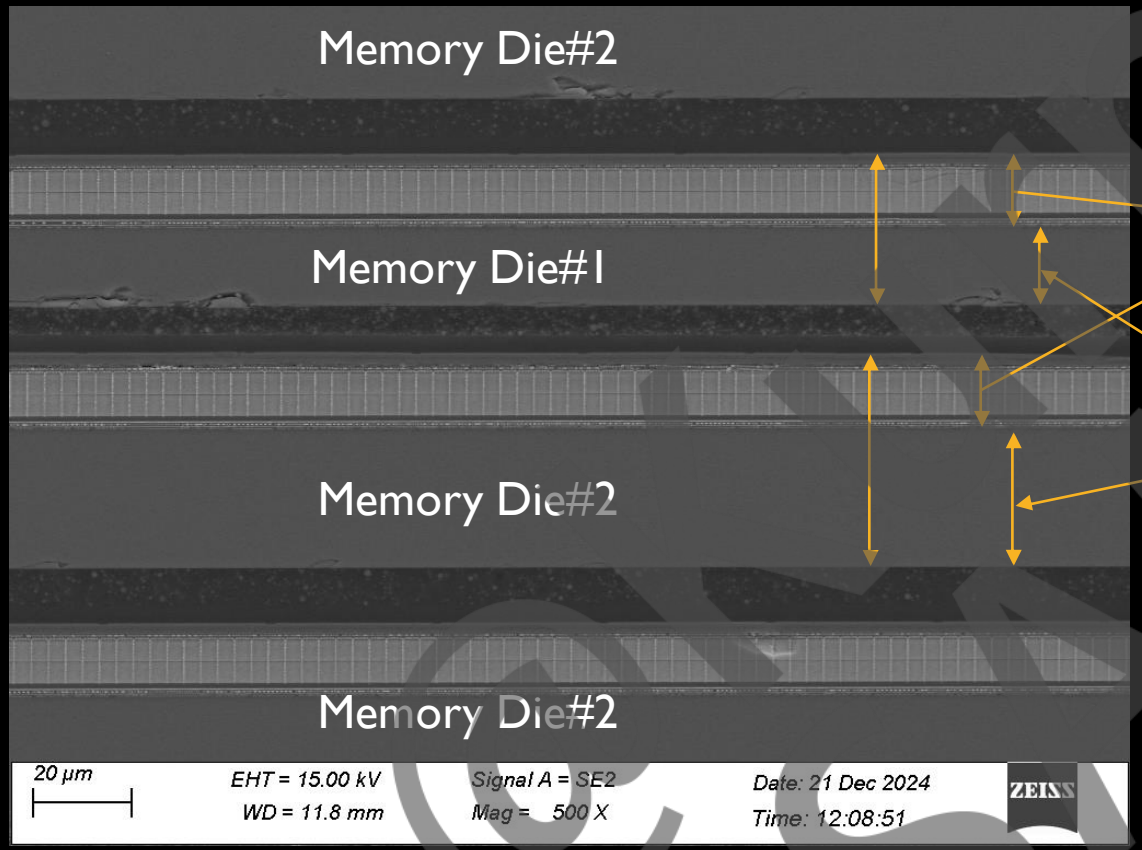
Package Capacity: 512GB
Die Capacity: 512GB/4
128GB

MATE70PRO+ NAND





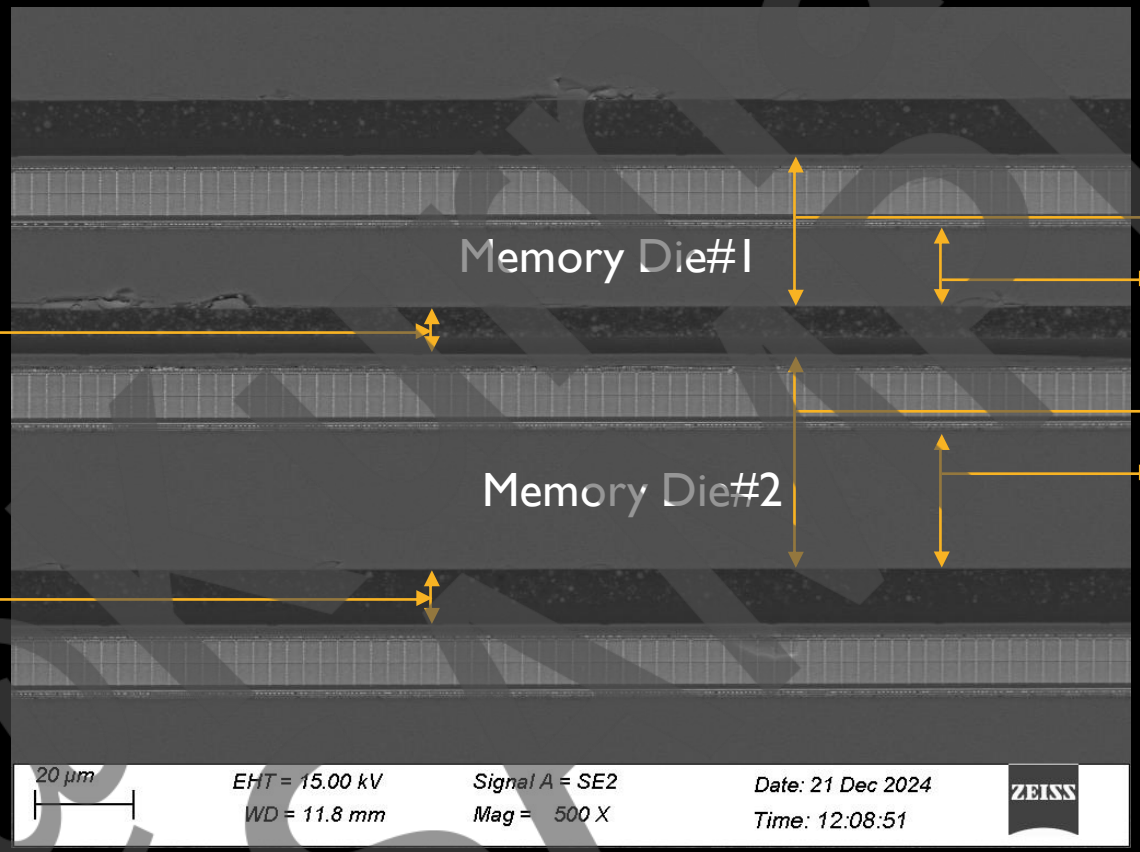
MATE70PRO+ NAND



Same Thickness: 15.28um

There are two thicknesses of Memory Die #1/#2.
The only difference is the Si Sub thickness.

MATE70PRO+ NAND



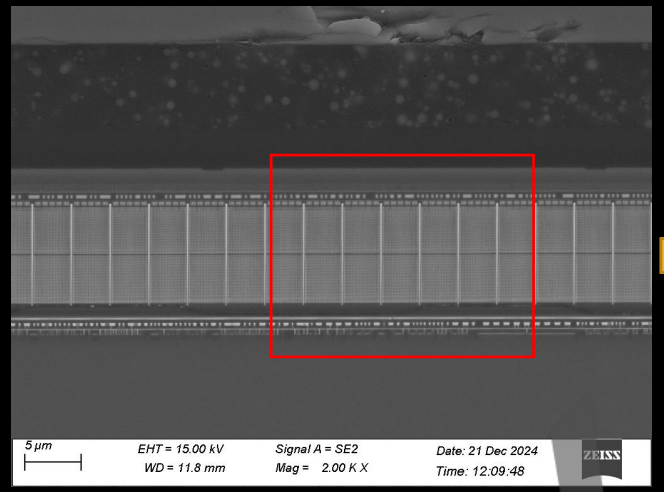
Adhesive#1:
9.282um

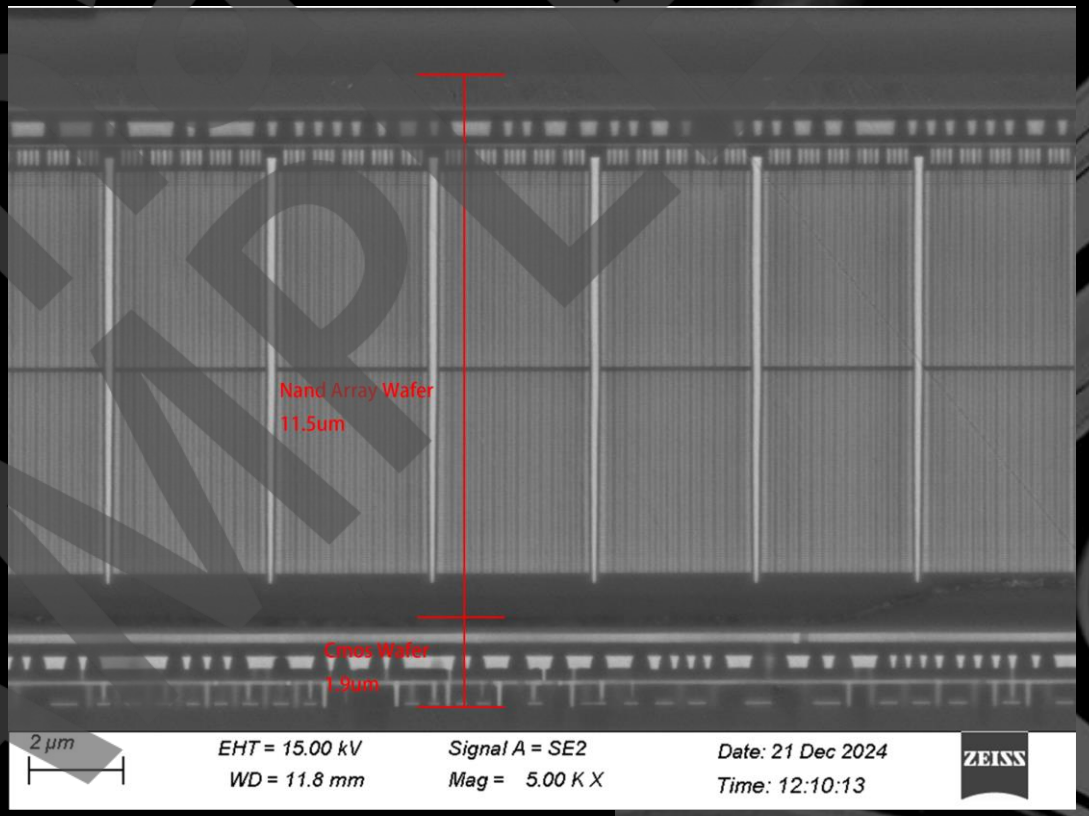
Adhesive#2:
11.027um

Memory Die #1 Thickness: 30.927um
Si Sub Thickness: 15.816um

Memory Die #2 Thickness: 43.328um
Si Sub Thickness: 28.078um

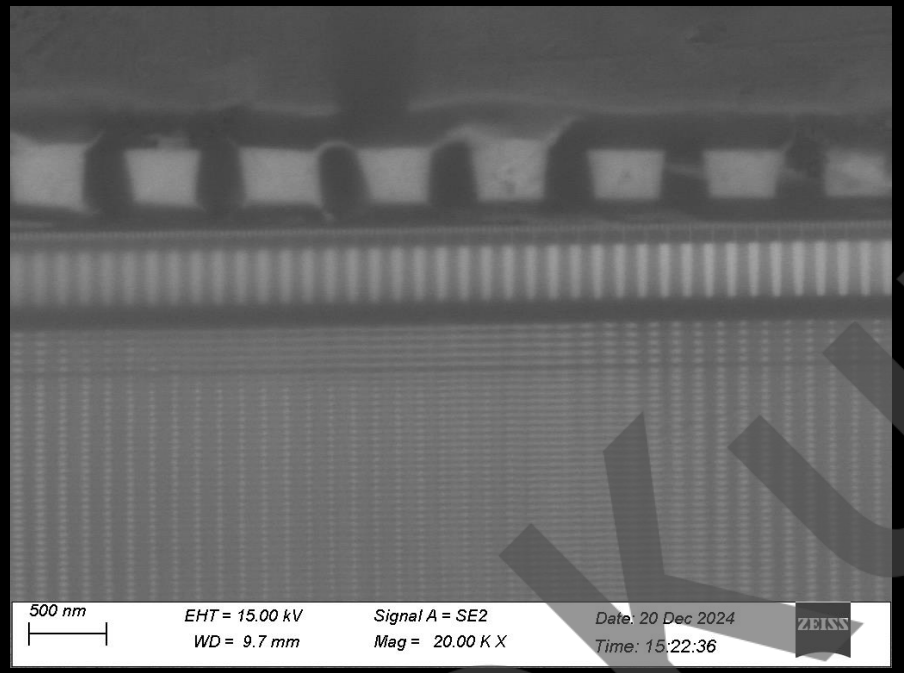
MATE70PRO+ NAND

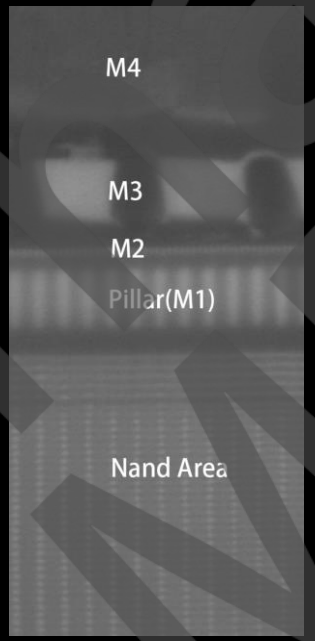




Nand Array Wafer : 11.5um
Cmos Wafer: 1.9um

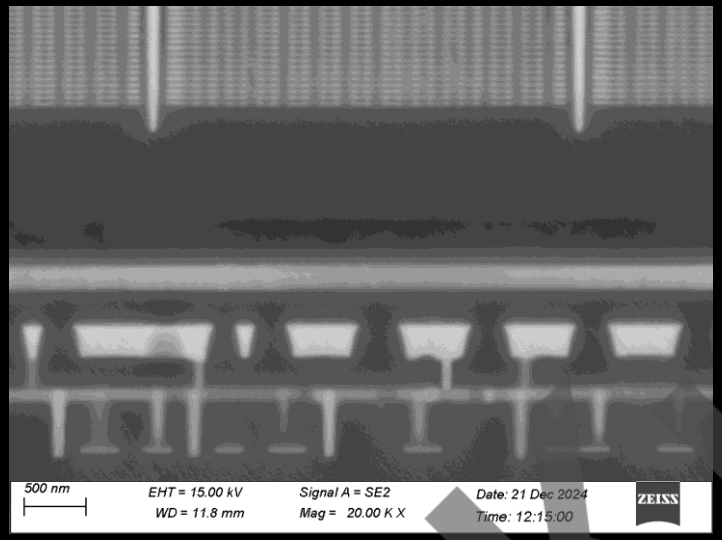
MATE70PRO+ NAND

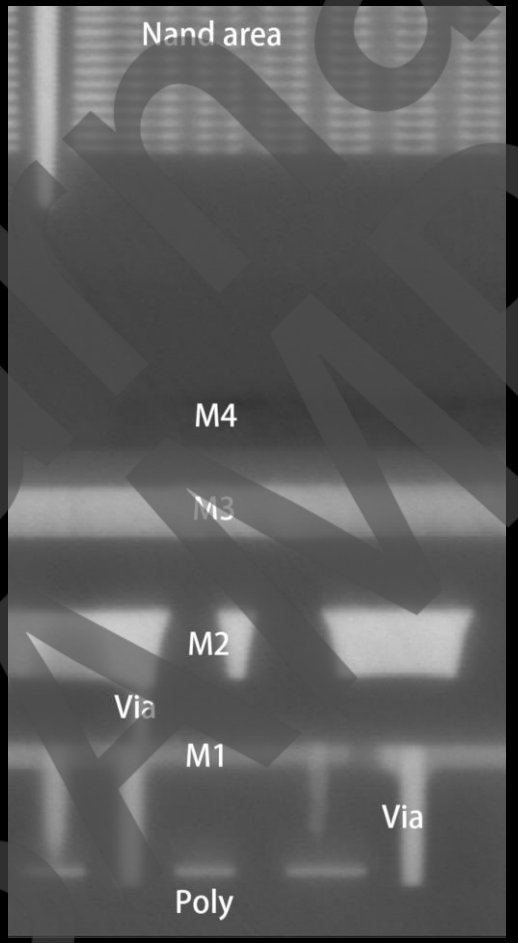




Nand Wafer use 4 Metal Layers

MATE70PRO+ NAND



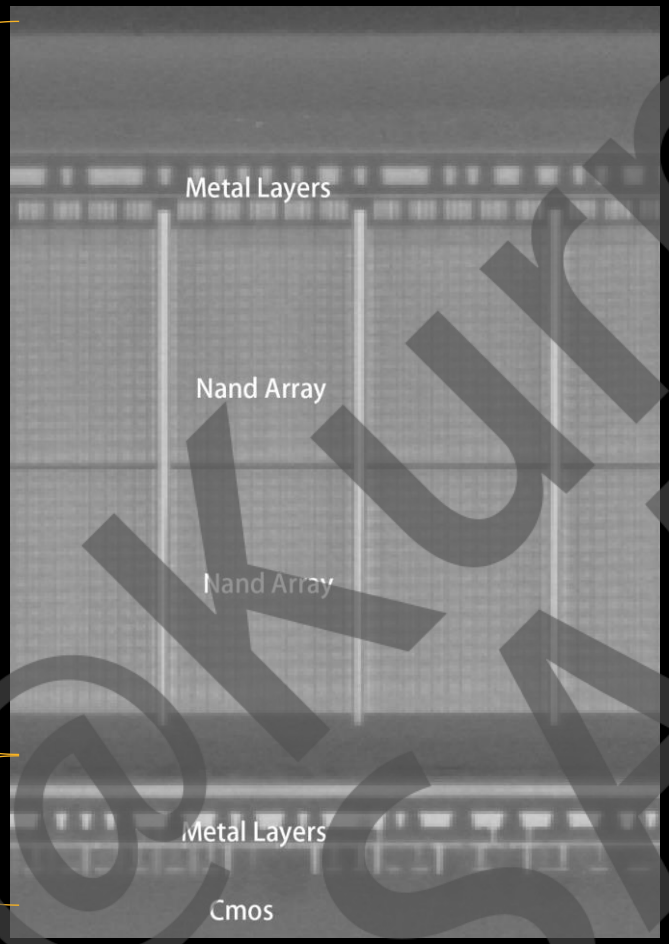


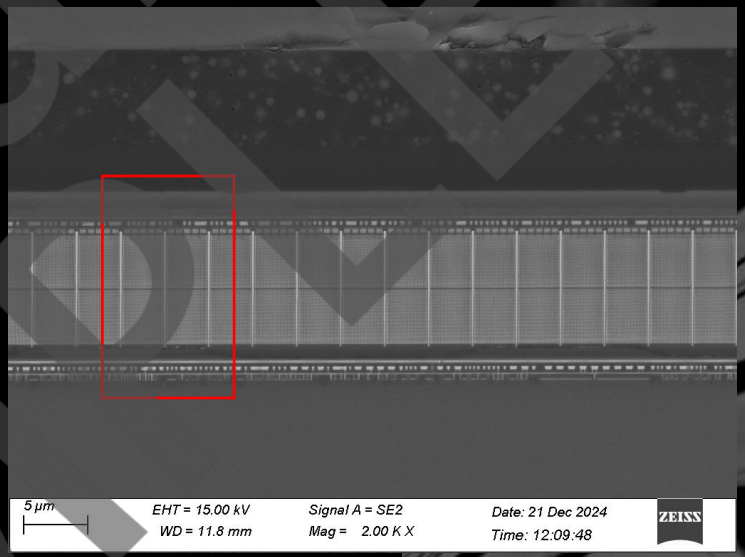
Cmos Wafer use 4 Metal Layers

MATE70PRO+ NAND

Nand Array Wafer

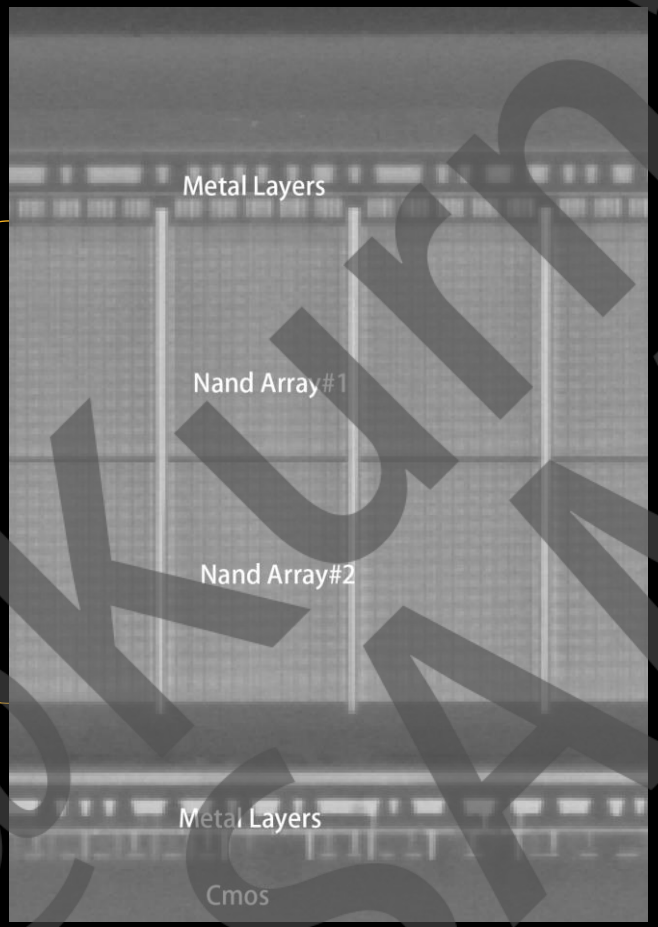
Cmos Wafer

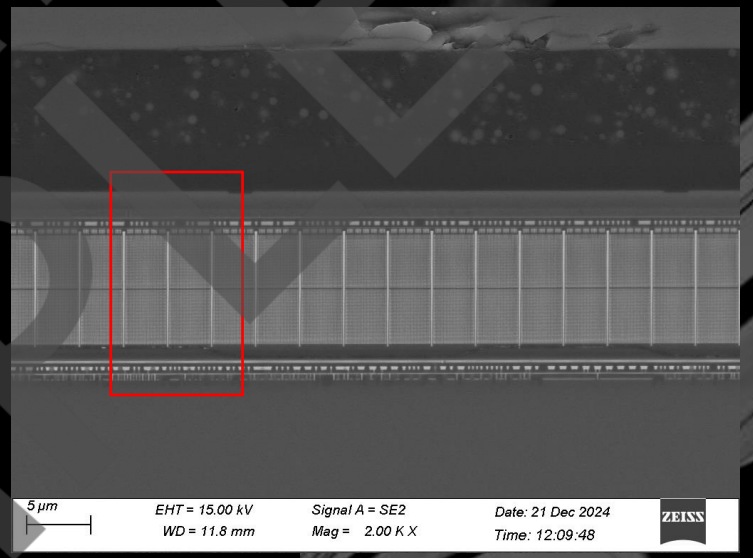




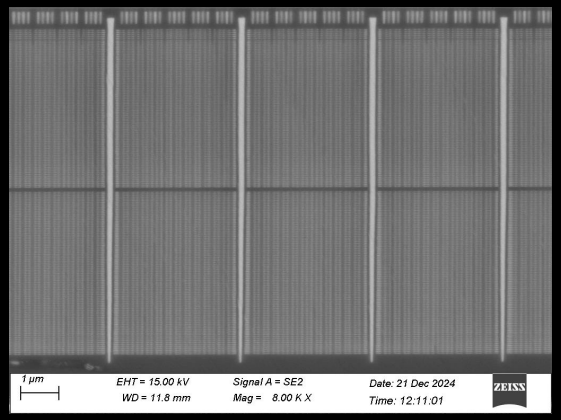
MATE70PRO+ NAND

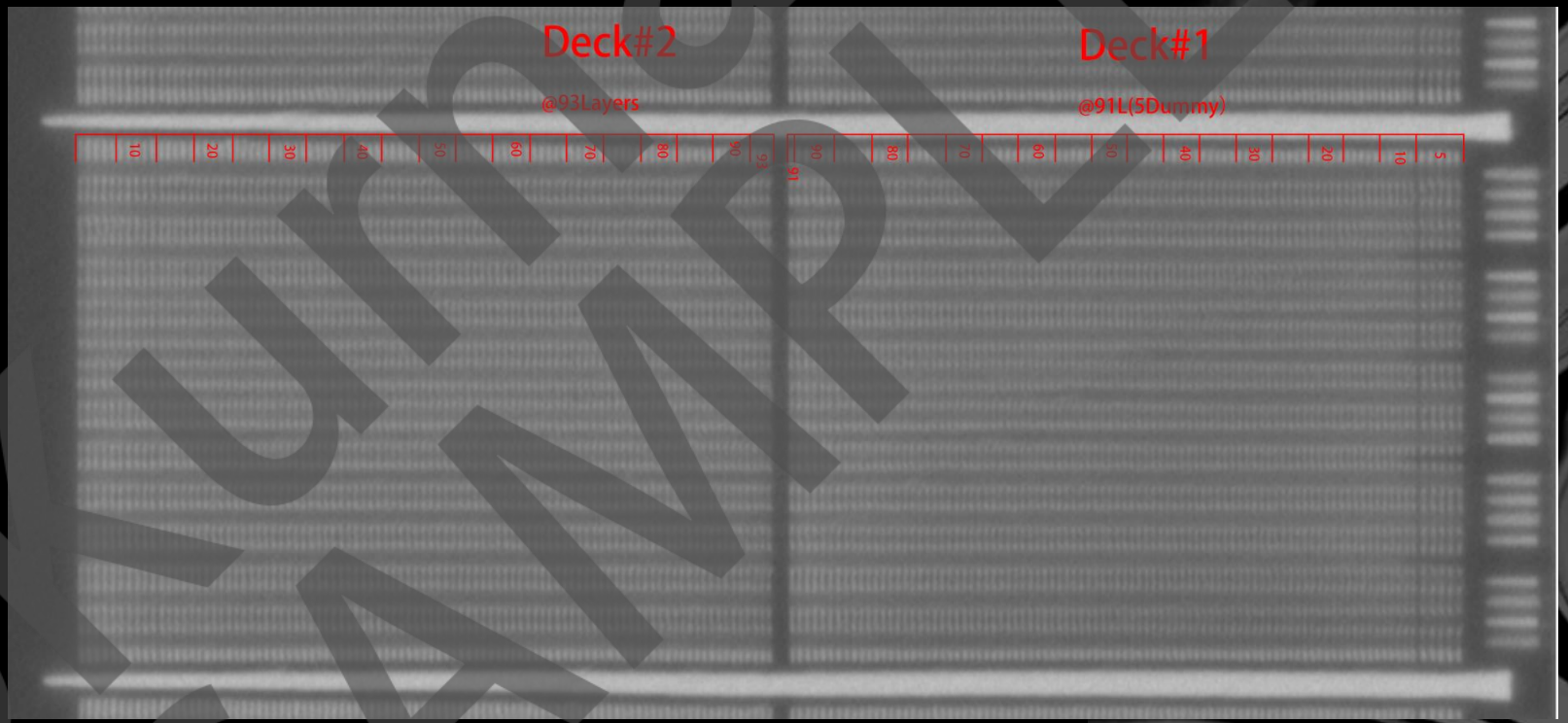
The Nand Array made of Deck1 and Deck2





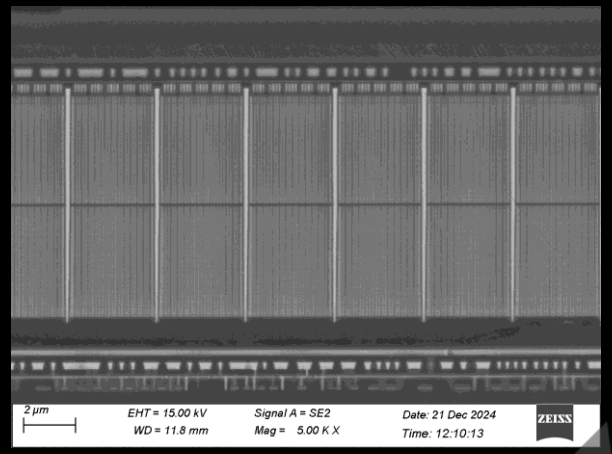
MATE70PRO+ NAND



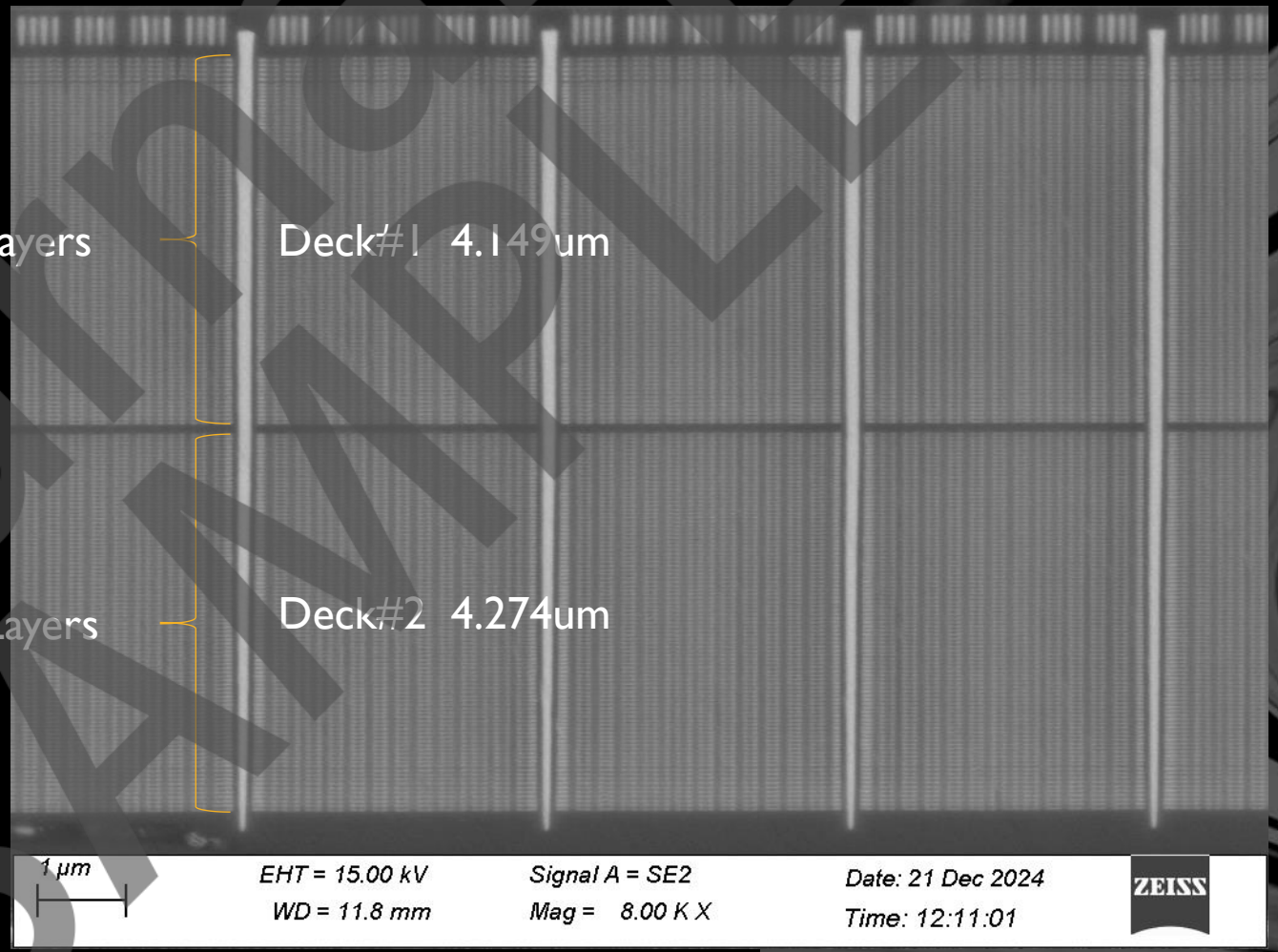


Deck#1 Layers	91
Dummy Layers	5
Deck#2 Layers	93
Total Layers	179

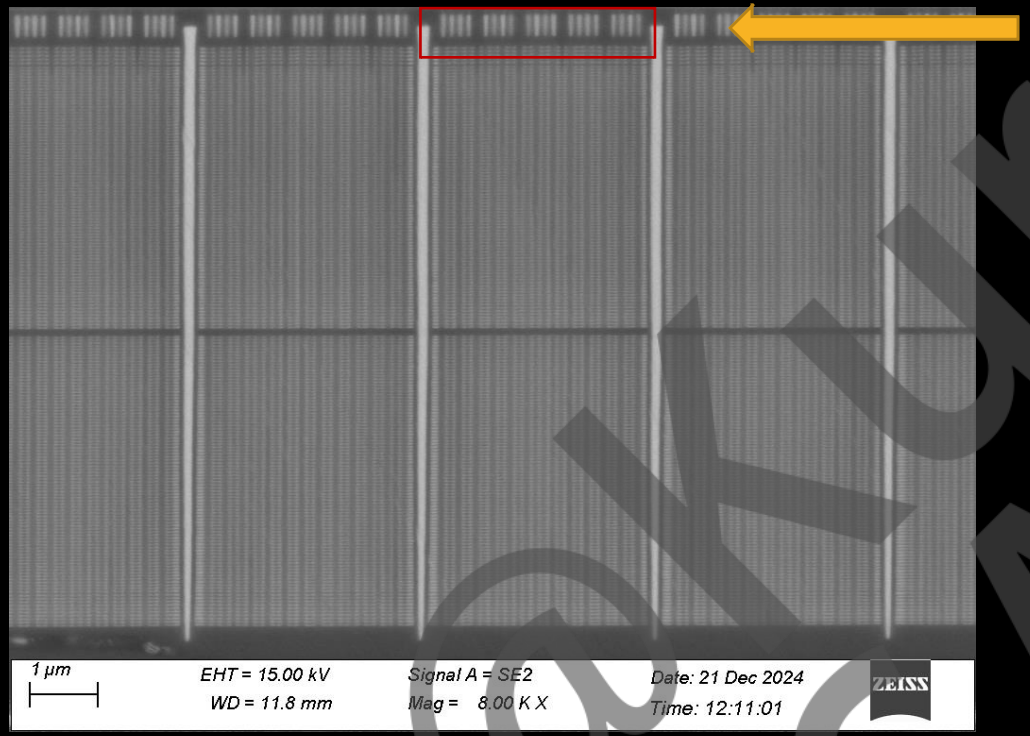
MATE70PRO+ NAND

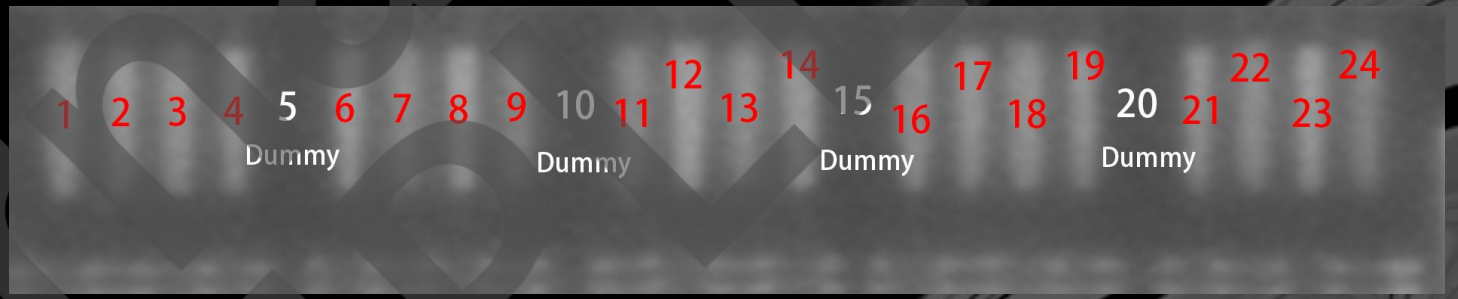


Deck#1 Layers	91(5dummy)
Deck#2 Layers	93
Total Layers	179
Deck#1 Thickness	4.149um
Deck#2 Thickness	4.274um
Total Thickness	8.535um



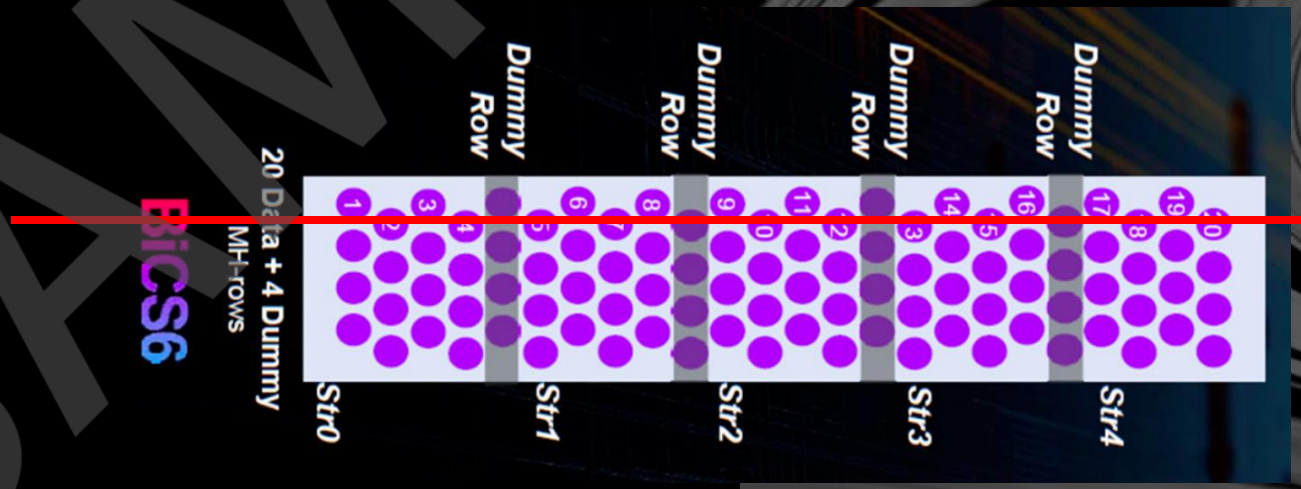
MATE70PRO+ NAND



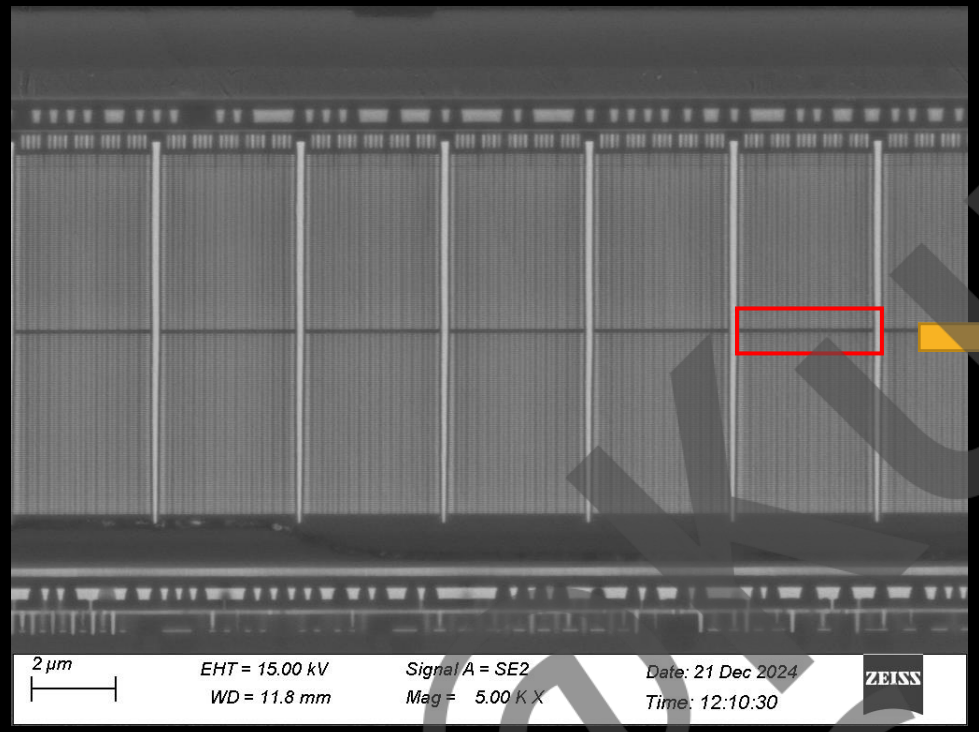


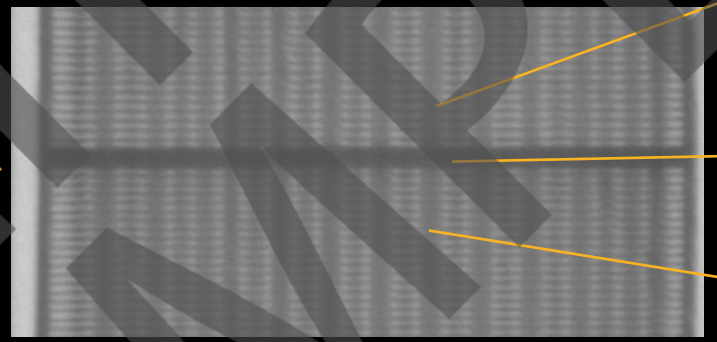
Have 24Pillar

20Pillar+4Dummy Pillar



MATE70PRO+ NAND



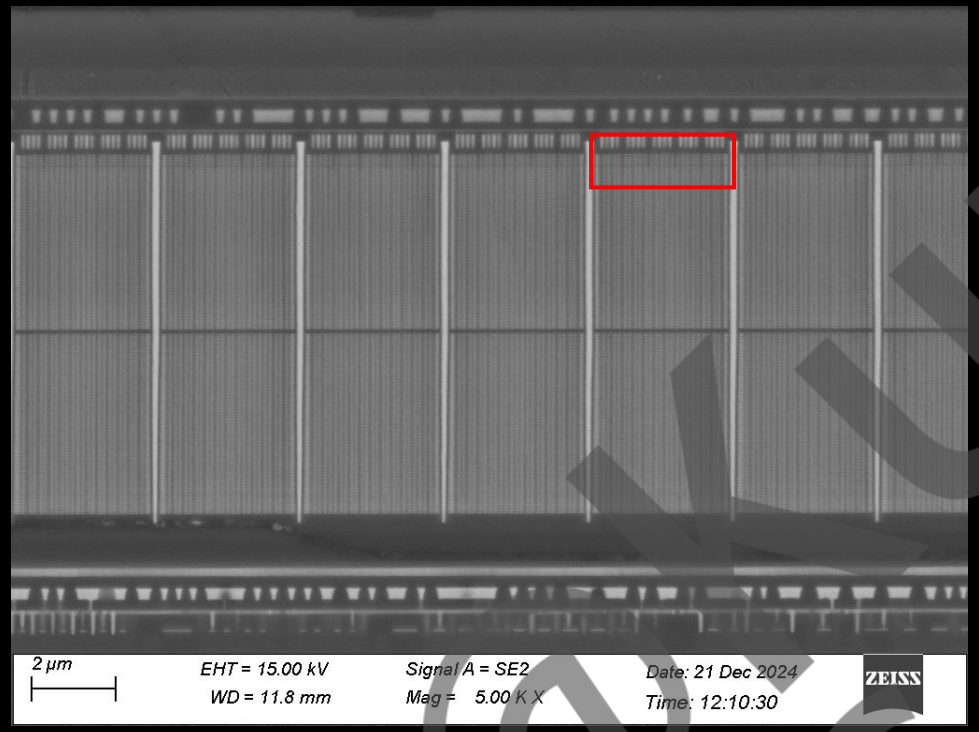


Deck#1 Channel Hole

Seperation of Deck interface

Deck#2 Channel Hole

MATE70PRO+ NAND



MATE70PRO+ NAND

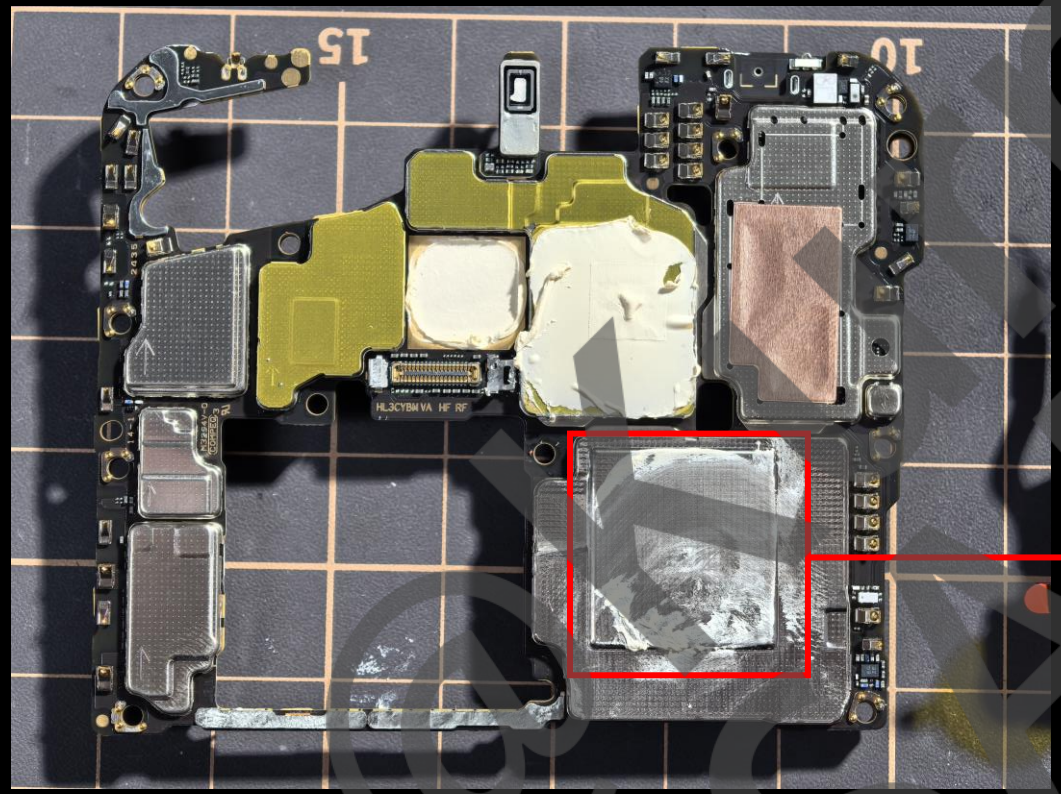
Die Capacity:	512GB/4 128GB
2Deck	
Deck#1 Layers	91(5dummy)
Deck#2 Layers	93
Total Layers	179
Pillar number	24

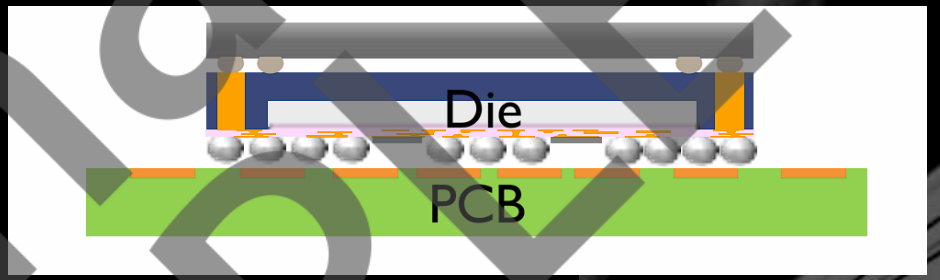
KIOXIA

Maybe it is BiCS6 By Kioxia

MEMORY (LPDDR)

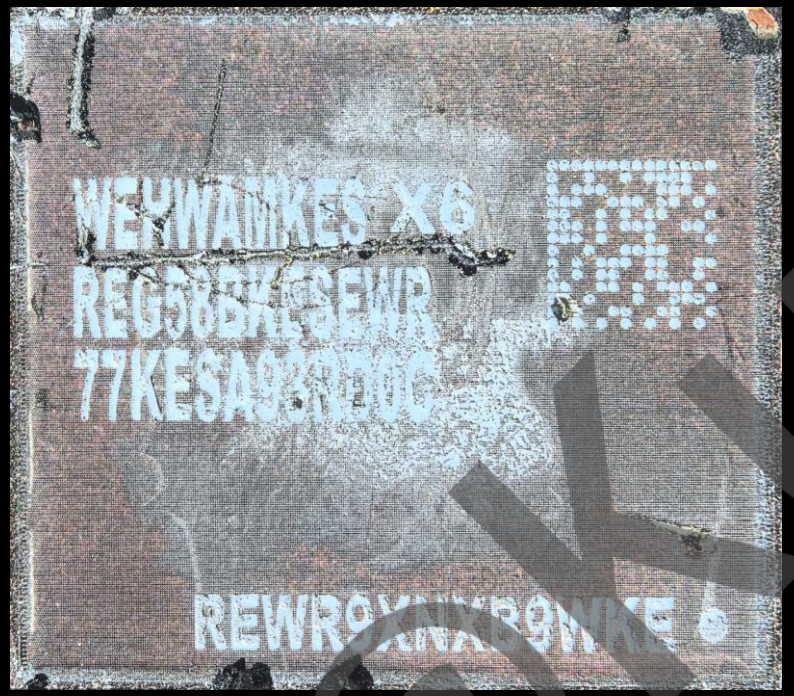
MATE70PRO+ LPDDR





Package on Package

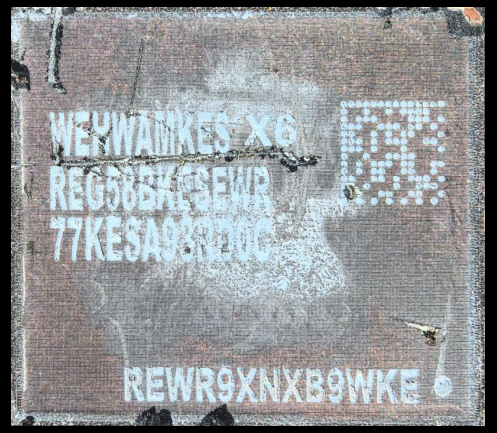
MATE70PRO+ LPDDR



Front

End

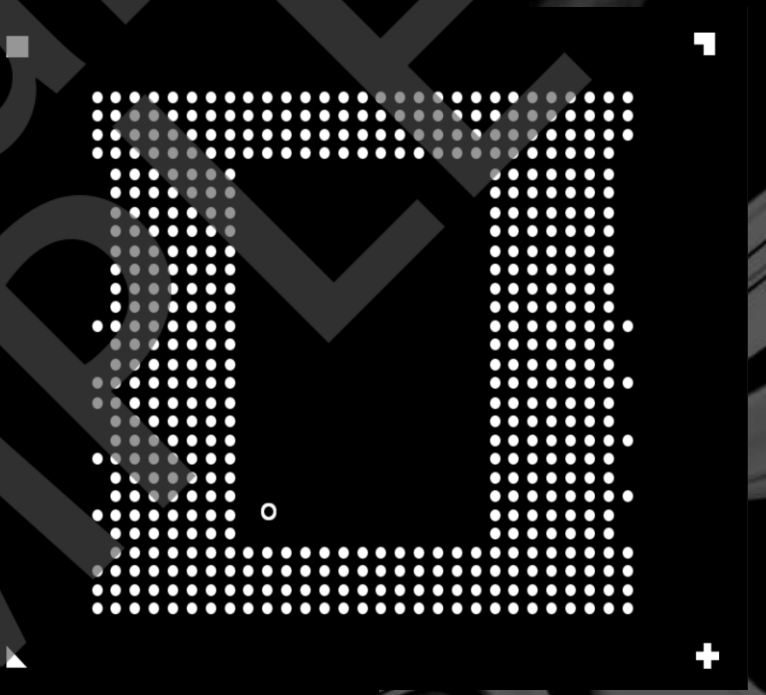
MATE70PRO+ LPDDR



WEHWAMKES X6
REG58BKESEWR
77KESA93ROOC

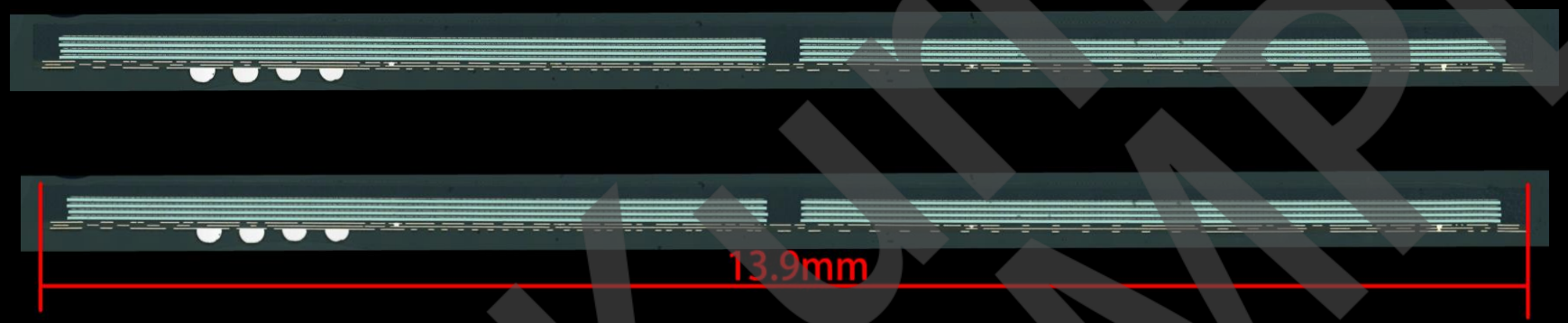
REWR9XNXB9WKE

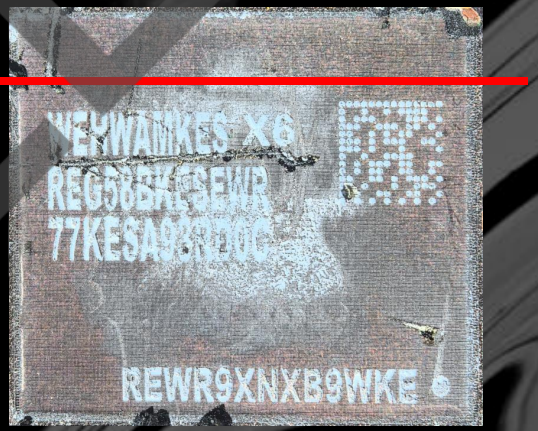
Memory Topmark



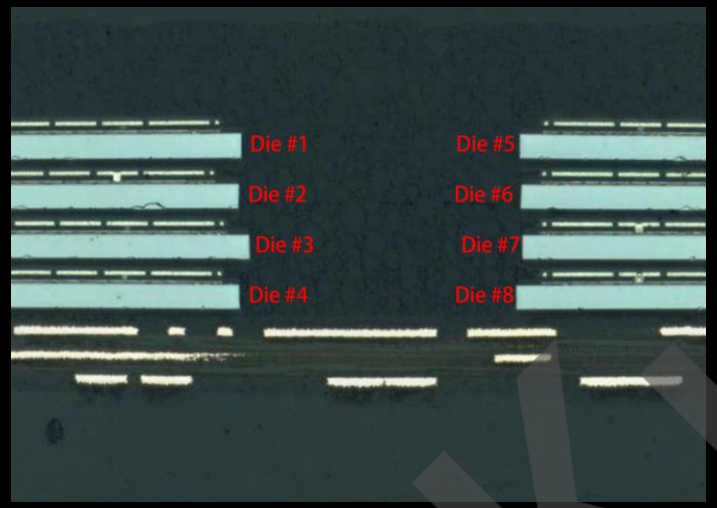
BGA519(BGA496?)

MATE70PRO+ LPDDR

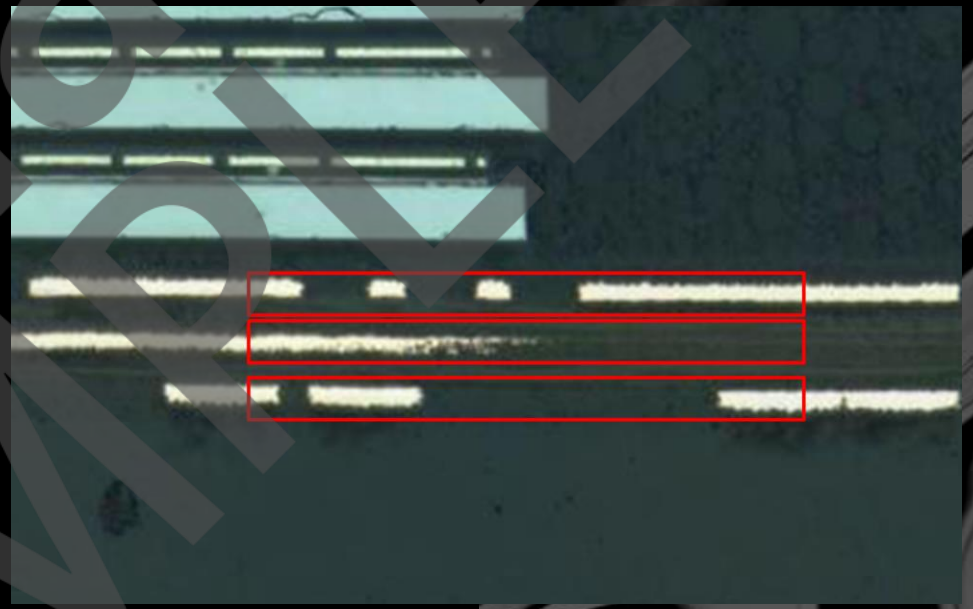




MATE70PRO+ LPDDR

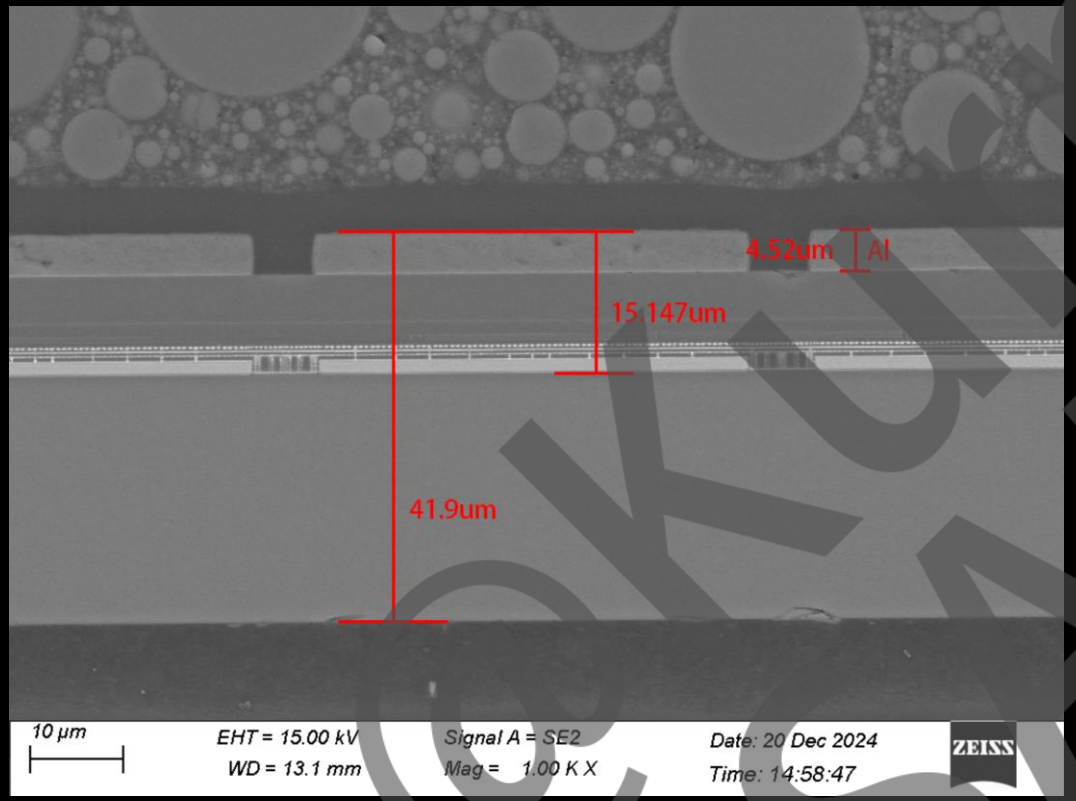


Die num in package: 8 dies
Package capacity: 16GB/128Gb
Die capacity: 2GB/16Gb



Package Sub RDL Number: 3Layers

MATE70PRO+ LPDDR



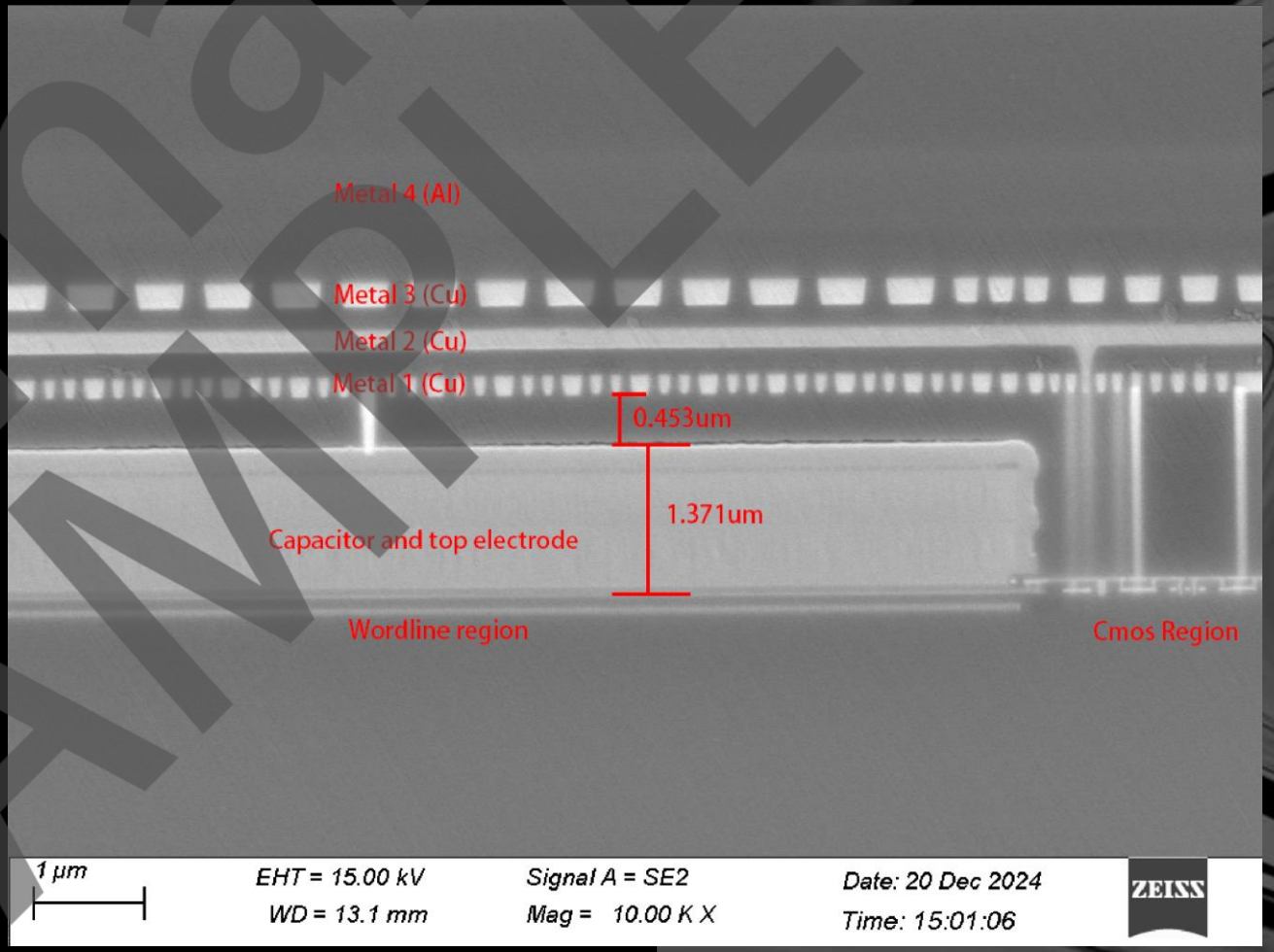
Die Total thickness:	41.9um
Si substrate thickness:	26.753um
Capacitor$Metal layer thickness:	15.147um
Al thick metal thickness	4.52um

MATE70PRO+ LPDDR

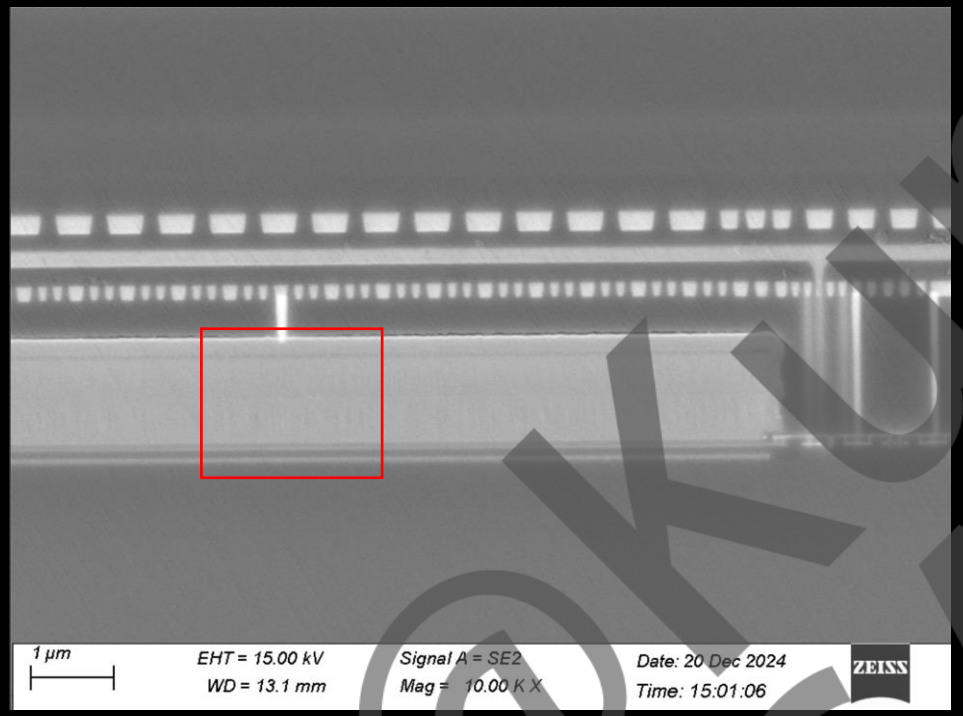
CMOS transistors and Capacitor are formed
At the base of the silicon substrate

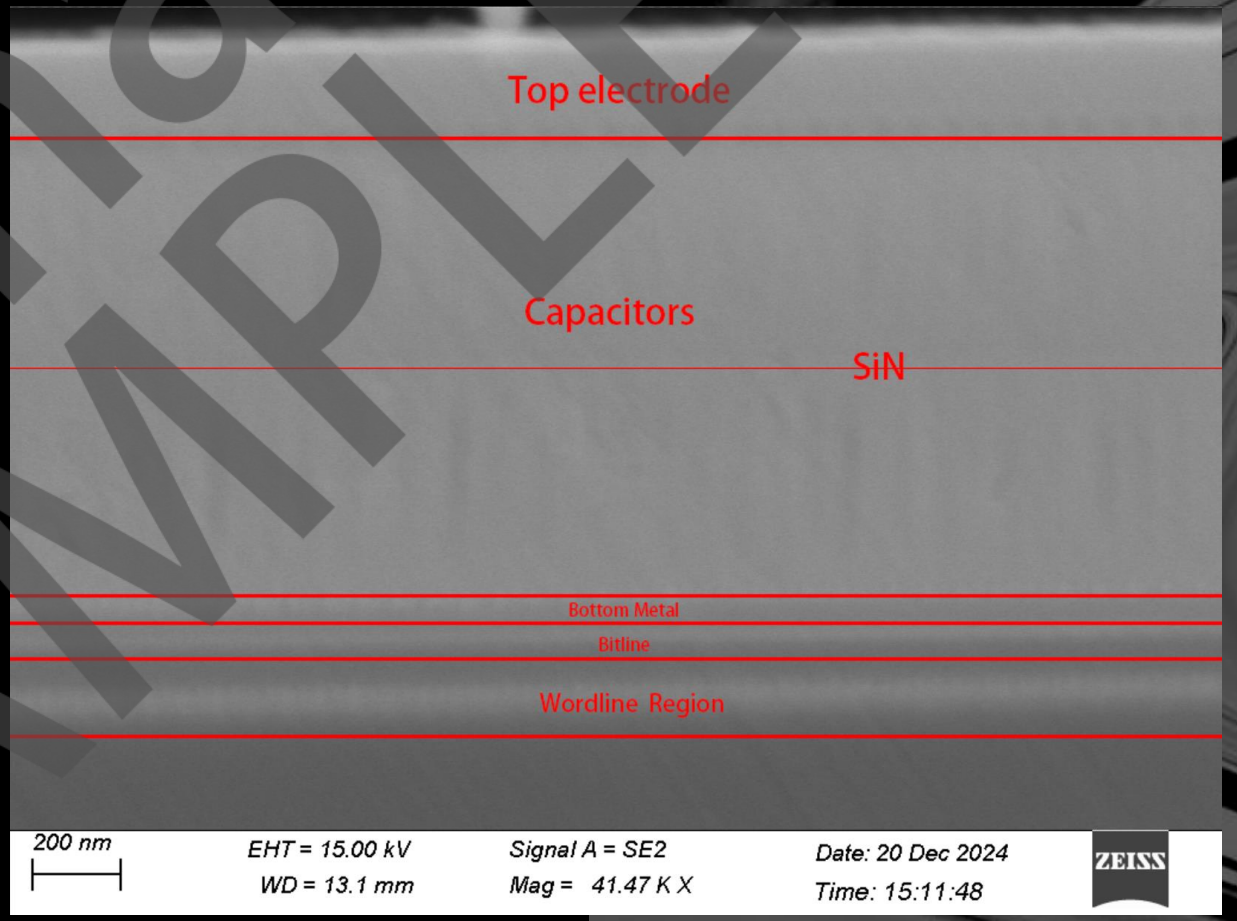
Below the capacitors there is a wordline region

And have 4 Metal layers



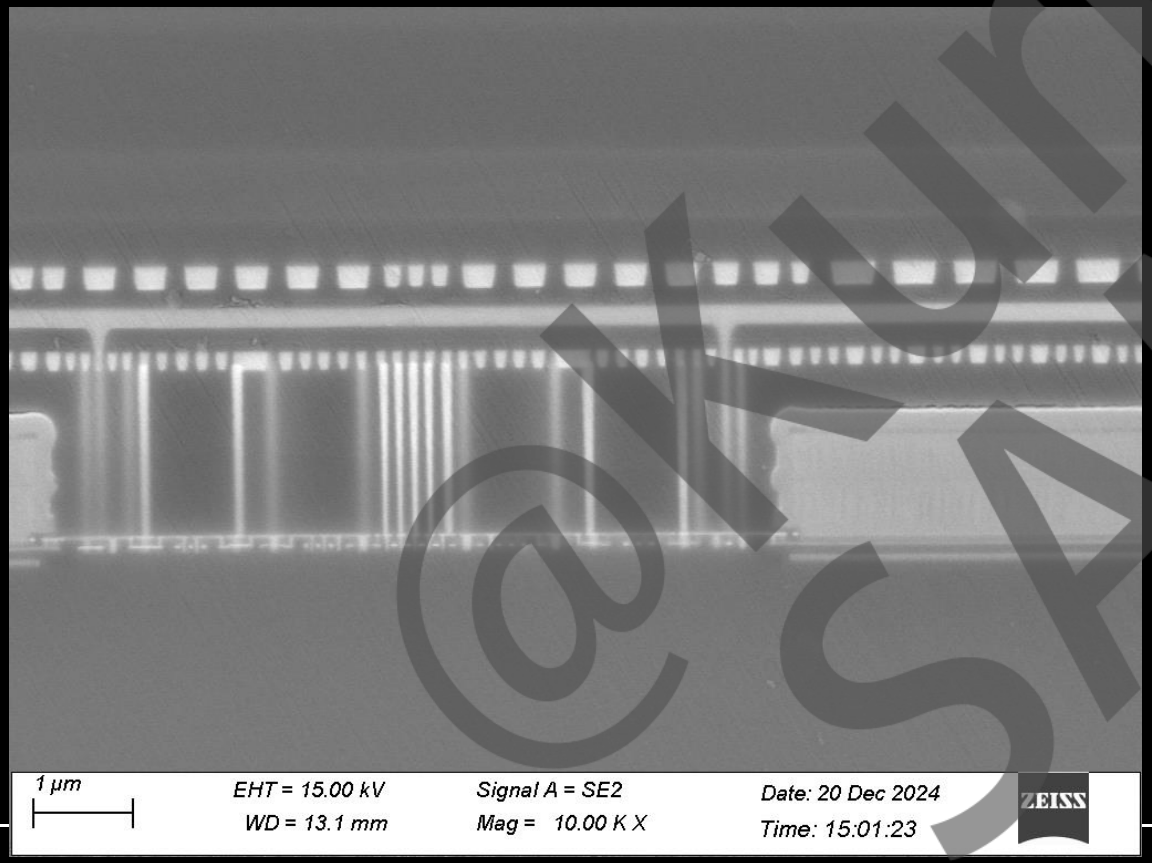
MATE70PRO+ LPDDR





MATE70PRO+ LPDDR

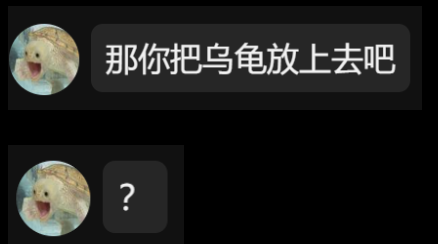
Unable to analyze, too little data
But according to the empirical formula,
this is a bit like Micron's Lpddr5/x



END

Thanks By @英短咕咕咕
Providing funds and products

Thanks By @FlowRay
Provide some technical support



Thanks