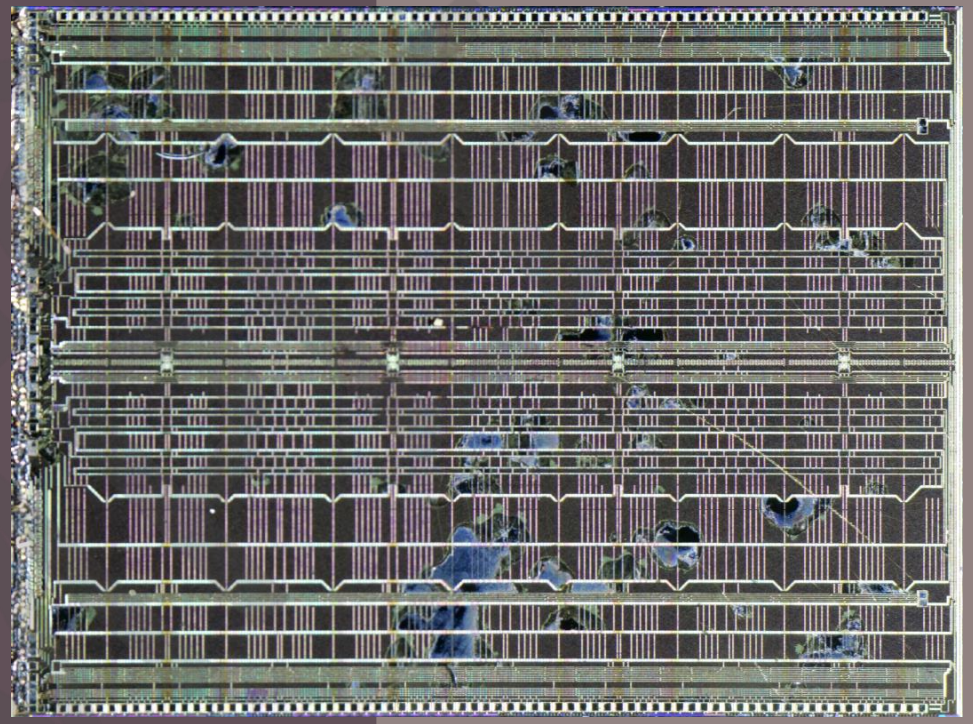
Micron 24GB Lpddr5 memory



Total analyze

V1

@Kurnal

Verison of this Report

Version	Date	Updates	Anthor
V0	2025/03/26 18:47	Doing	Kurnal
V1(Over)	2025/03/27 05:02	Over data	Kurnal
1-B站工坊			

About Anthors

This Report made by @Kurnal

BiliBili: @Kurnal
X: @Kurnal
WeChat: @KurnalWeChat

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Physical Analyze

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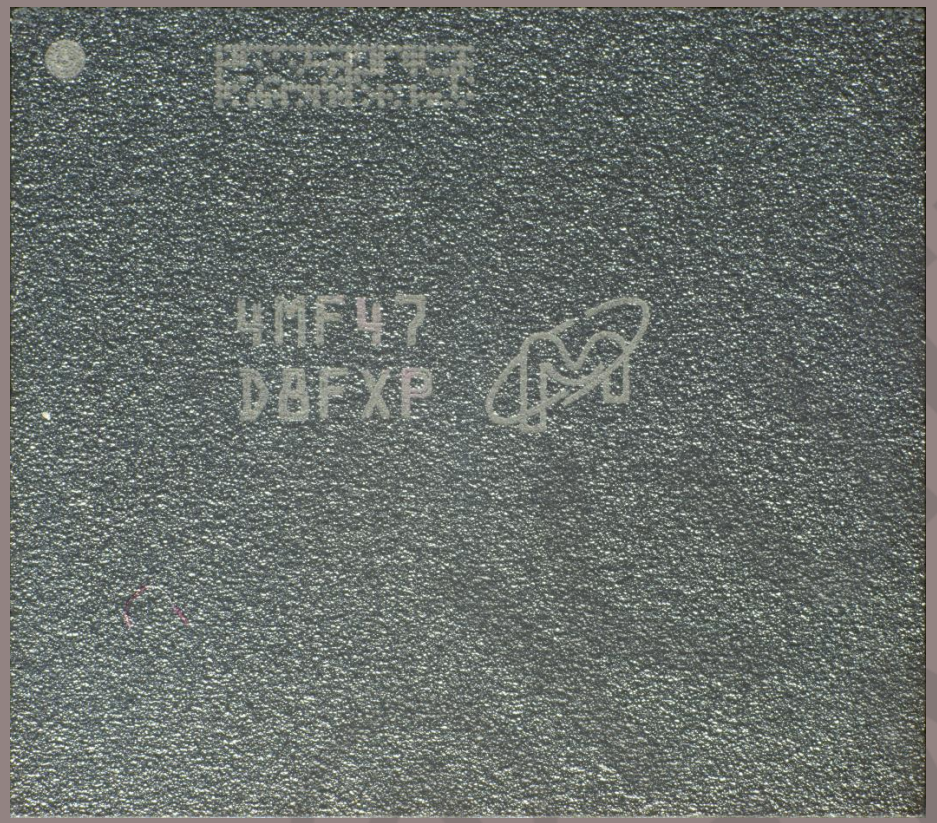
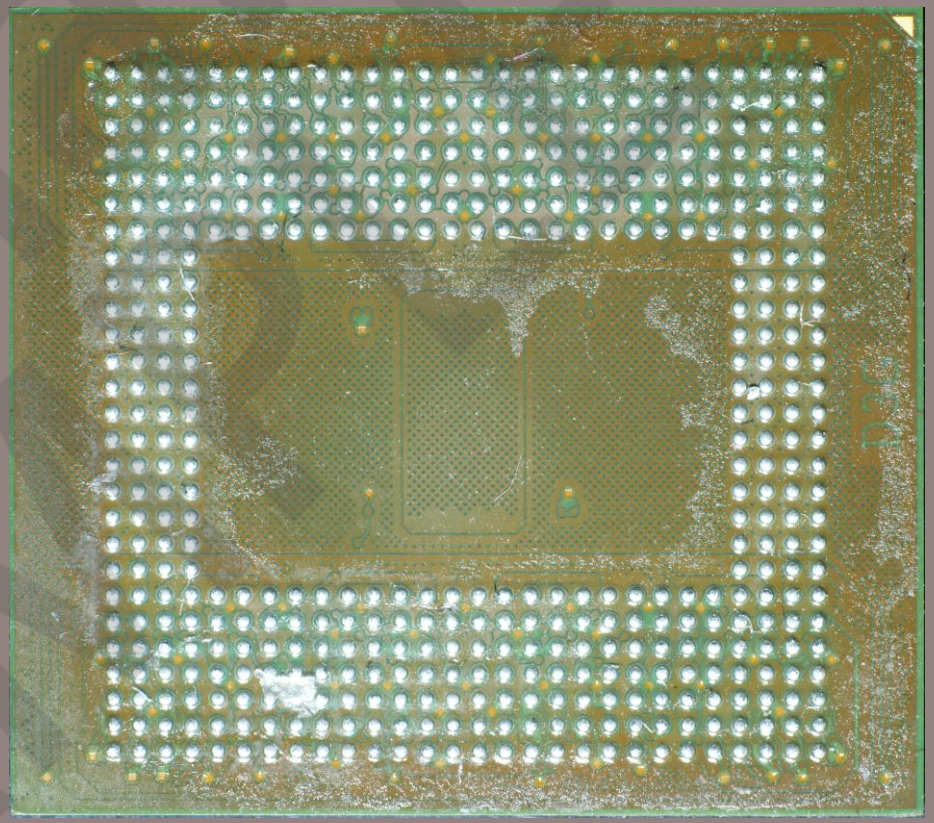
Package analyze

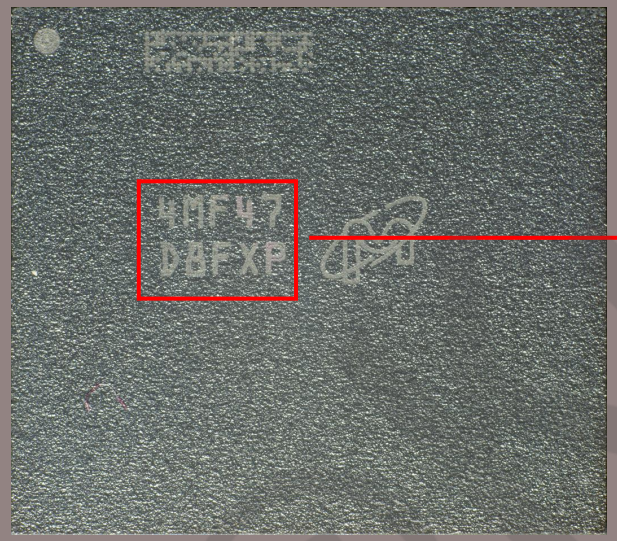


Package Top View



Package Bottom View

Diemark



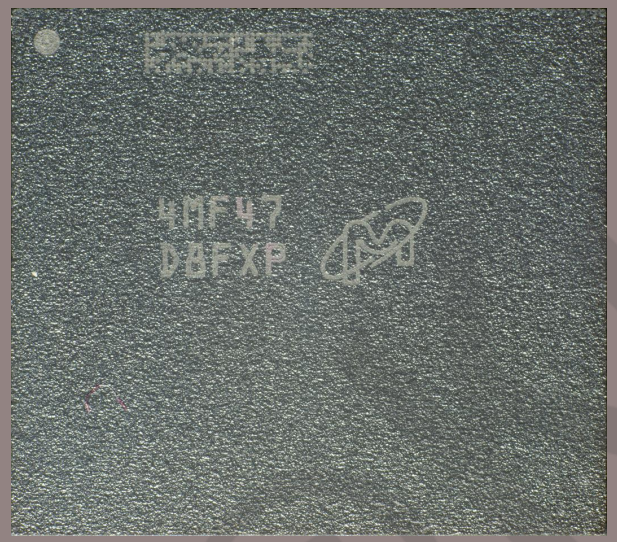
Package Top View

Package Top Mark

D8FXP
Micron Mark decode
MT62F3G64DBFH-020 WT:F

Diemark

LPDDR5 192Gbit @4800Mhz



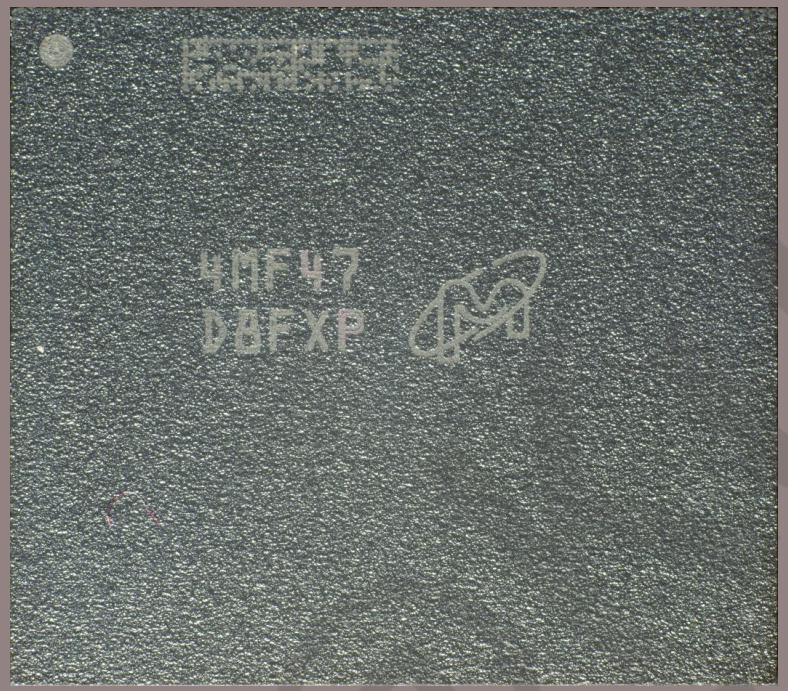
Package Top View

Specifications

Component Density 192Gb	Speed 4800MHz	MT/s 9600MTPS	I/O Voltage 0.5 VOLTS	Operating Temp -25C to +85C	Bus Width x64
CAS Latency CL = Programmable	Pin Count 496-ball	Part Status Code Production	Component Config 3G x64	Dry Pack Qty 1190	Package Dimension (W x L x H) mm 14.00 x 12.40 x 0.81
Tape & Reel Qty 2500	Package Type GREEN	Number of Components 12	Package VFBGA	Family DRAM	Technology LPDDR5

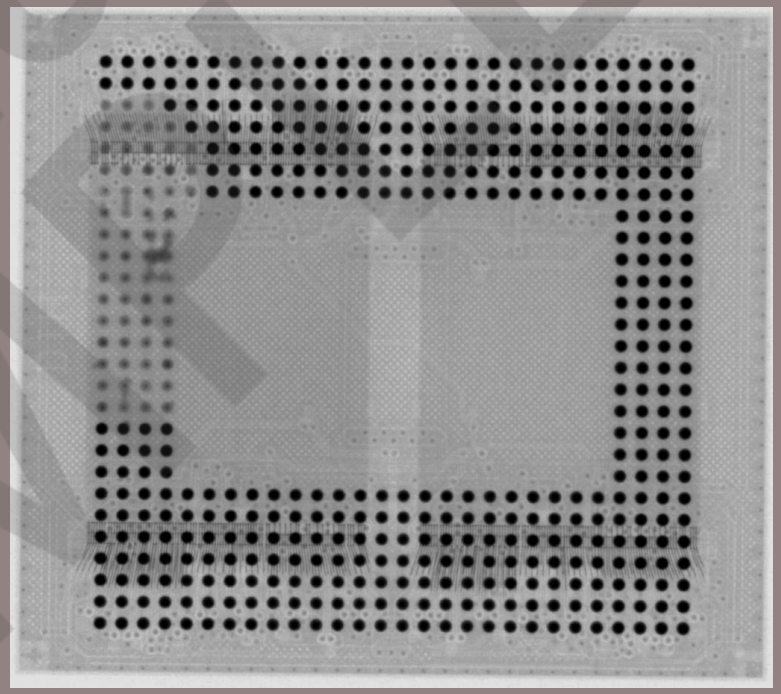
Package: BGA496
Dimensions: 14x12.4x0.8mm
Surface size: 173.6mm2
Bump Pitch: 0.4mm

Package-Xray



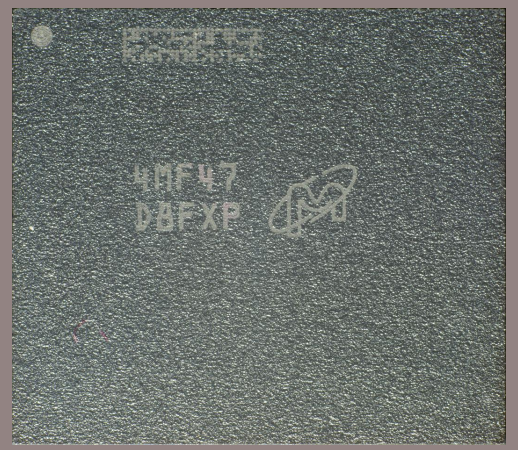
Package Top View

X-Ray

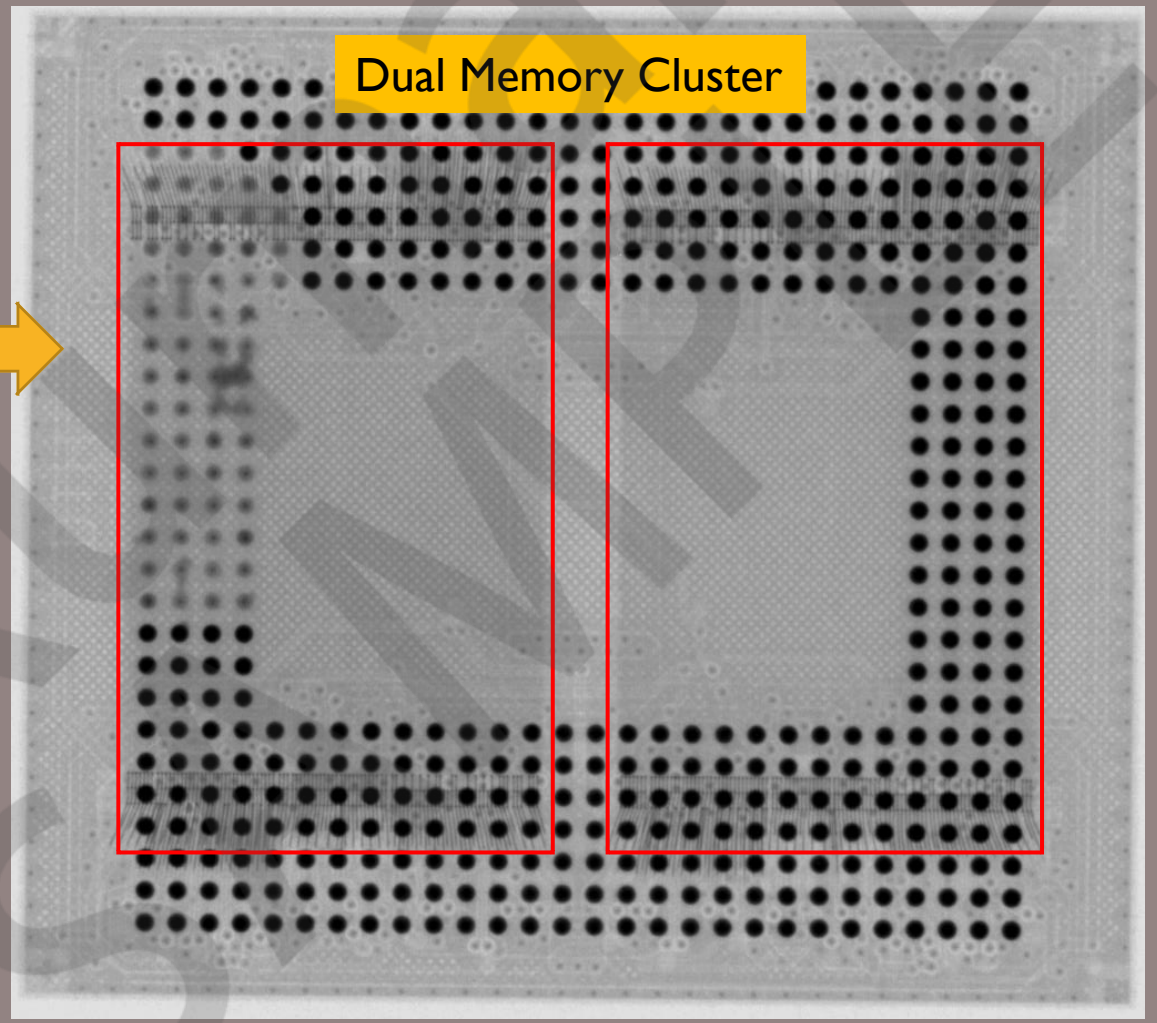


Package Xray photo

Package-Xray

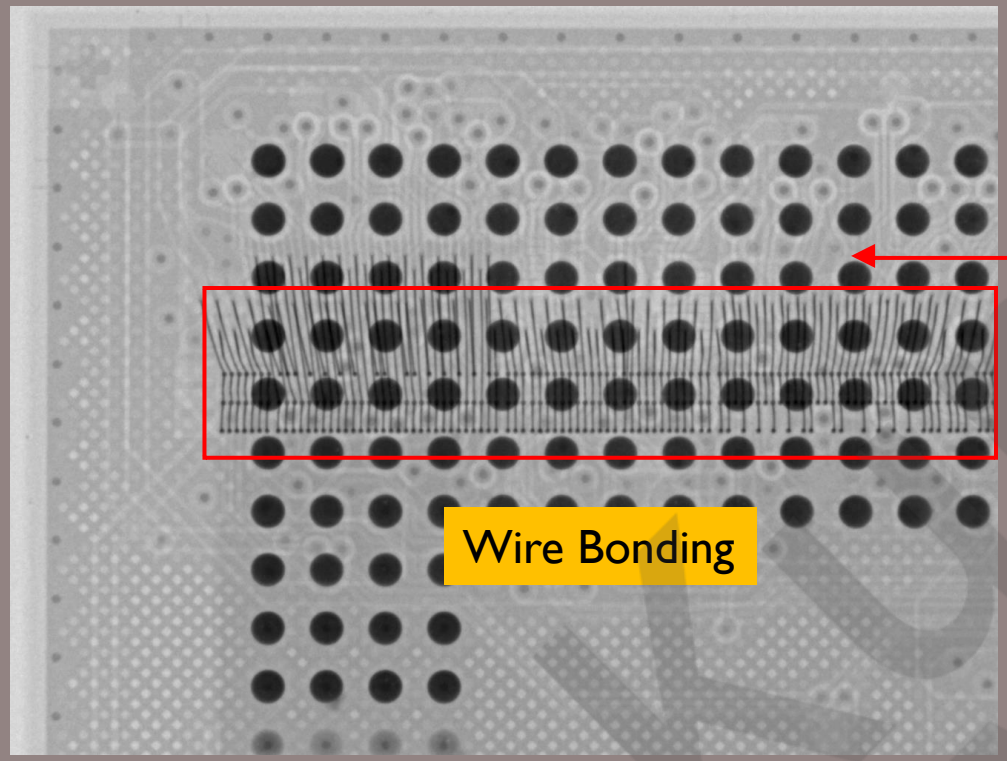


Package Top View

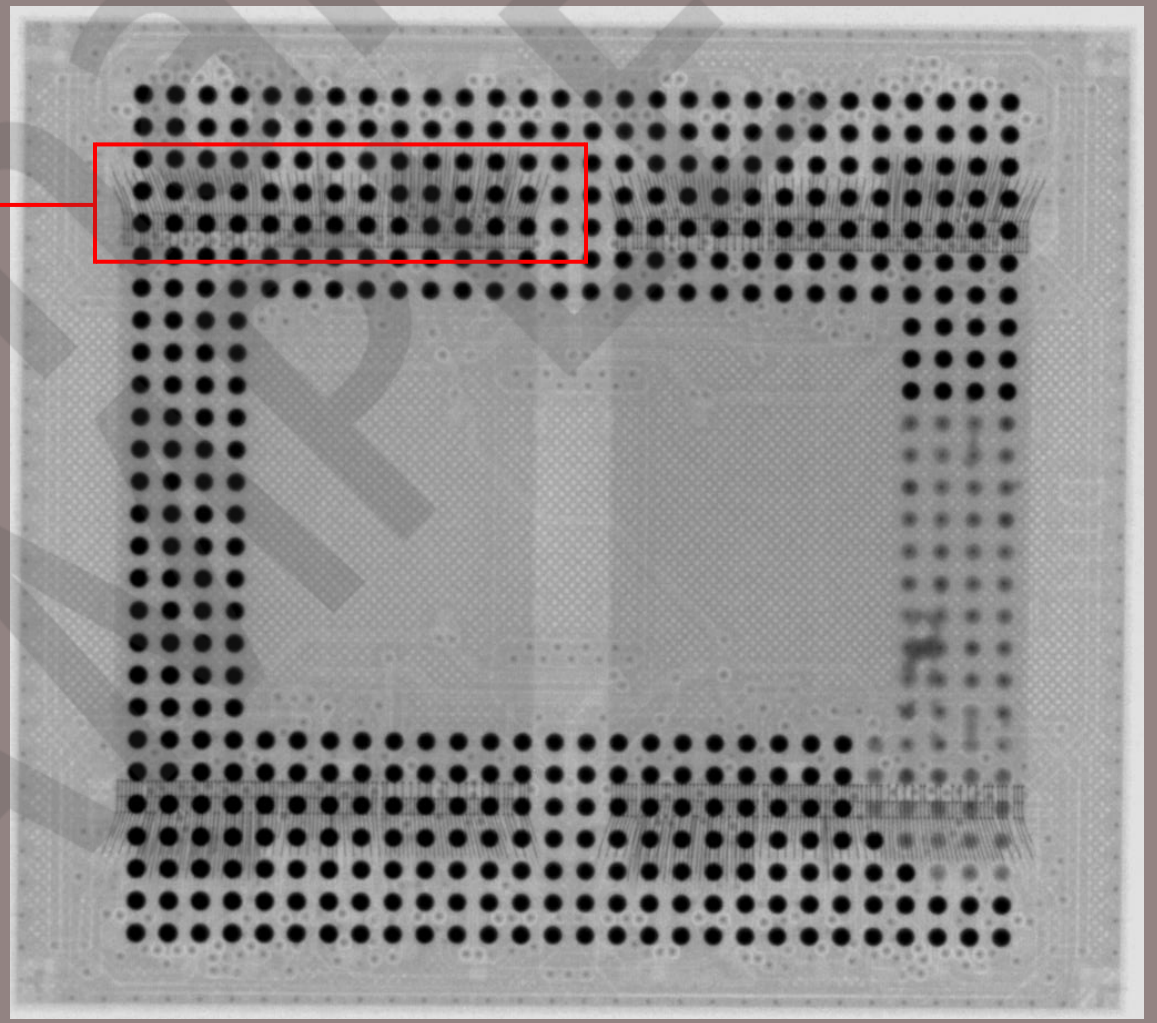


Package Xray photo

Package-Xray

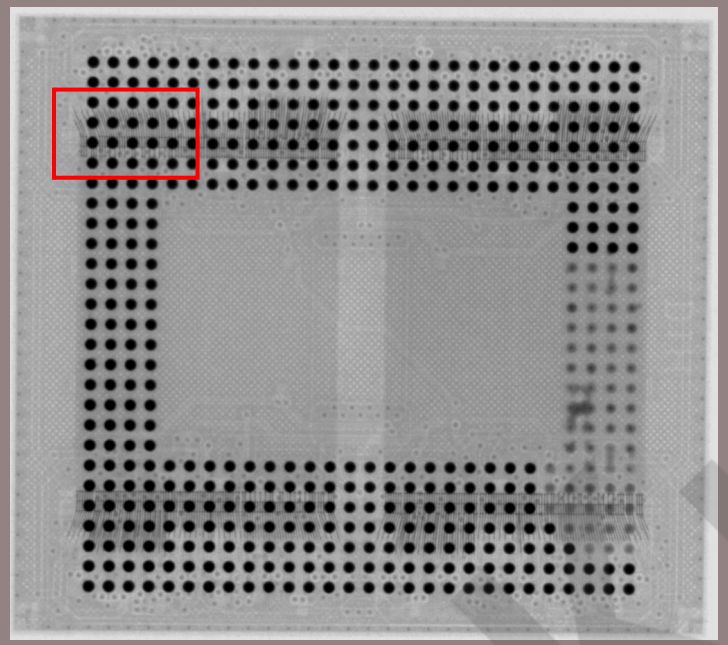


Package Xray corner



Package Xray photo

Package-Xray



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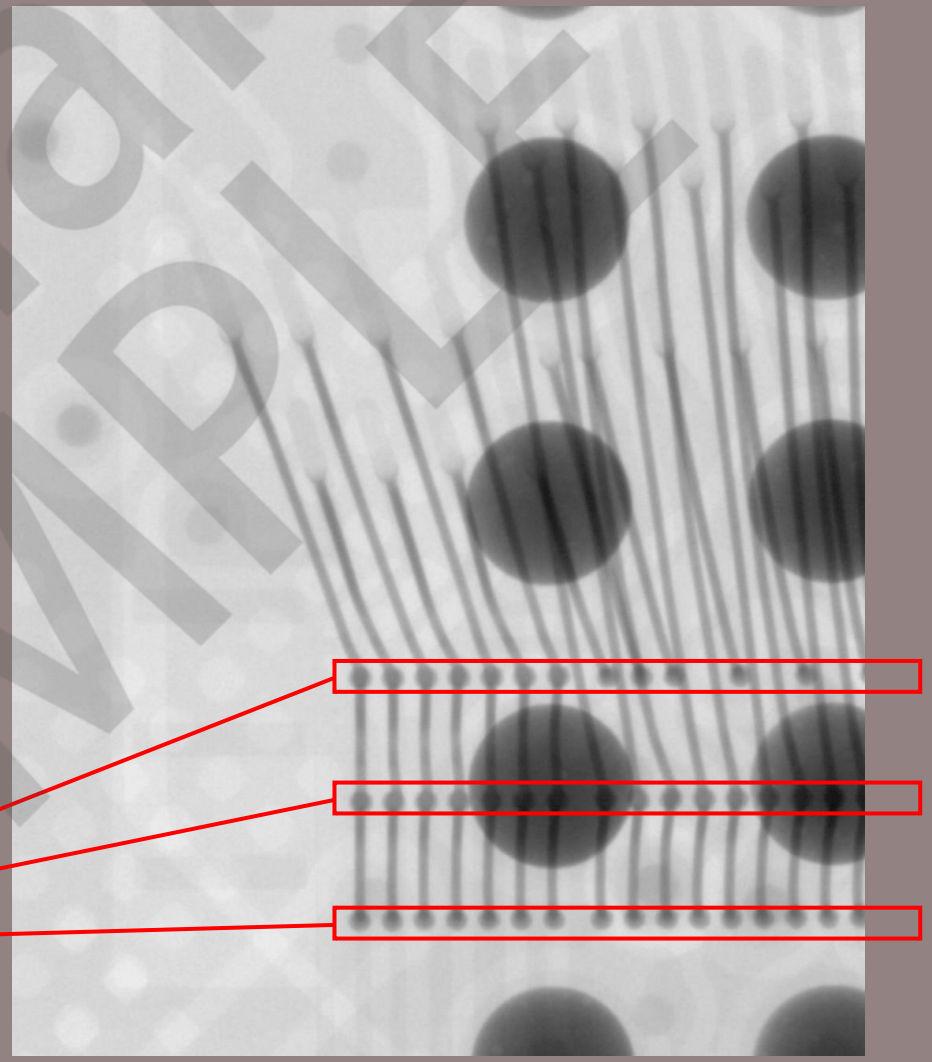
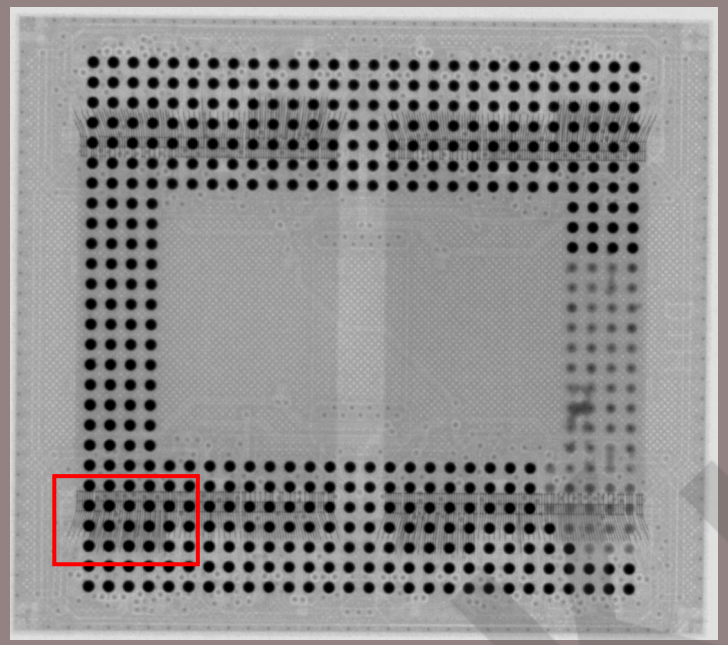


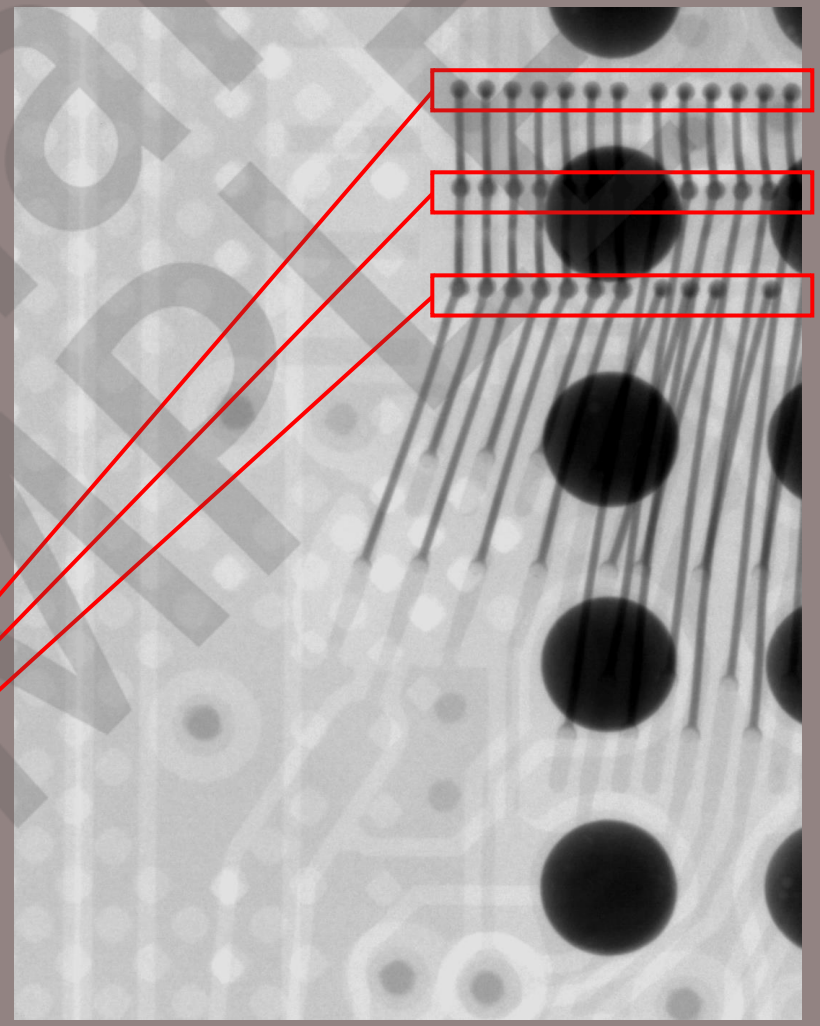
Package Xray corner

On the xray photo with Above
Have 3 layers bonding pad

Package-Xray



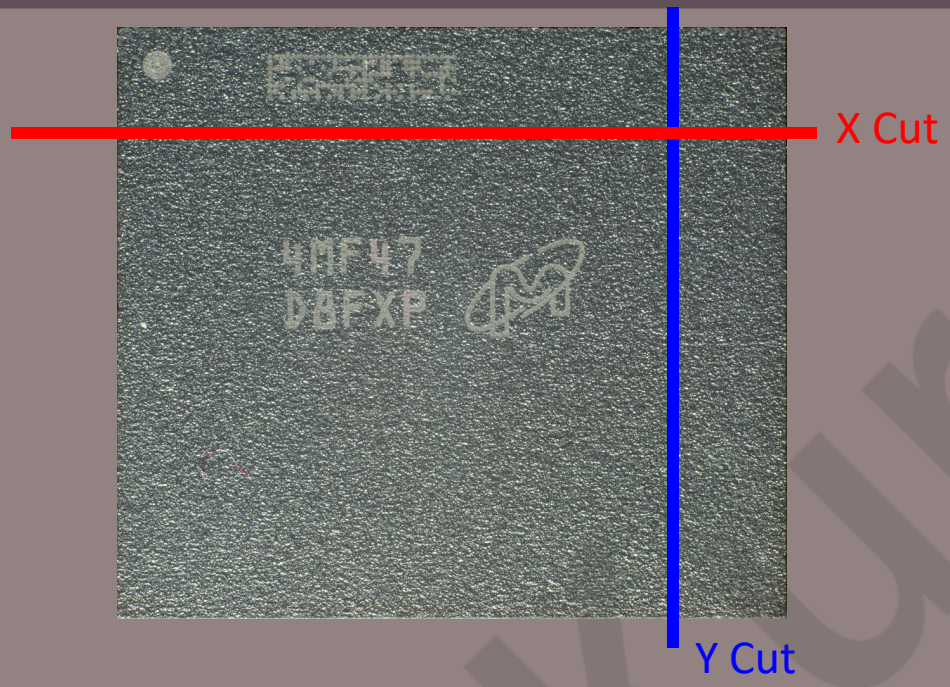
Package Xray photo

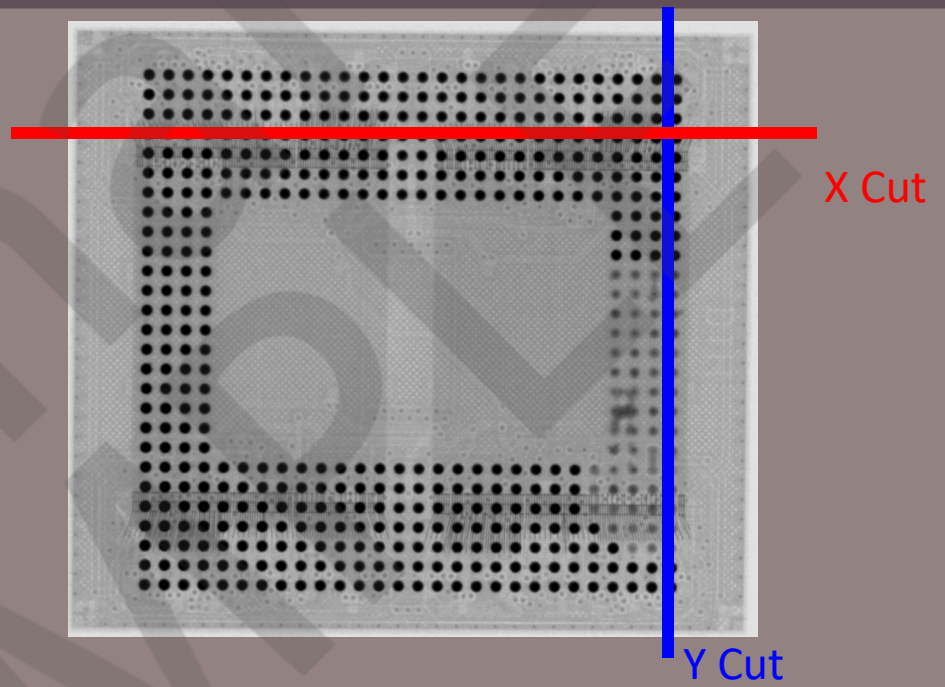


Package Xray corner

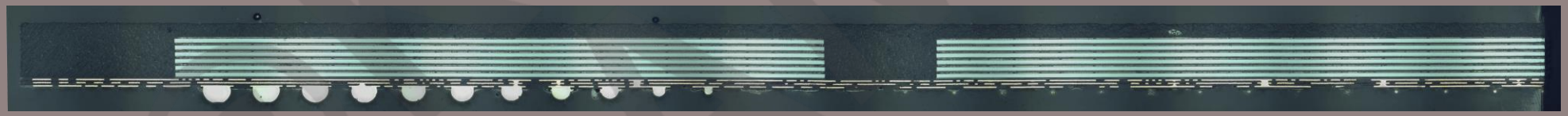
On the xray photo with below
Have 3 layers bonding pad

Package-Cross Section





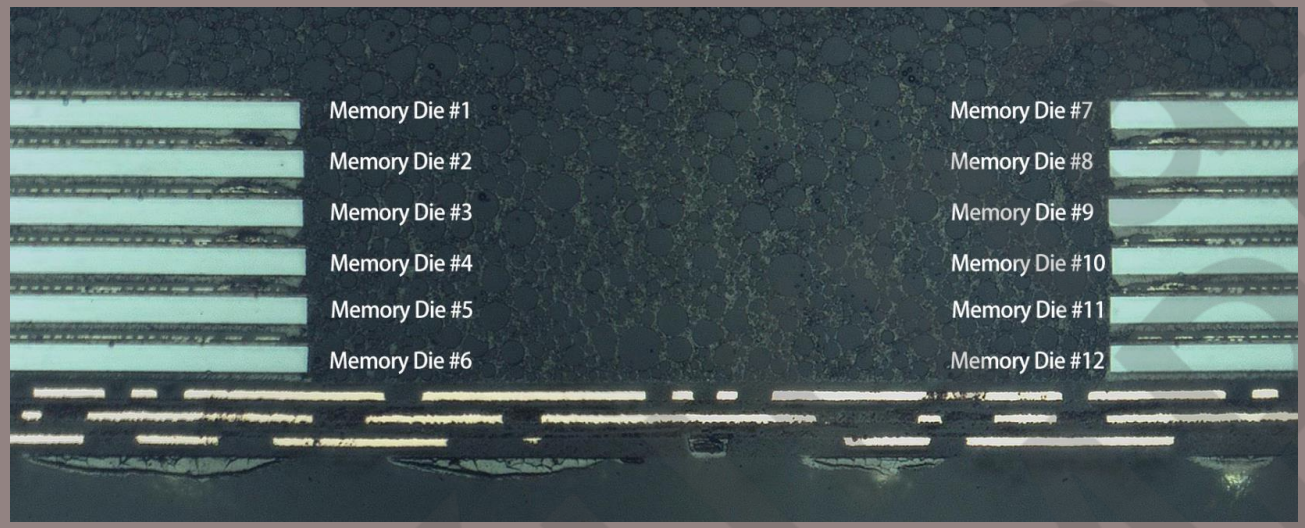
X Cut



Y Cut

Package-Cross Section

X Cut



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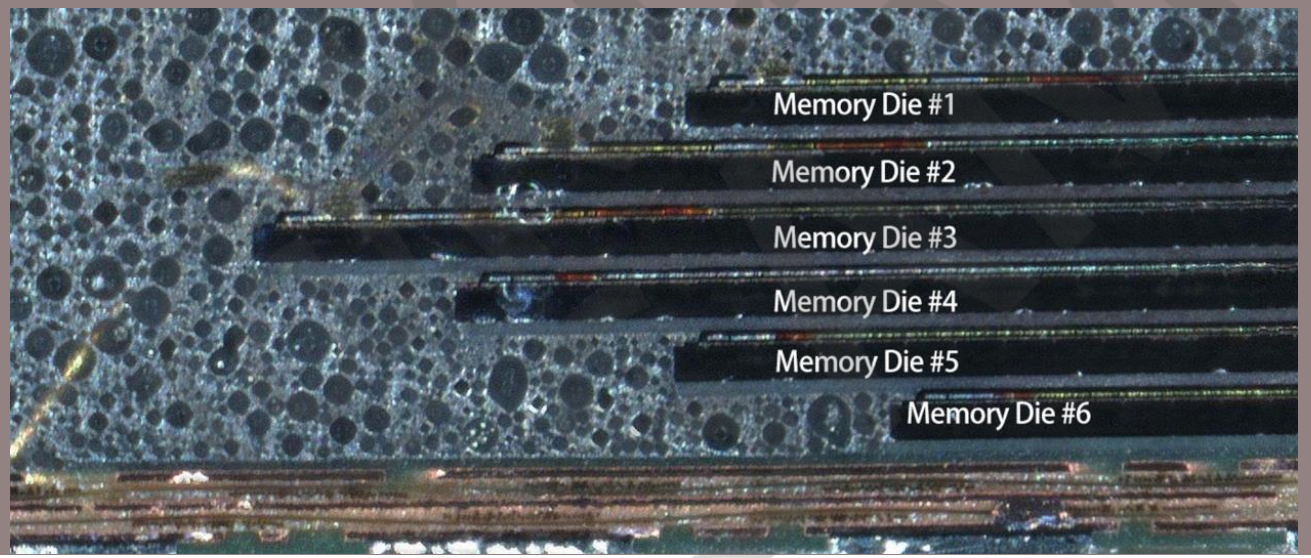
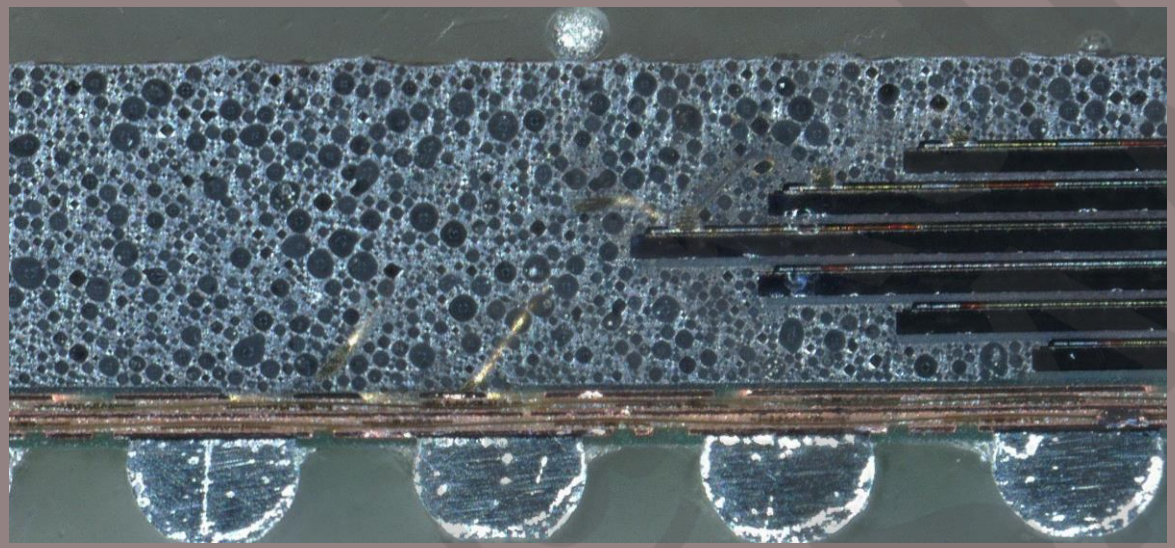


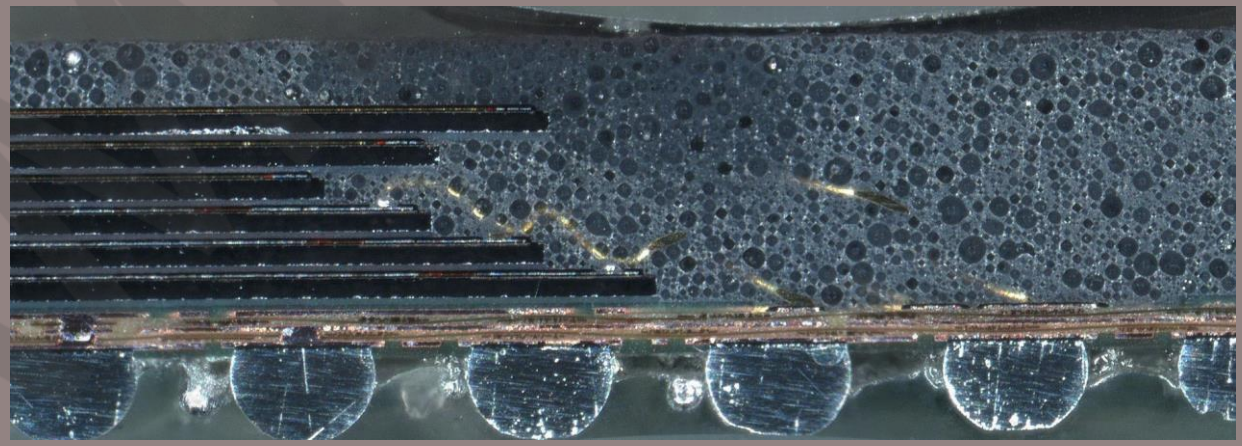
On package have 12 DRAM dies

Package capacity: 24GB/192Gb
Die capacity: 16Gb/die

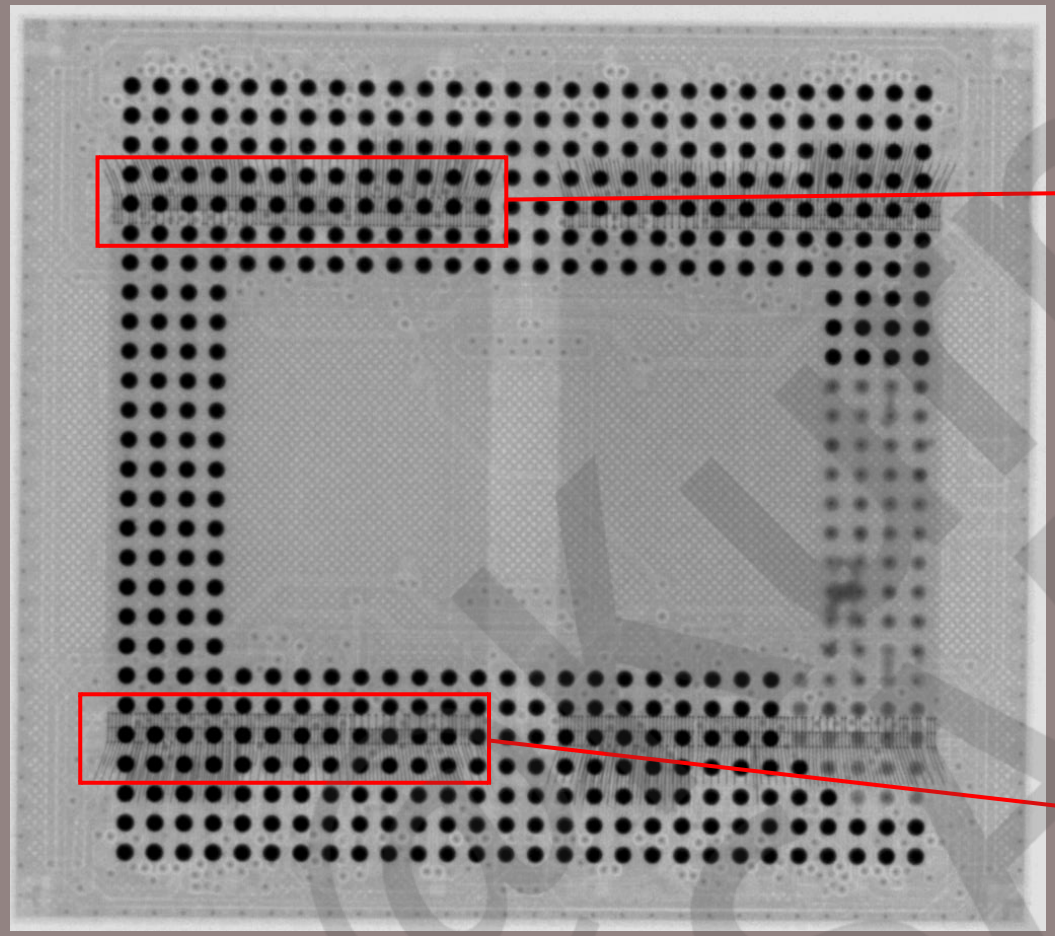
Package-Cross Section

Y Cut

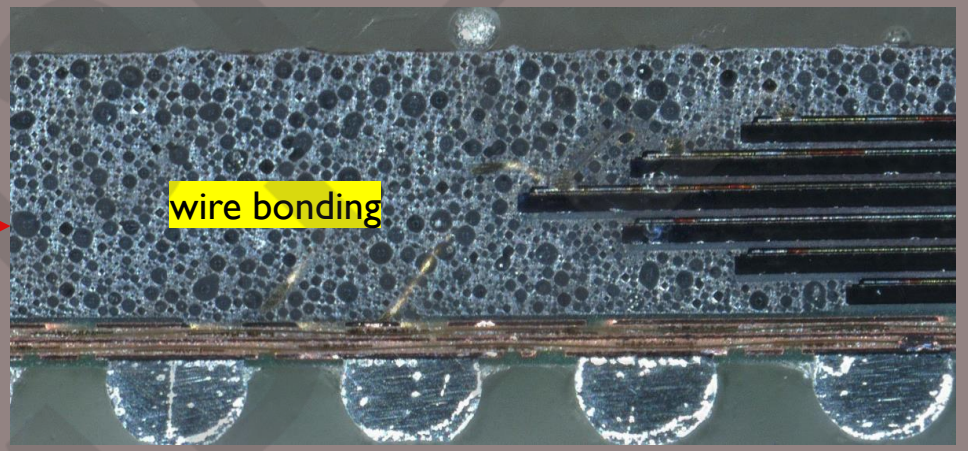




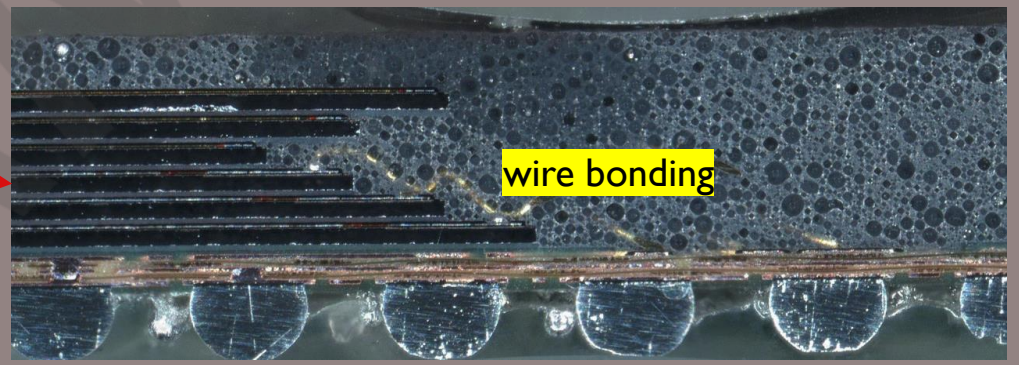
Package-Cross Section



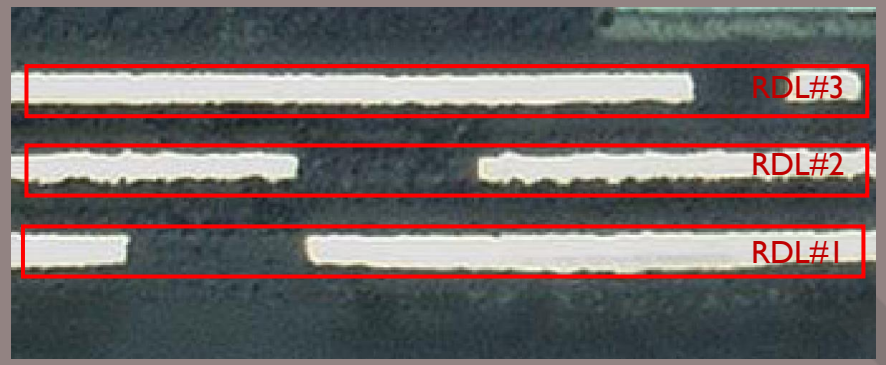
Package Xray photo

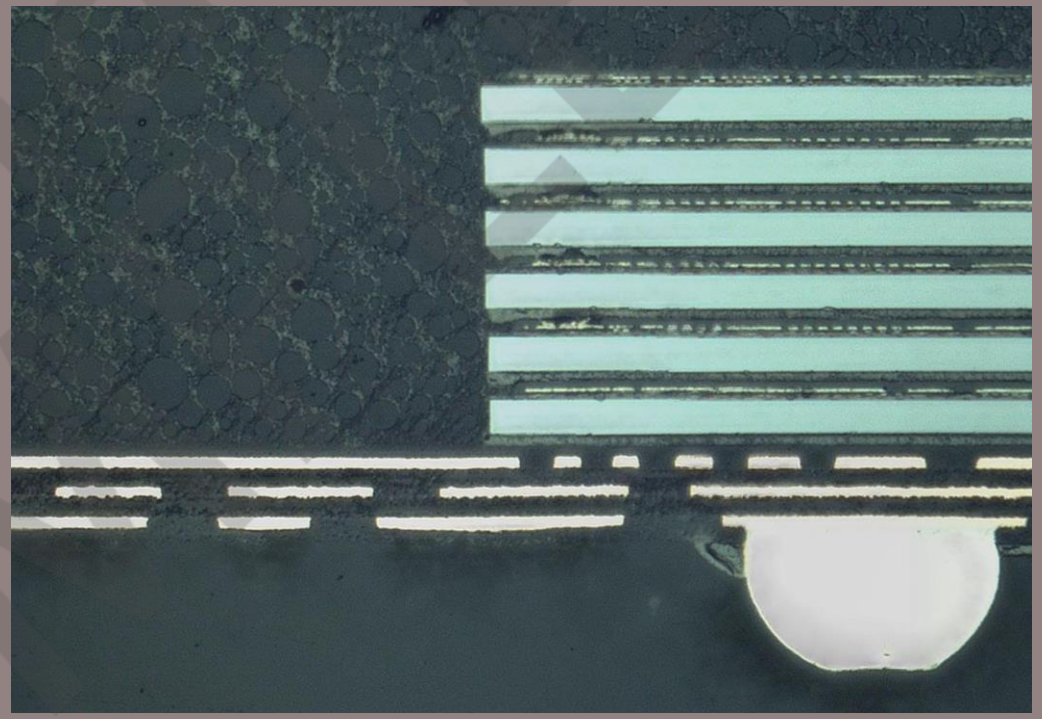


On the 1 clusterbonding layers
Use 3+3 Layers wire bonding



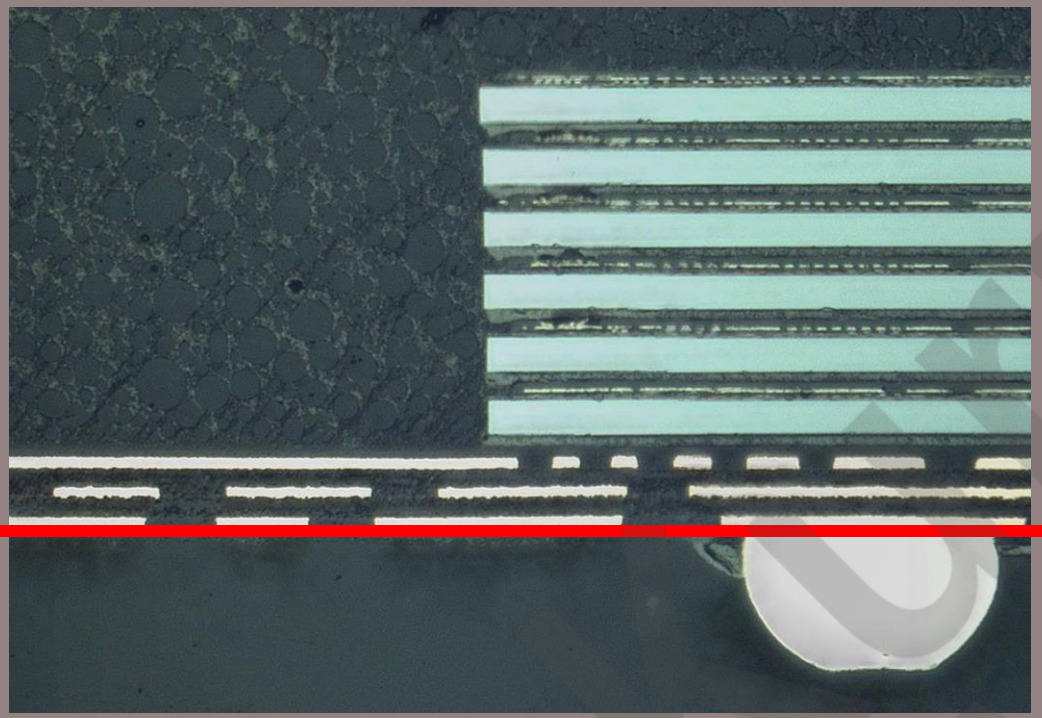
Package-Cross Section-RDL





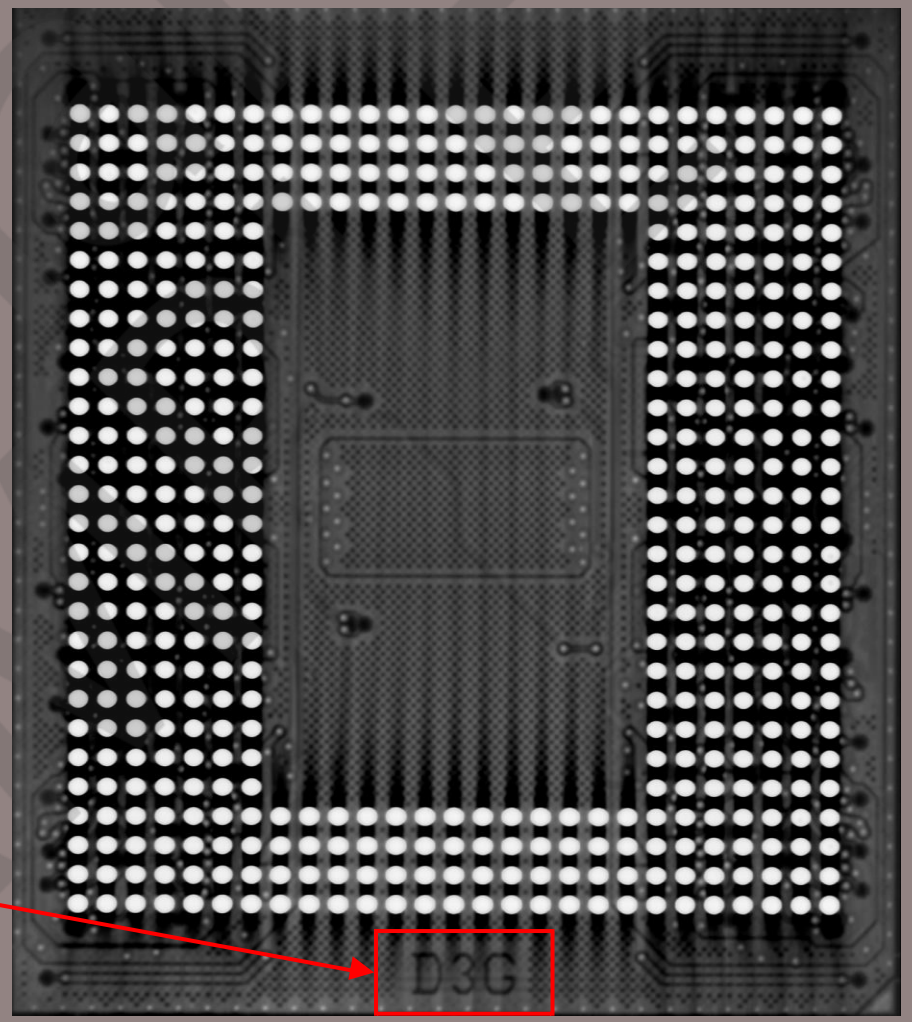
Package RDL number: 3Layers

Package-Cross Section-RDL



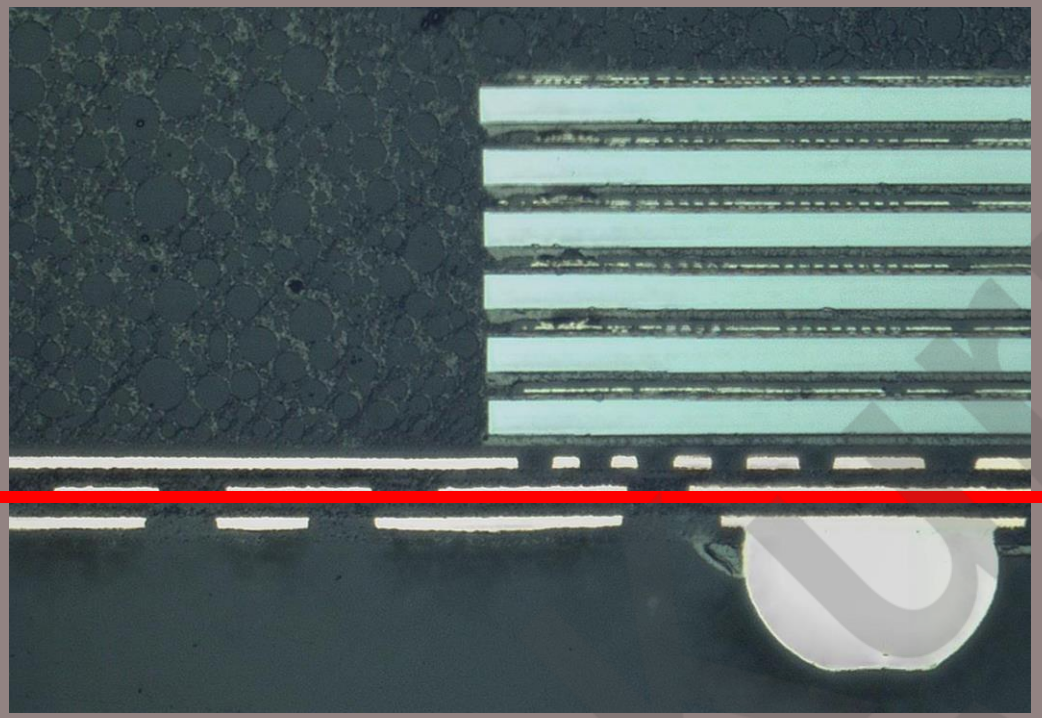
RDL#1 Layers

Package mark:D3G

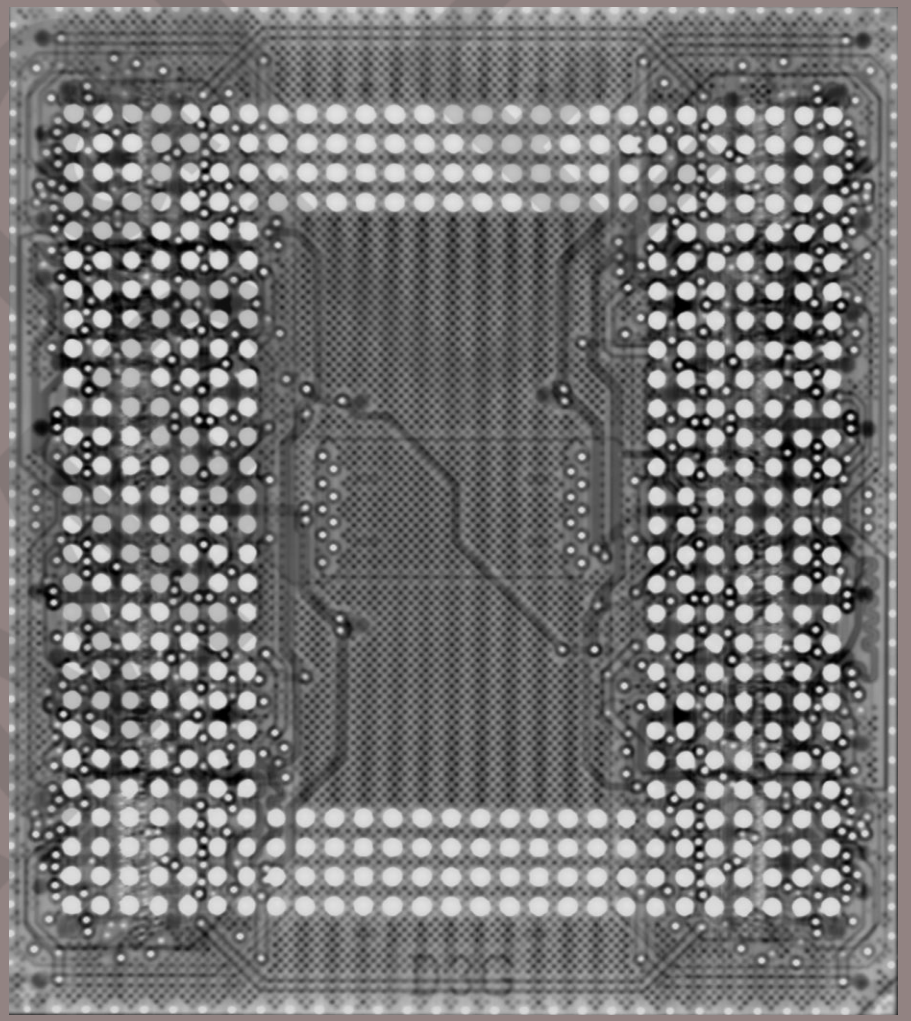


RDL#1 Layers

Package-Cross Section-RDL

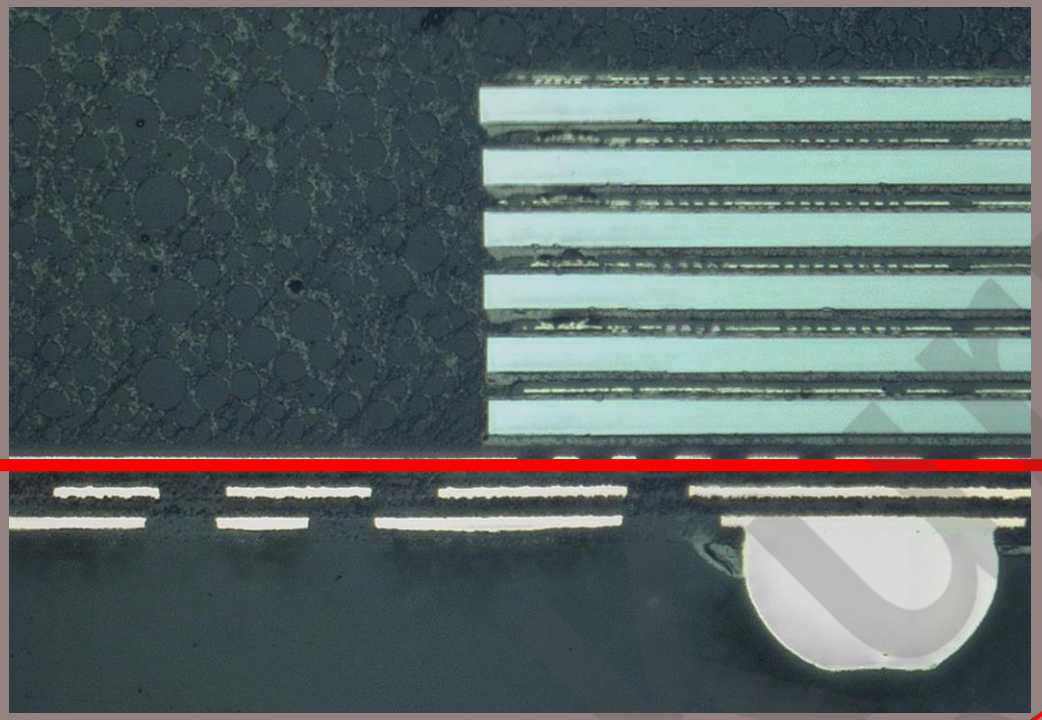


RDL# Layers



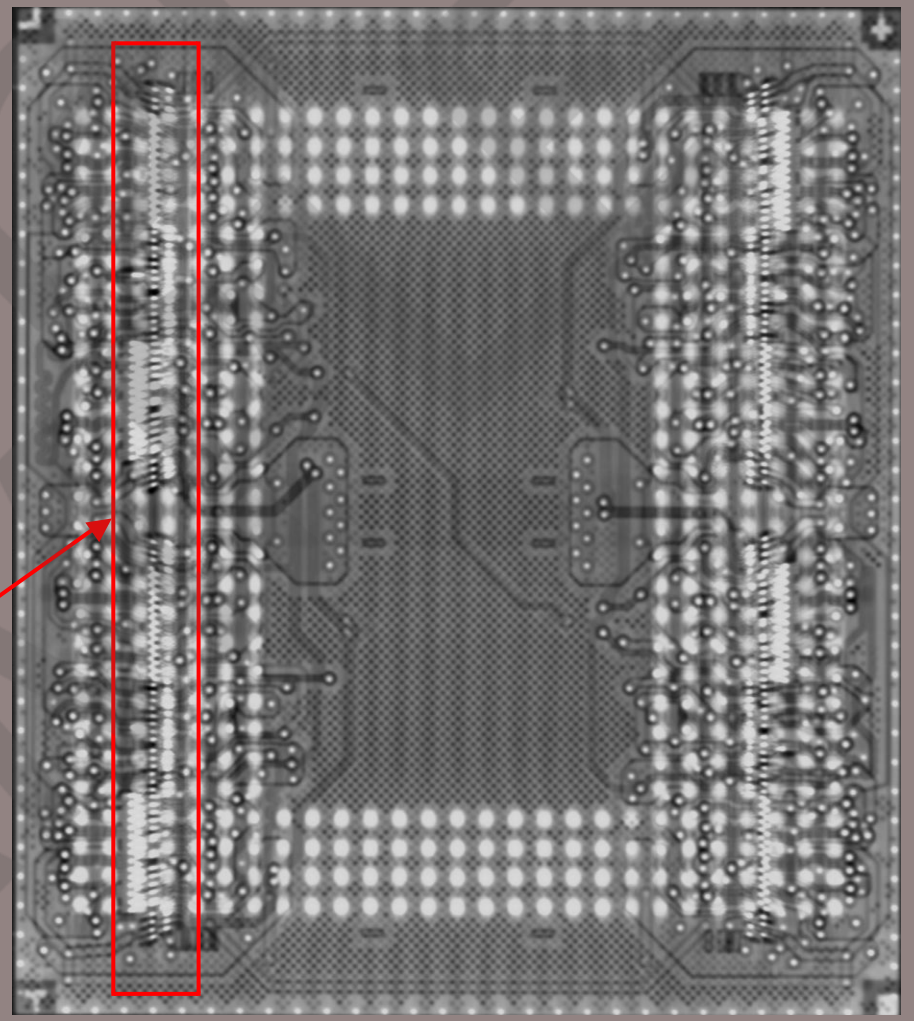
RDL#2 Layers

Package-Cross Section-RDL



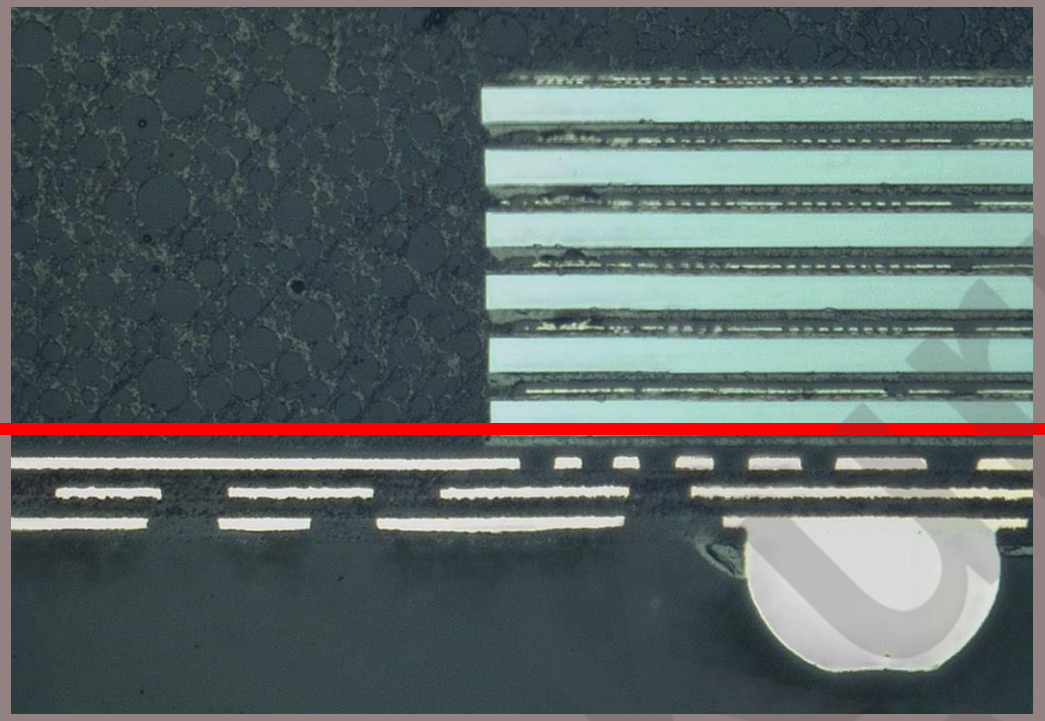
RDL#3 Layers

Wire Bonding area

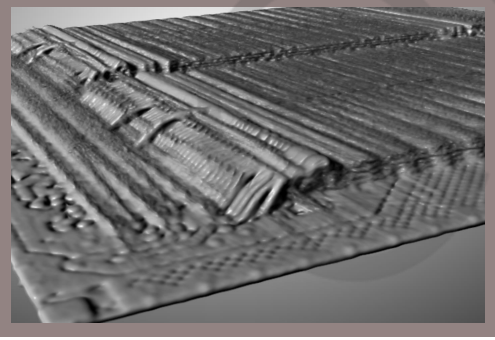


RDL#3 Layers

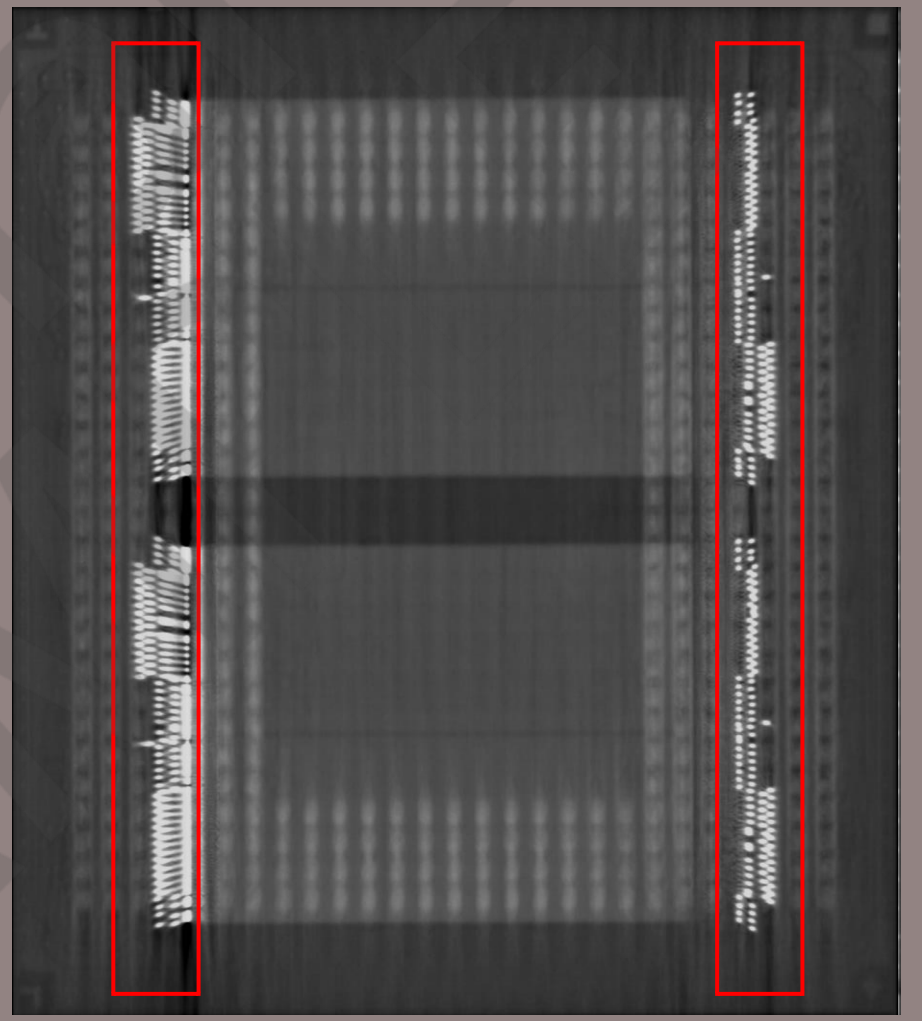
Package-Cross Section-RDL



Die Layers

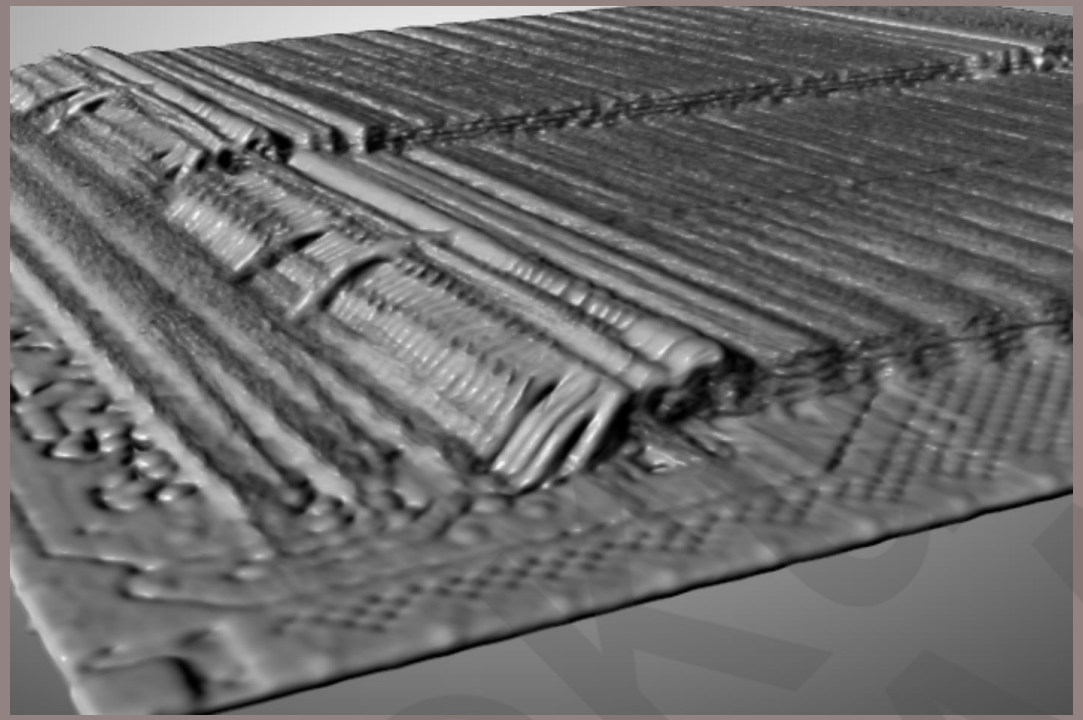


Wire Bonding area

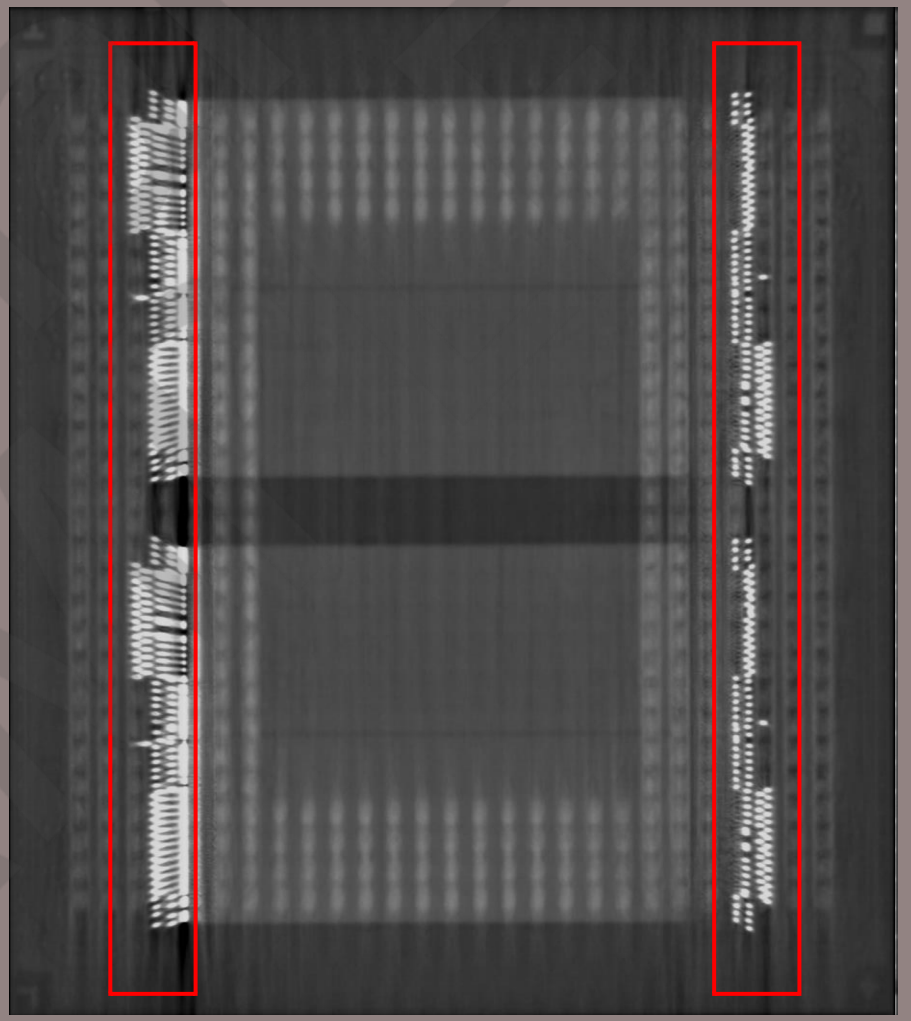


Die Layers

Package-Cross Section-RDL

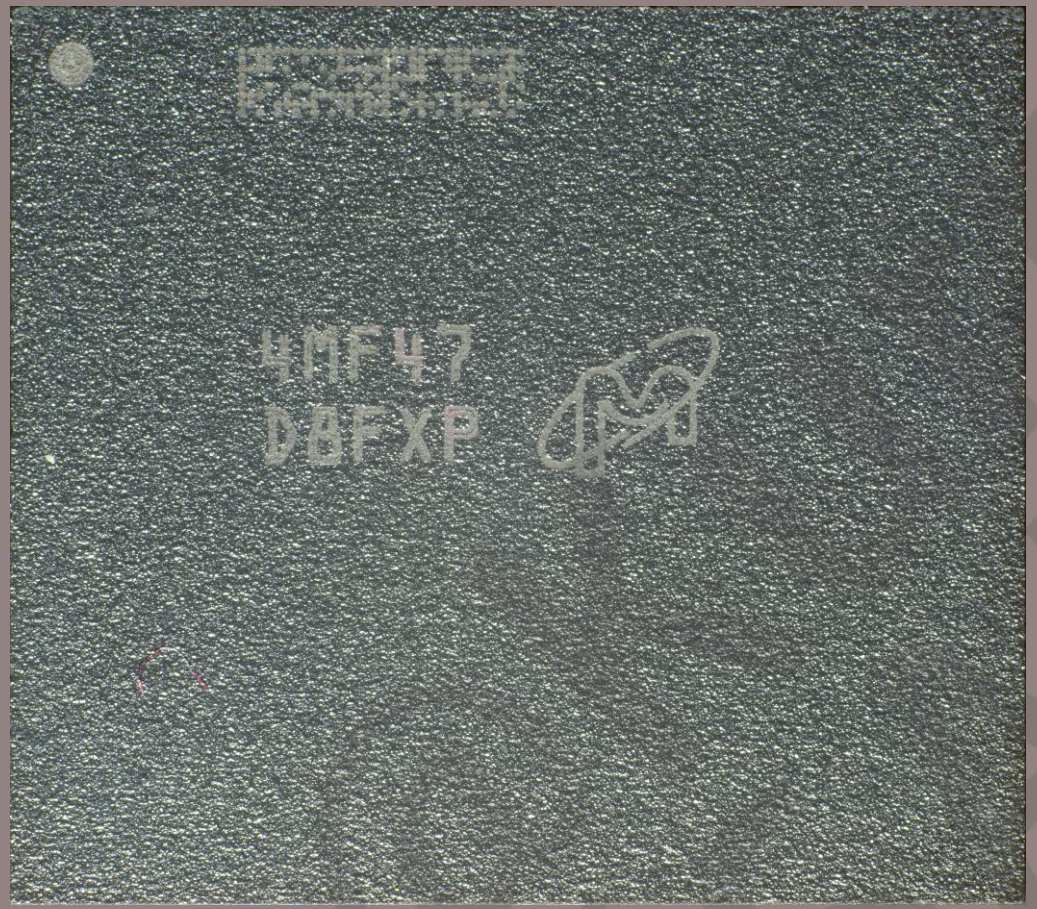


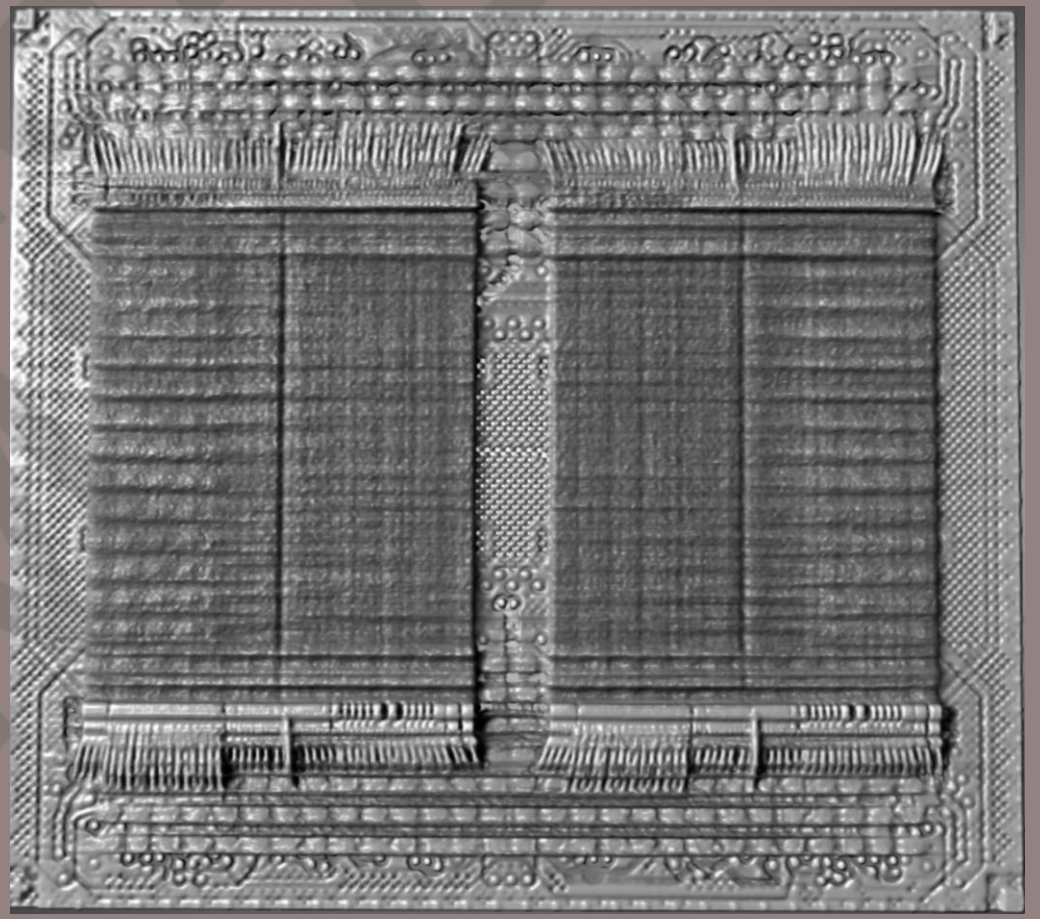
Wire Bonding area



Die Layers

Package-Cross Section-RDL

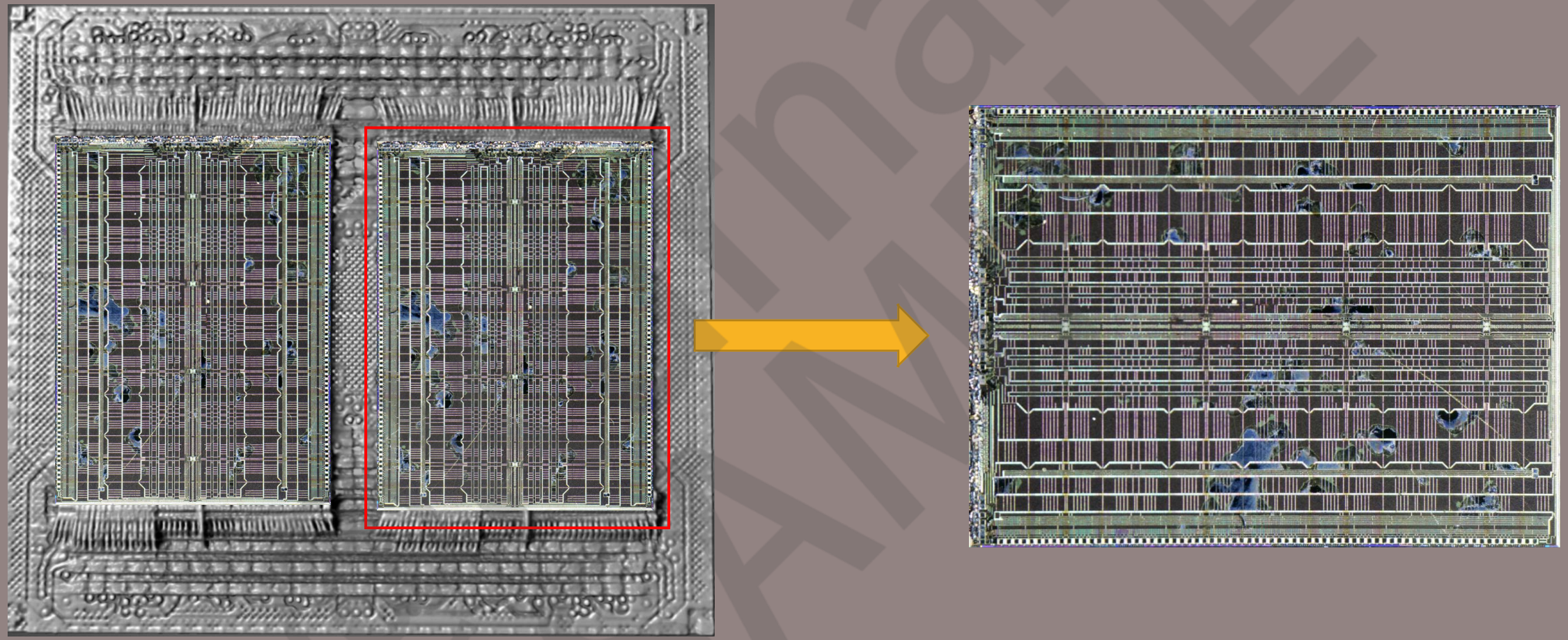




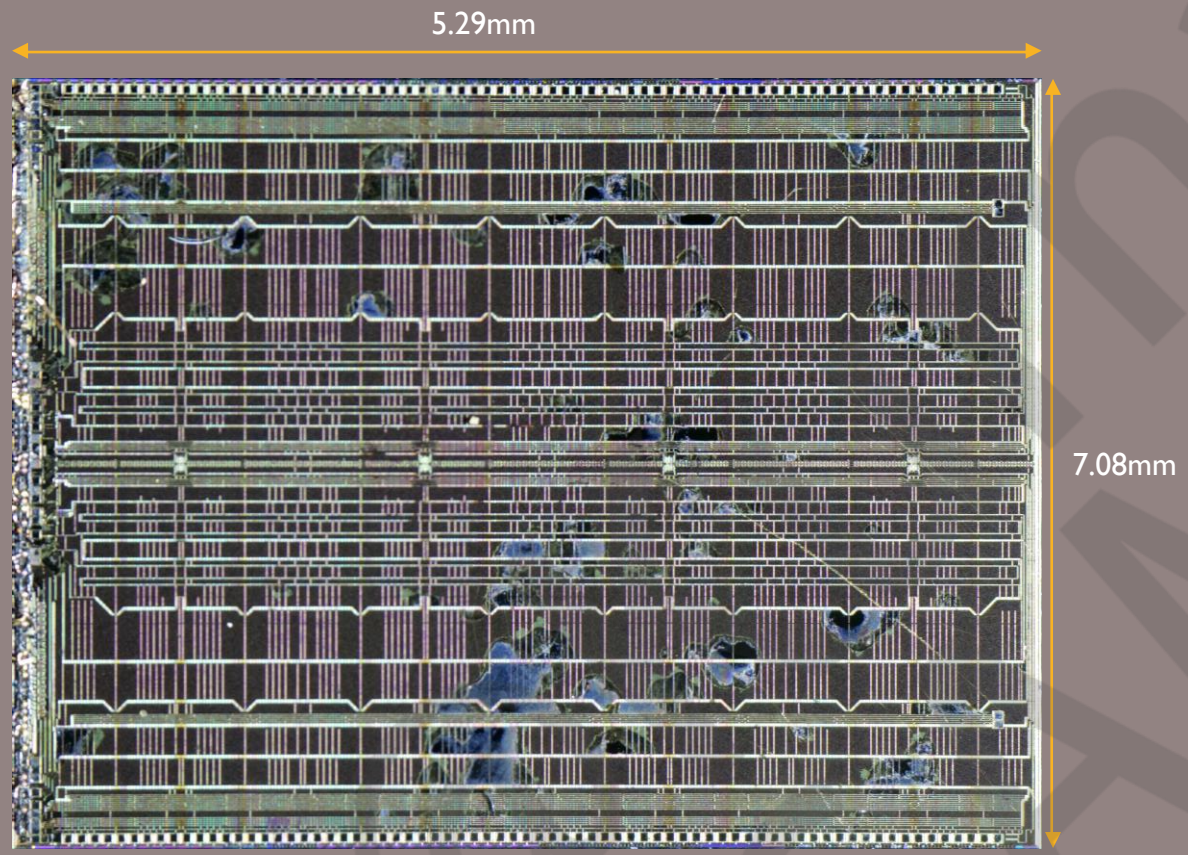
Memory Die analyze

Decaped

Memory Die Package Opening



Memory Die analyze



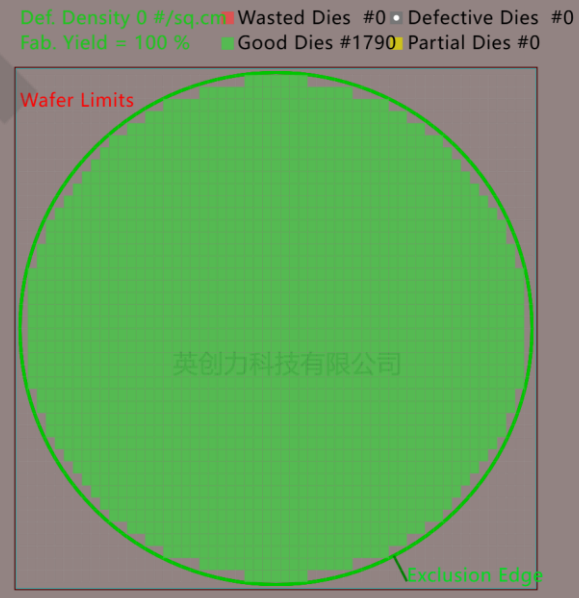
Micron Lpddr5 16Gb Memory Die

Die area: 37.4532mm2
(5.29x7.08mm)

NB of Die Per Wafer: 1790

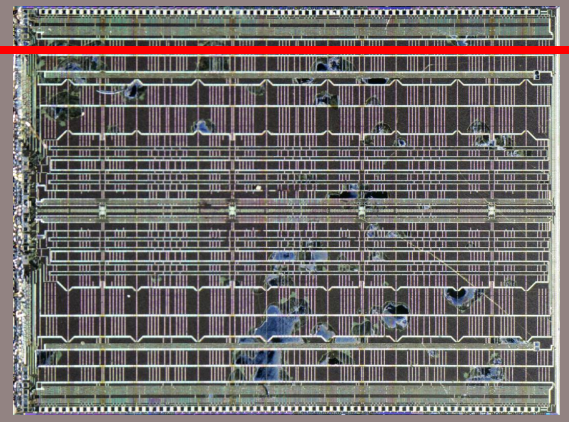
Die density: 16Gb/37.4532mm2
0.4272Gb/mm2

Potential Gb/Wafer 28640Gb



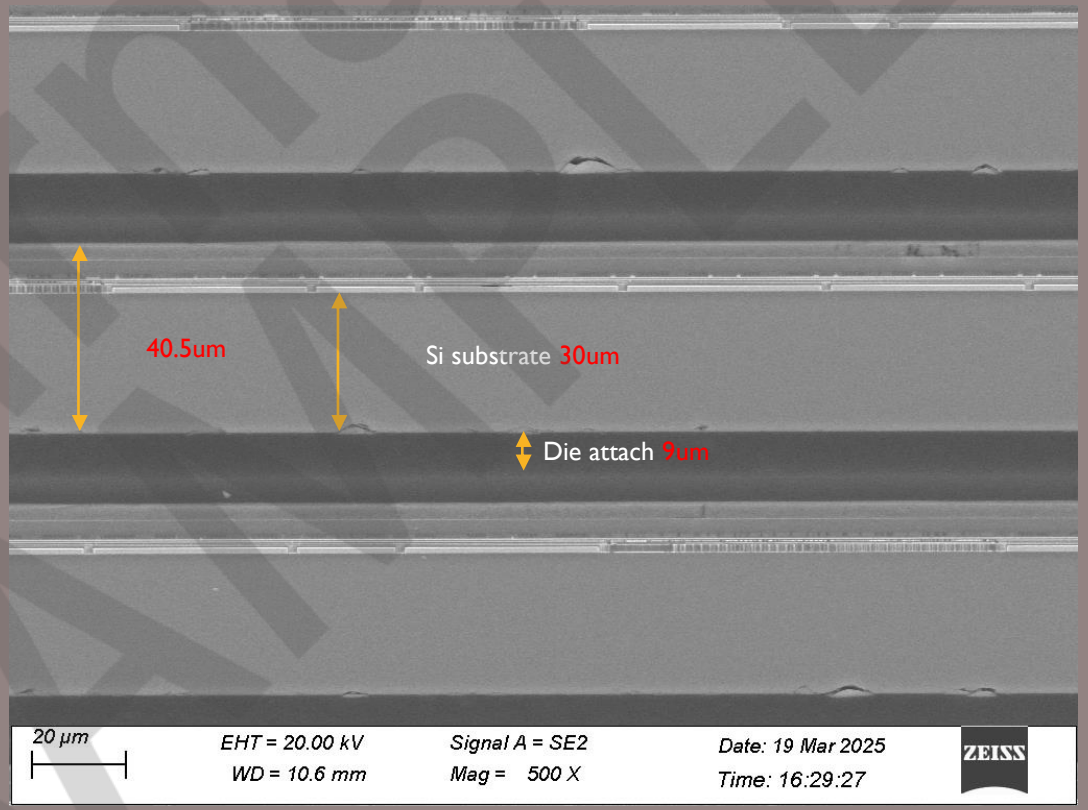
Max Dies Per Wafer (without defect) #1790

Memory Die analyze-Cross Section-X



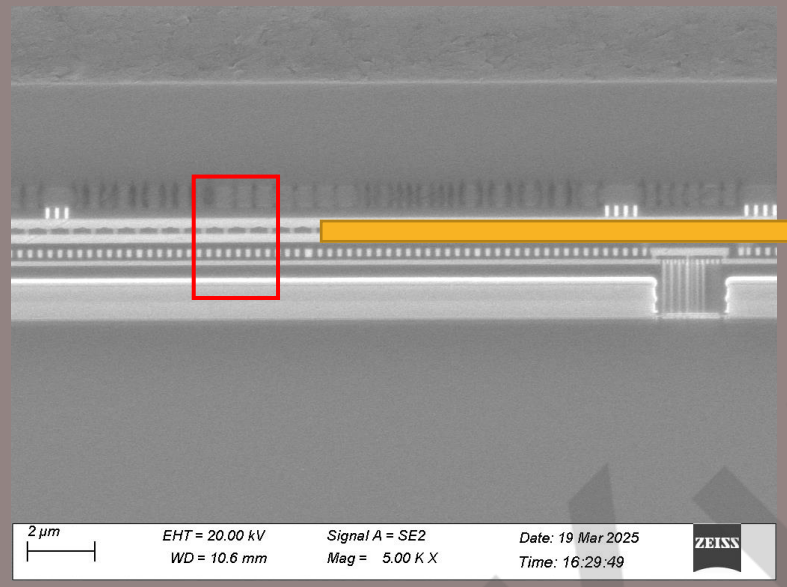
X Cut

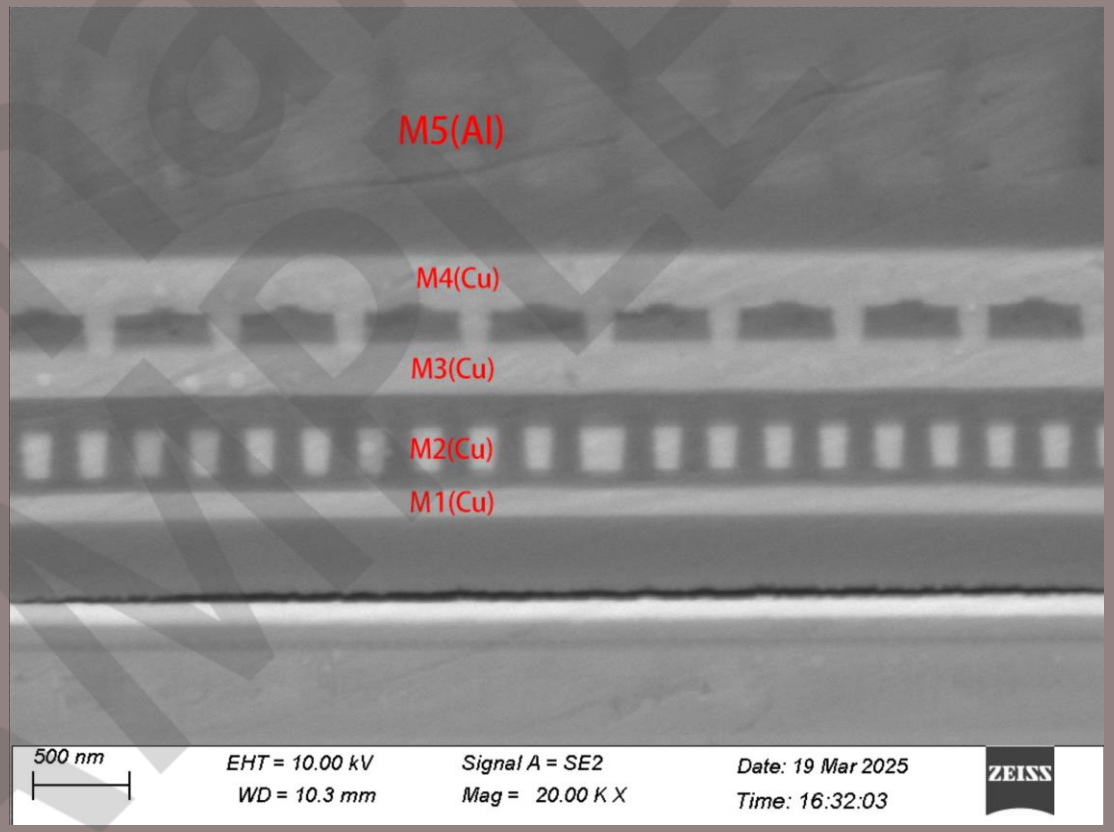
Micron Lpddr5 16Gb Memory Die



Memory Total thickness	40.5um
Si Sub thickness	30um
Die attach thickness:	9um

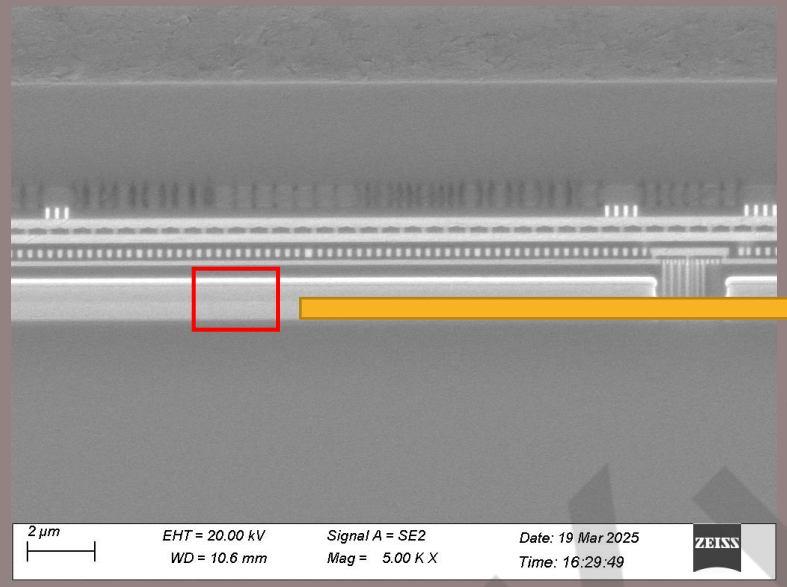
Memory Die analyze-Top Metal



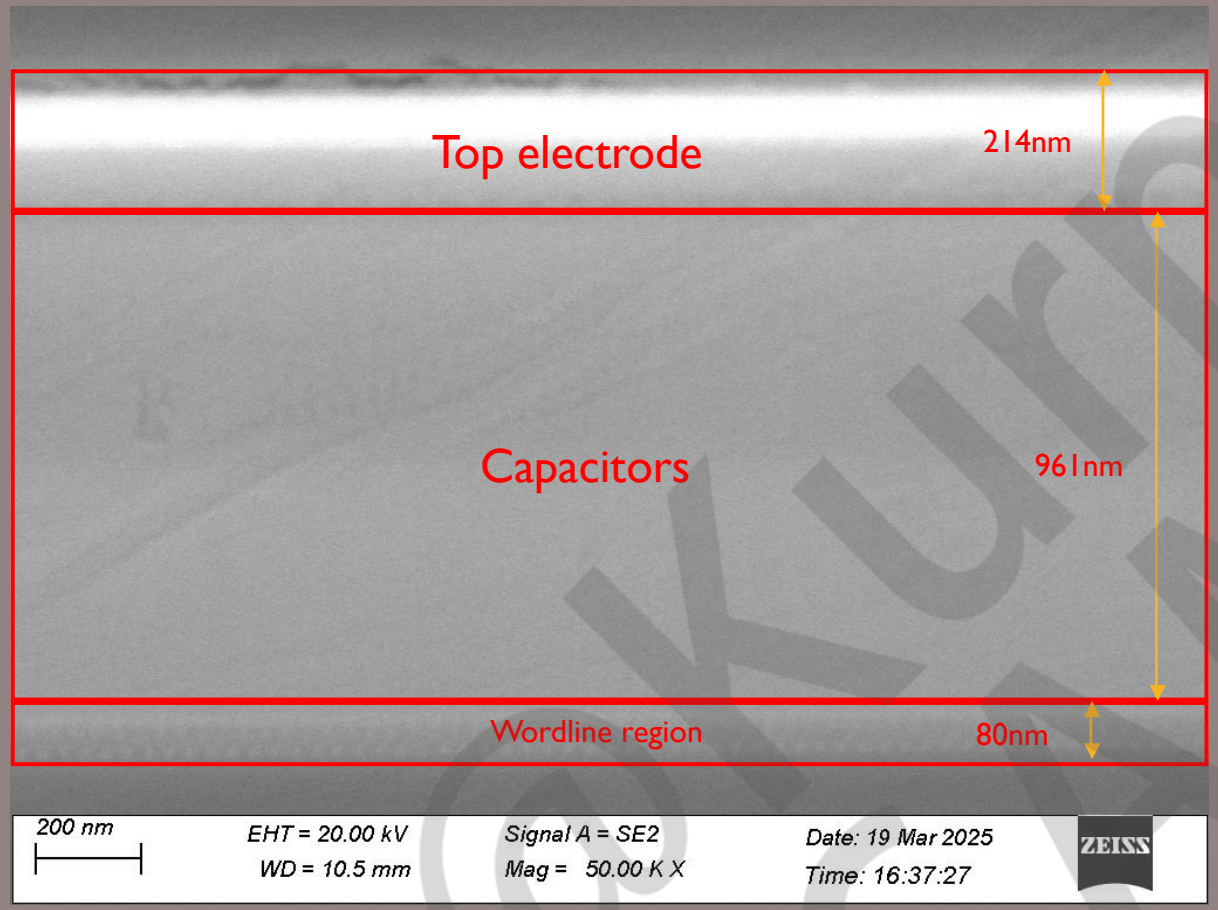


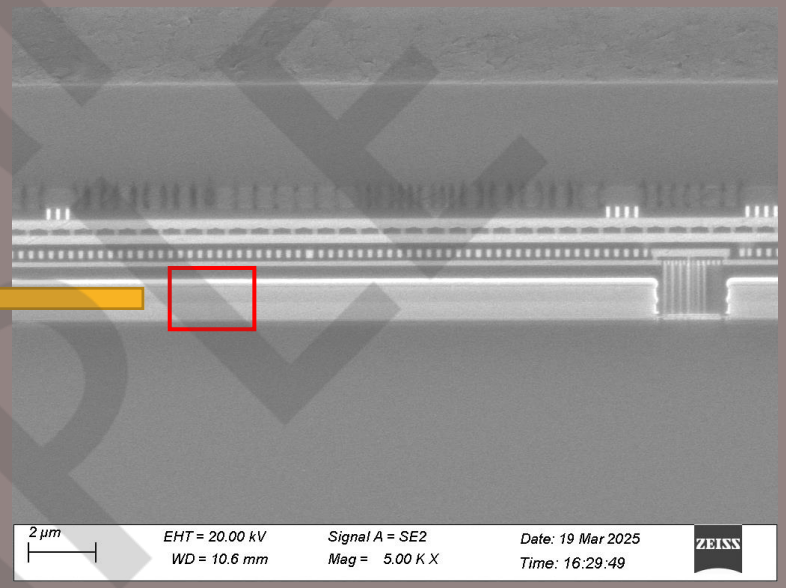
Dram die have 5 Layers Metal on the top

Memory Die analyze-Memory Capactiors



Memory Die analyze-Memory Capactiors

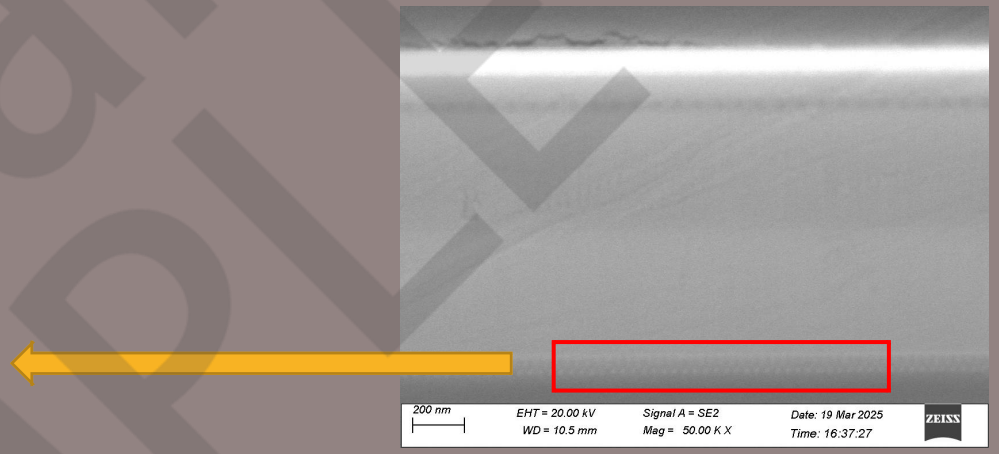




Capacitors Total thickness: 1255nm

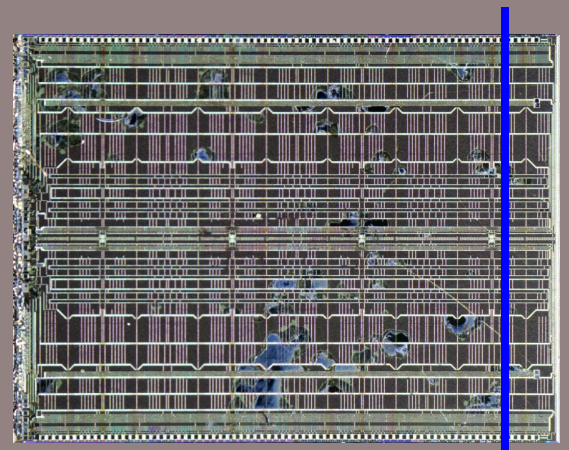
Top electrode thickness: 214nm
Capacitors thickness: 961nm
Wordlline region thickness: 80nm

Memory Die analyze-Memory Capactiors



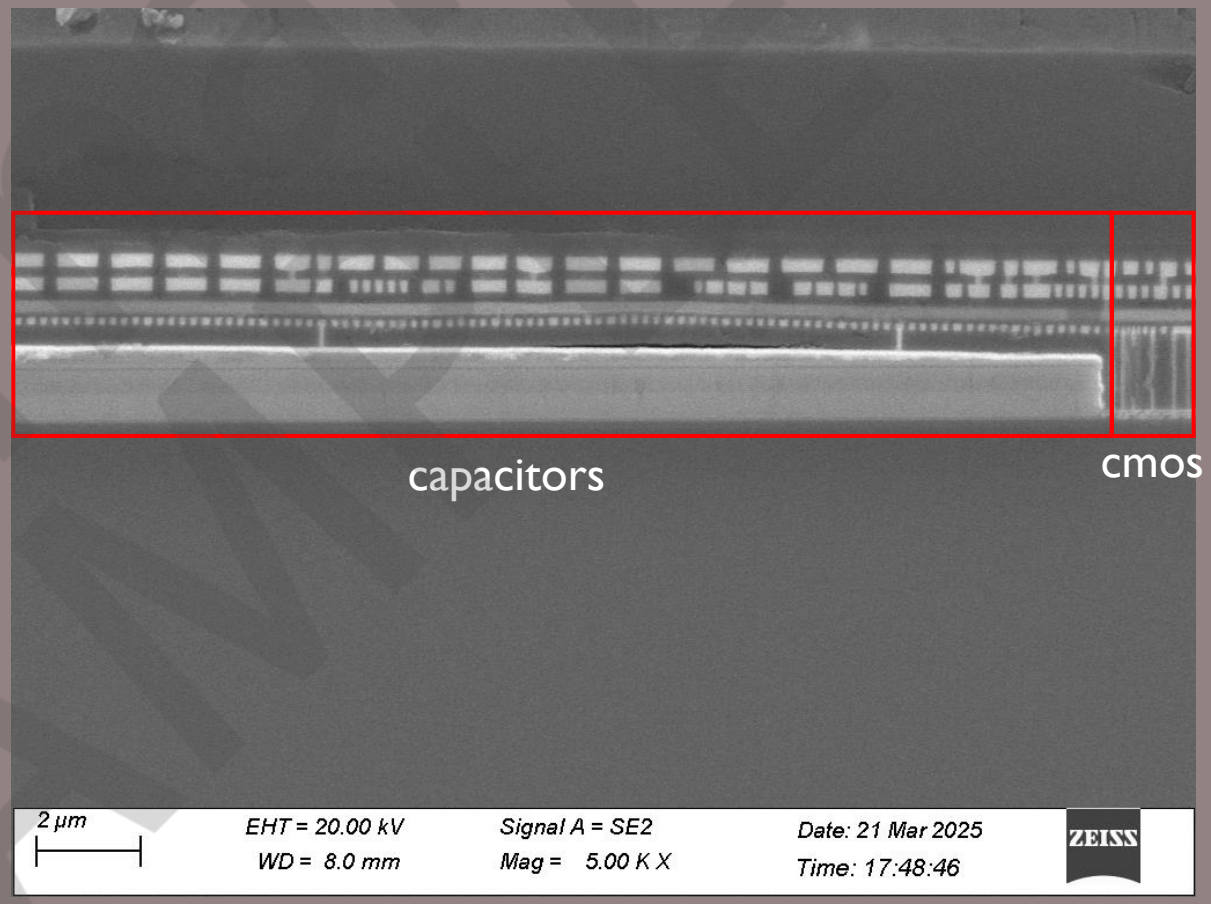
Need to cut another axial

Memory Die analyze-Cross Section-Y

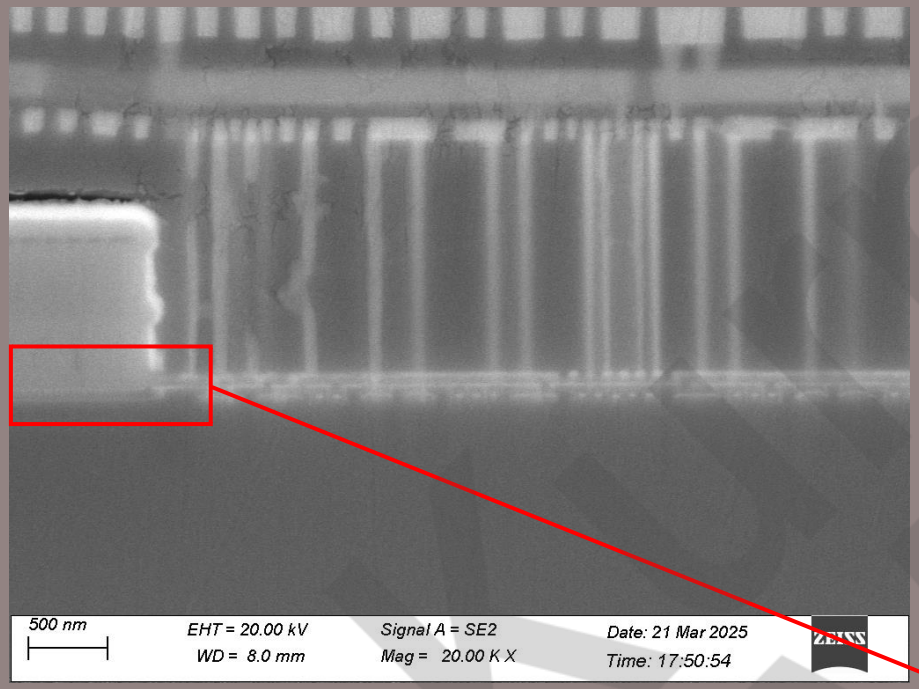


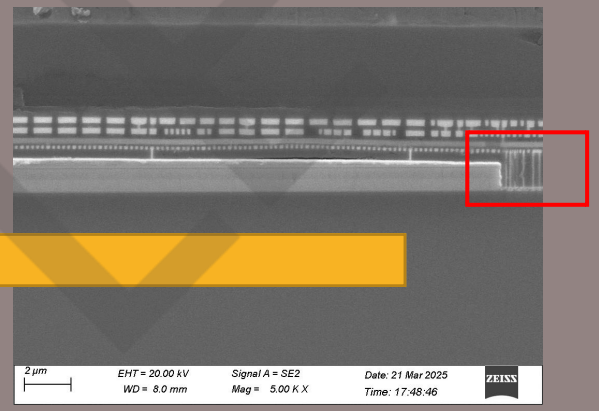
Micron Lpddr5 16Gb Memory Die

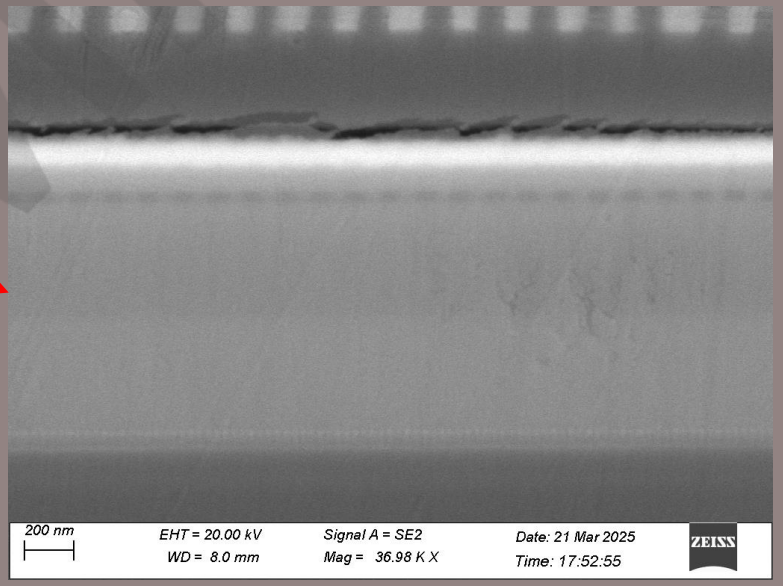
Y Cut



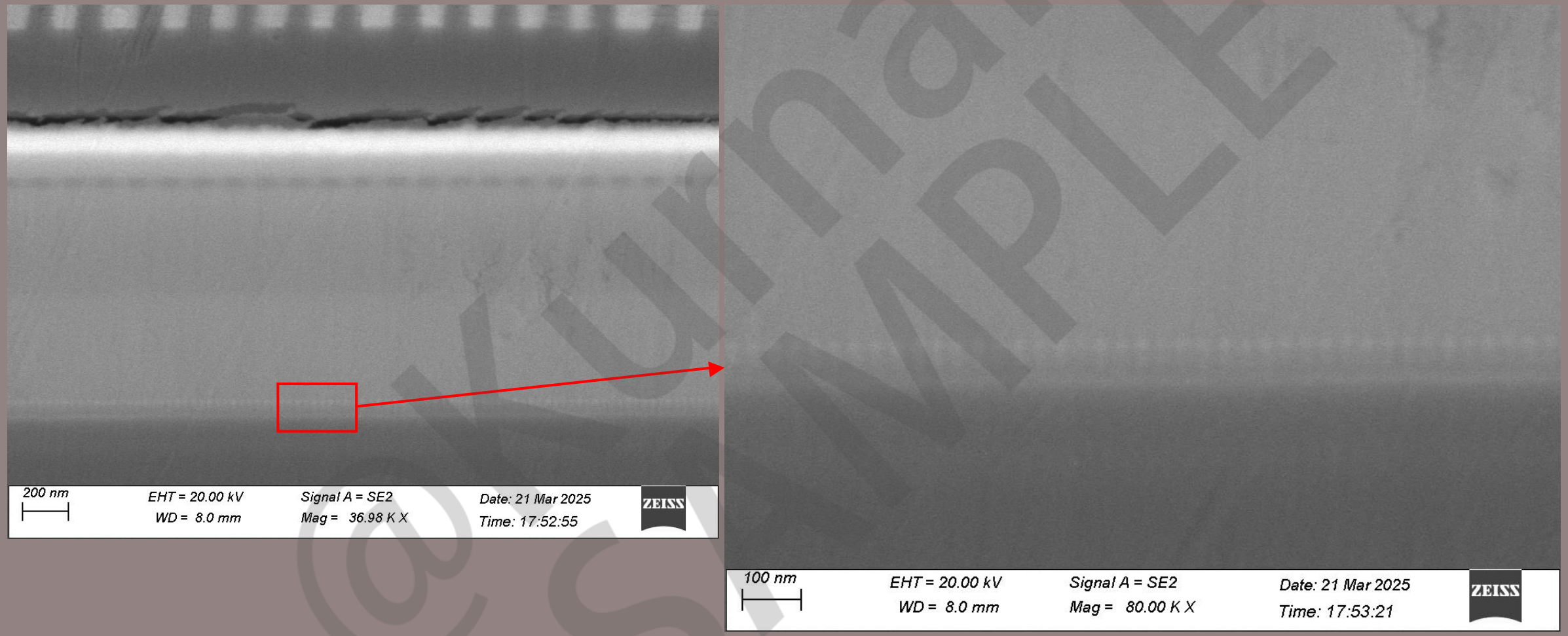
Memory Die analyze-Memory Capactiors



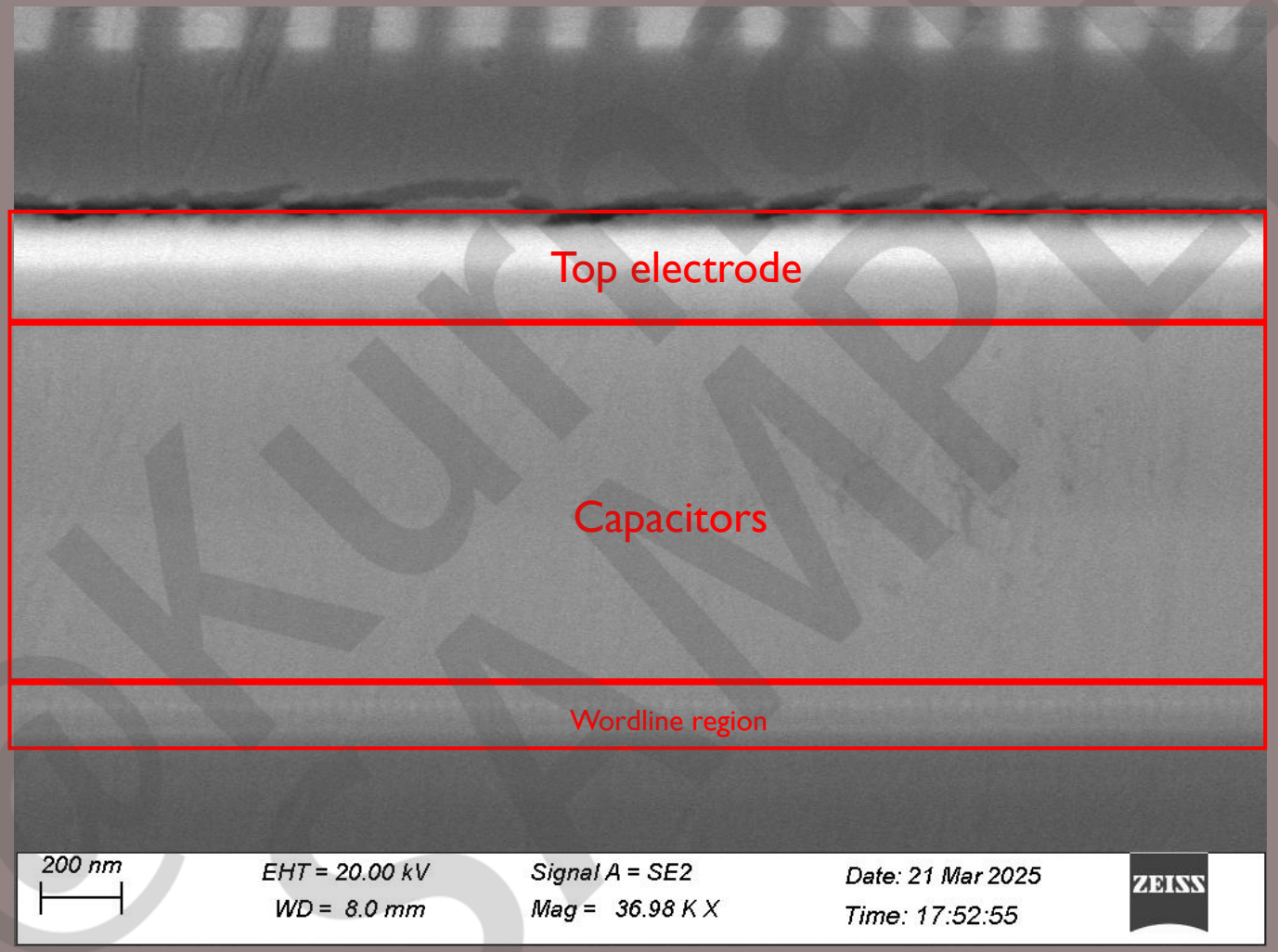




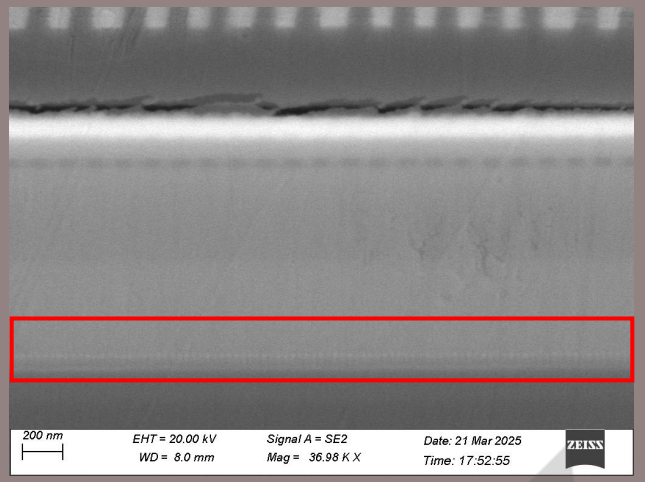
Memory Die analyze-Memory Capactiors



Memory Die analyze-Memory Capactiors

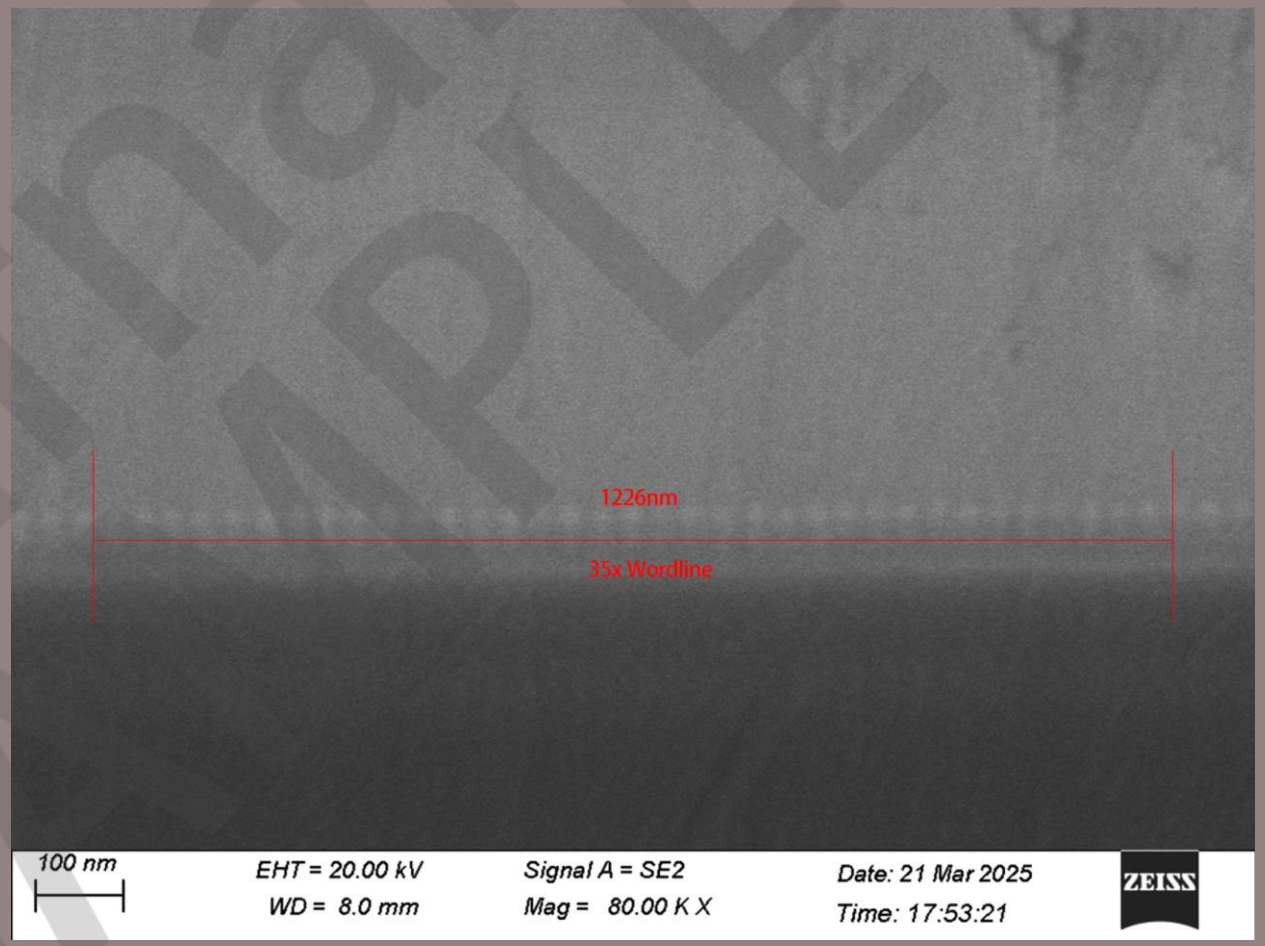


Memory Die analyze-Memory Capactiors

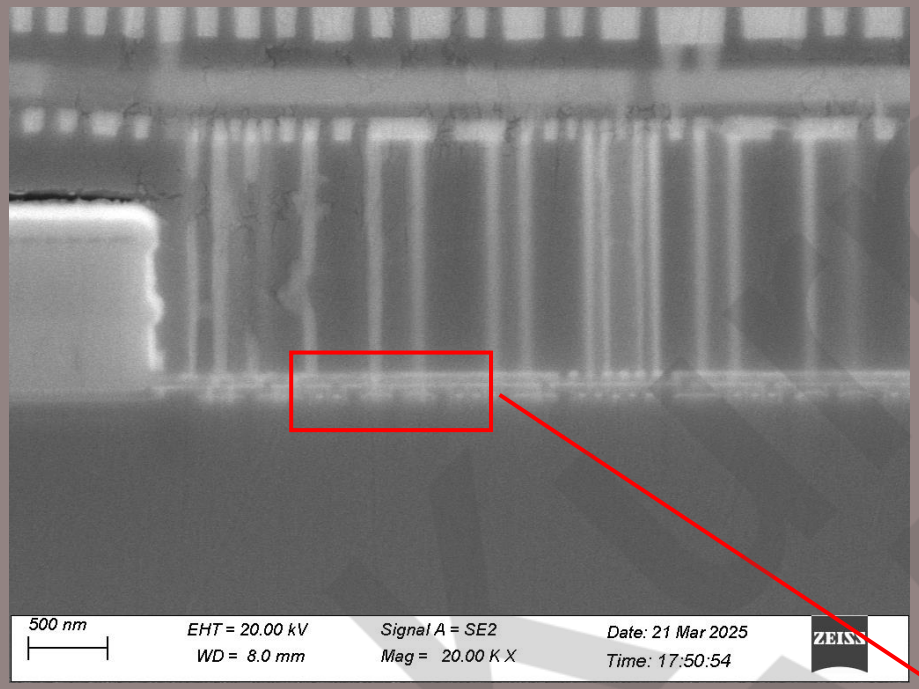


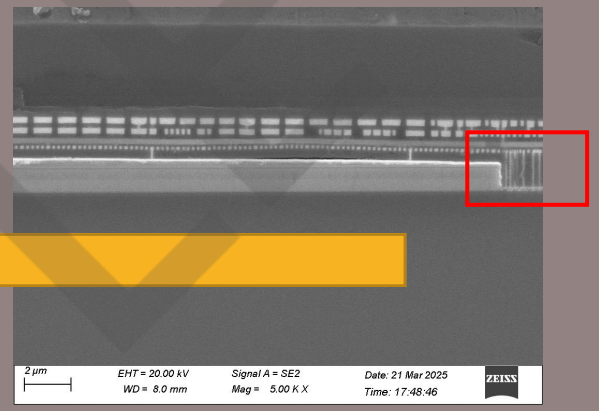
Wordline pitch: 35.03nm

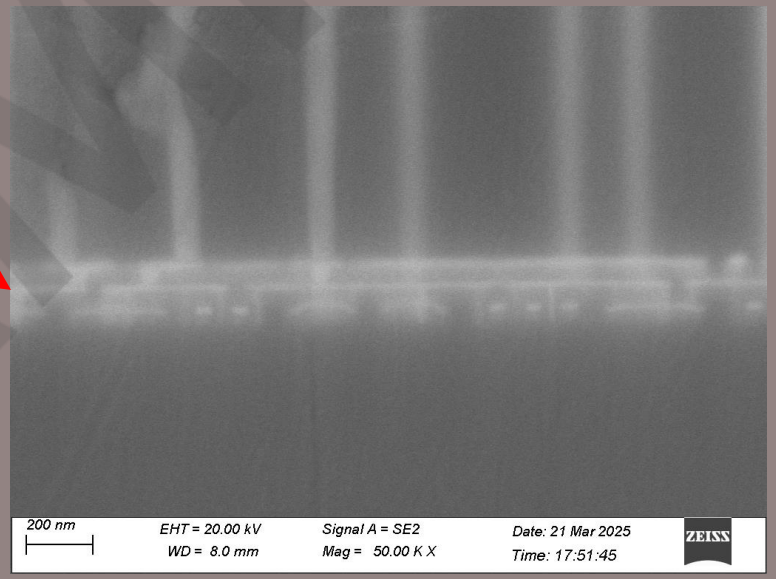
Technology node: 17.5nm



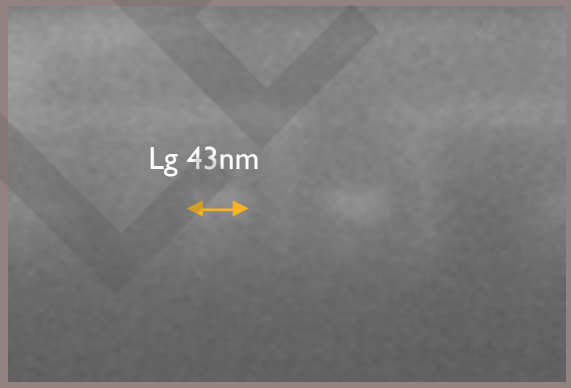
Memory Die analyze- CMOS Logic







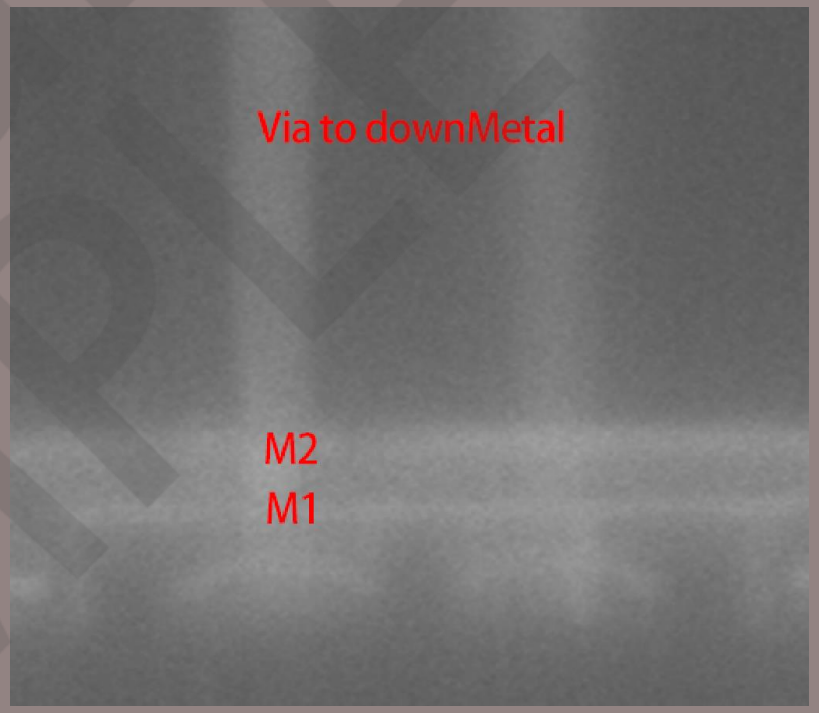
Memory Die analyze- CMOS Logic



Gate Length: 43nm

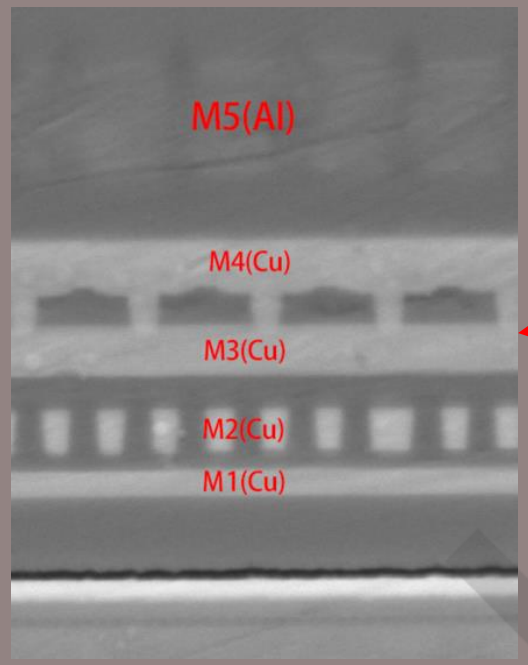
The Cmos technology node: 45nm

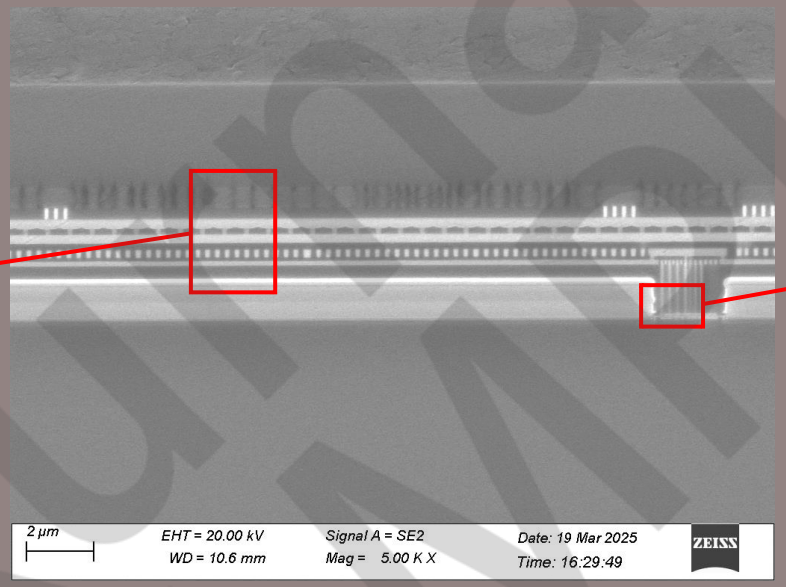
Memory Die analyze-Down Metal

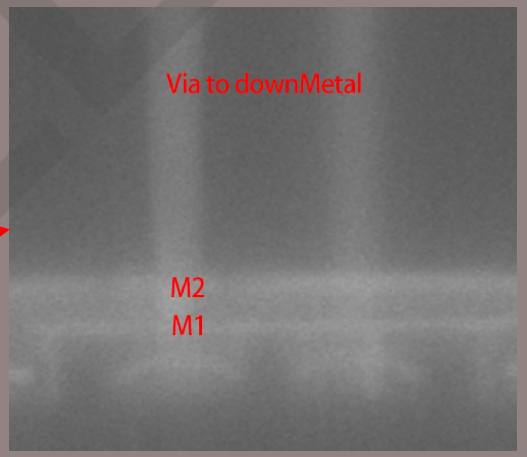


Down Metal Layer have 2 Metal layers

Memory Die analyze-Metal Layers







Top Metal Layers have 5 Metal Layers → Total have 7 Metal Layers ← Down Metal Layer have 2 Metal layers

Summary

Summary

Micron 24GB Lpddr5 summary

Package analyze

On package have 12 DRAM dies

Package capacity: 24GB/192Gb
Die capacity: 16Gb/die

Package RDL Nb: 3Layers

Die process

Die area: 37.4532mm2
(5.29x7.08mm)

NB of Die Per Wafer: 1790

Die density: 16Gb/37.4532mm2
0.4272Gb/mm2

Potential Gb/Wafer 28640Gb

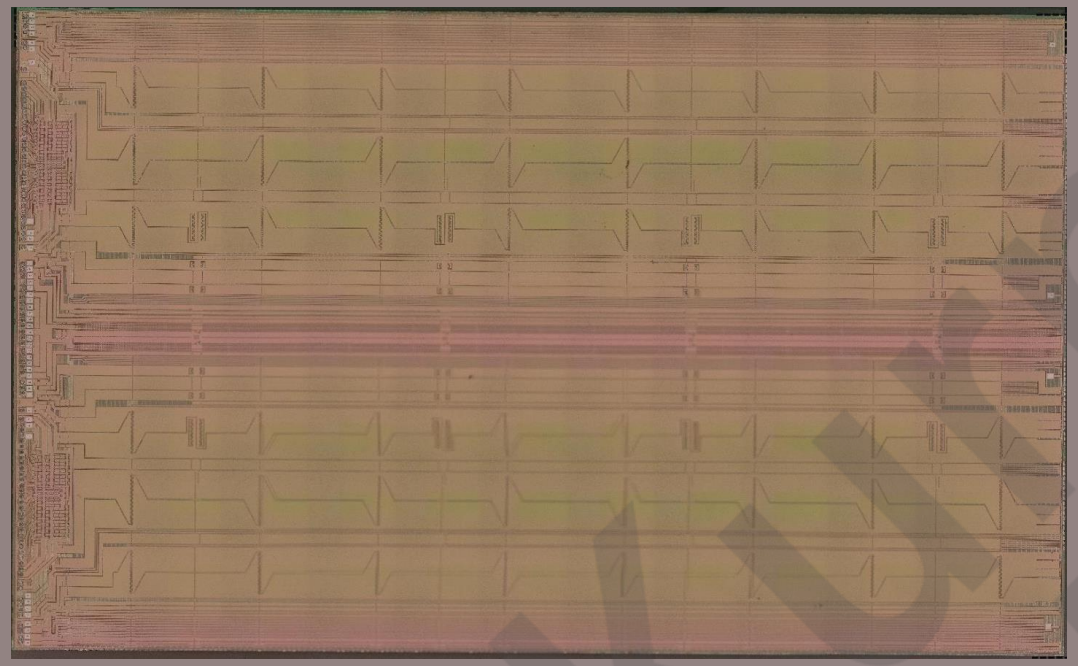
Cmos and Metal layers front-end process

Process Type: CMOS(Digital,Analog)
Metal Layers: 5+2=8 Total
Technology node: 45nm for the CMOS transistors

Dram cell process

Technology node: 1y nm (17.5nm)

Micron Lpddr5 VS

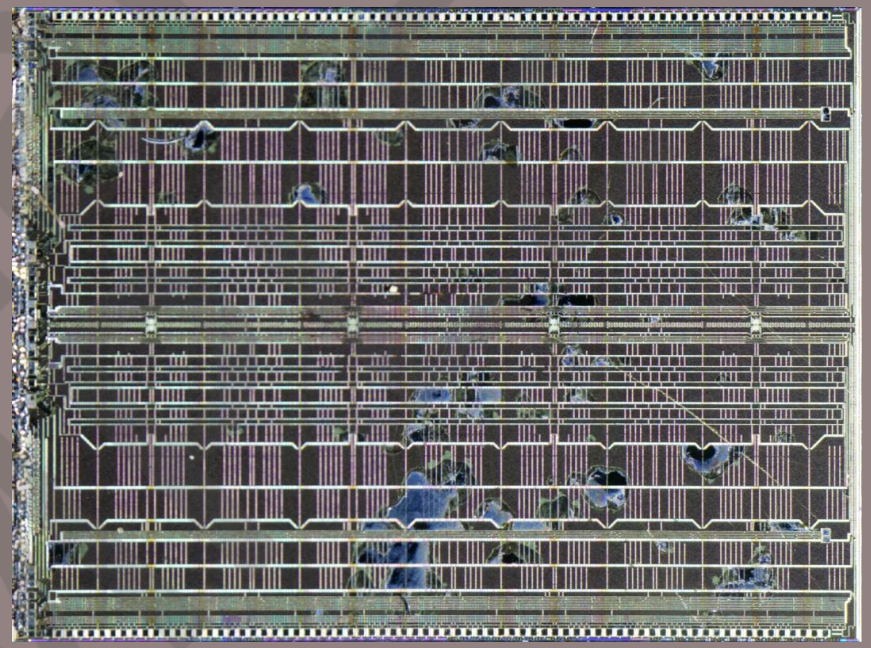


Micron Lpddr5 12Gb Memory Die

Dram Technology node: 18nm(1Ynm)

Die area: 50.89mm2

Die density: 12Gb/50.89mm2
0.23Gb/mm2



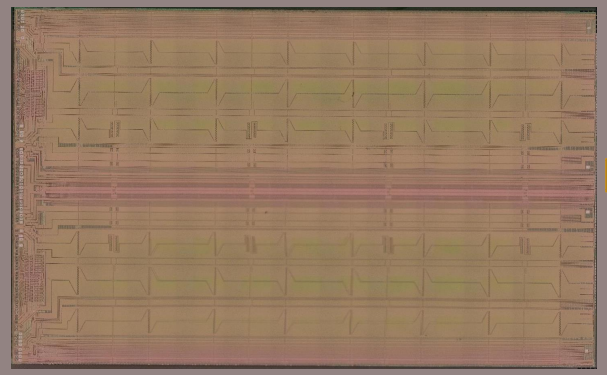
Micron Lpddr5 16Gb Memory Die

Dram Technology node: 17.5nm(1Ynm)

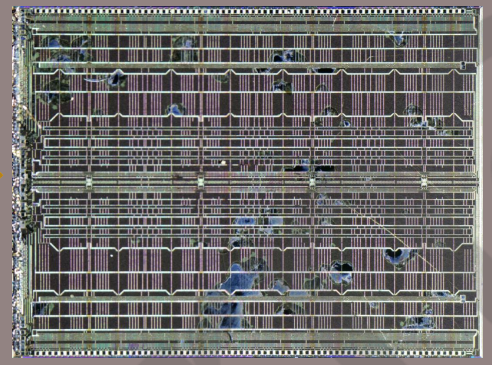
Die area: 37.4532mm2

Die density: 16Gb/37.4532mm2
0.4272Gb/mm2

Micron Lpddr5 VS



Micron Lpddr5 12Gb Memory Die



Micron Lpddr5 16Gb Memory Die

Micron's LPDDR5 has increased capacity by 33% (12Gb→16Gb/die) while reducing die size by 26.4%

Achieving 85.7% density improvement

Despite retaining the 1Y nm DRAM process node,
the equivalent process node has been refined from 18nm to 17.5nm.

Dram Technology node:	18nm(1Ynm)
Die area:	50.89mm2
Die density:	12Gb/50.89mm2 0.23Gb/mm2

Dram Technology node:	17.5nm(1Ynm)
Die area:	37.4532mm2
Die density:	16Gb/37.4532mm2 0.4272Gb/mm2