Not For Sale

Li-Auto M100 Ultra

On chip analysis

Kurnal insights

Version 1.0 | 2026 Q2

Kurnal Insights

Kurnal-insights.com

Version of this Report

Version	Date	U/pdates	Author
V0	2026/03/17 19:34	writing	Kurnal
V0.1	2026/06/12 21:26	修改PPT模板	Kurnal
V1	2026/06/22	大抵是写完了	Kurnal

About Authors

This Report is made From @Kurnal

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WeChat: KurnalWeChat
Website: Kurnal-insights.com

01

Overview

Methodology

Executive Summary

Li-Auto M100 Ultra automotive driving SoC

TSMC N5
Process node

410.97 mm²
Die area · 25.51 × 16.11 mm

45 × 45 mm
FC-BGA package

24× A78AE
CPU cluster · 2.3 GHz

56 cores
NPU tensor engine · 56.76% die

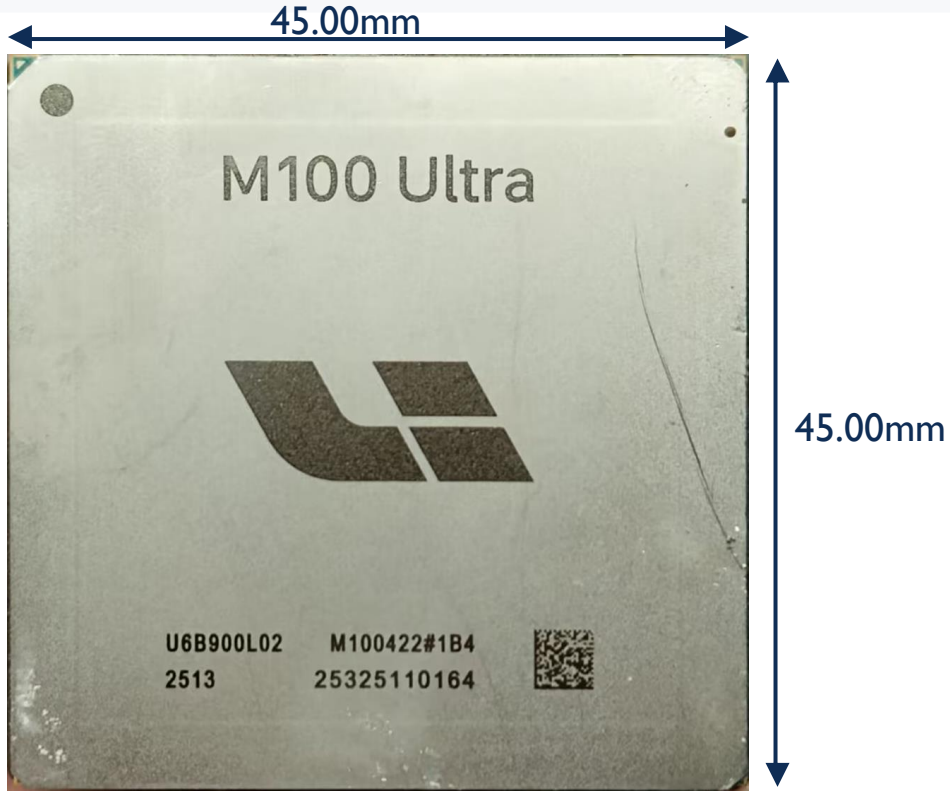
256-bit
LPDDR5 memory bus

An NPU-first SoC — the neural engine occupies **4.68×** the silicon of the 24-core CPU.

Physical analysis

Li-Auto M100Ultra

Package Analysis-Top Marking



M100Ultra-Topview

Measured package size
45 mm × 45 mm

Top Marking Analysis		
U6B900L02	Traceability Code	Likely internal traceability identifier for lot tracking
M100422#1B4	Version Code	Indicates product version or stepping information
2513	Date Code (YYWW)	Manufactured in 2025, Week 13
25325	Assembly/Test Code	Package assembly / test completed on 2025-03-25 (YYMDD format)
5110164	Internal Identifier	Likely internal package identifier or part number

Package Overview

- Package Type : FC-FOP (*Flip-Chip On Package*)
- Package Size : 45 mm × 45 mm
- Surface Area : 2025 mm²

Key Observation

The top marking provides key information on product version, manufacturing date, and internal traceability codes used for production and quality control.

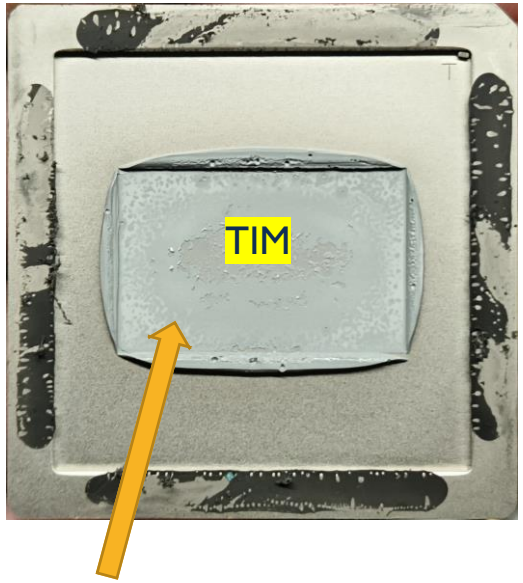
Package analyze

1 Top View (As Received)

M100Ultra-Topview

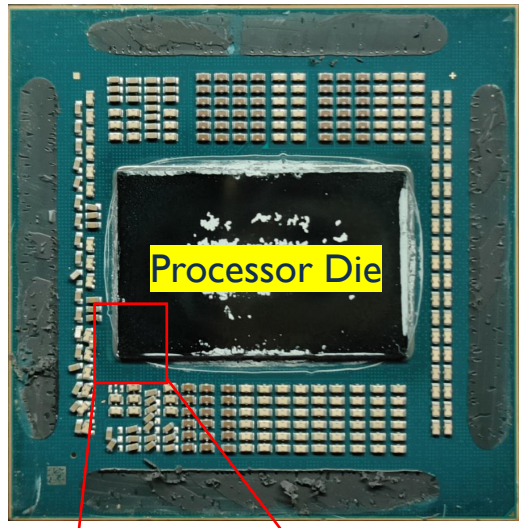
Remove IHS

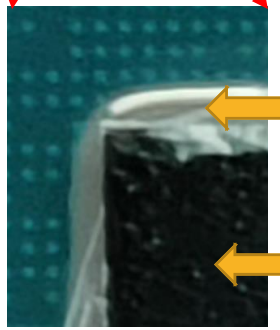
M100Ultra-IHS



Use silicone grease for TIM
Uniform application helps improve thermal contact and reliability.

M100Ultra-Sub





Underfiller

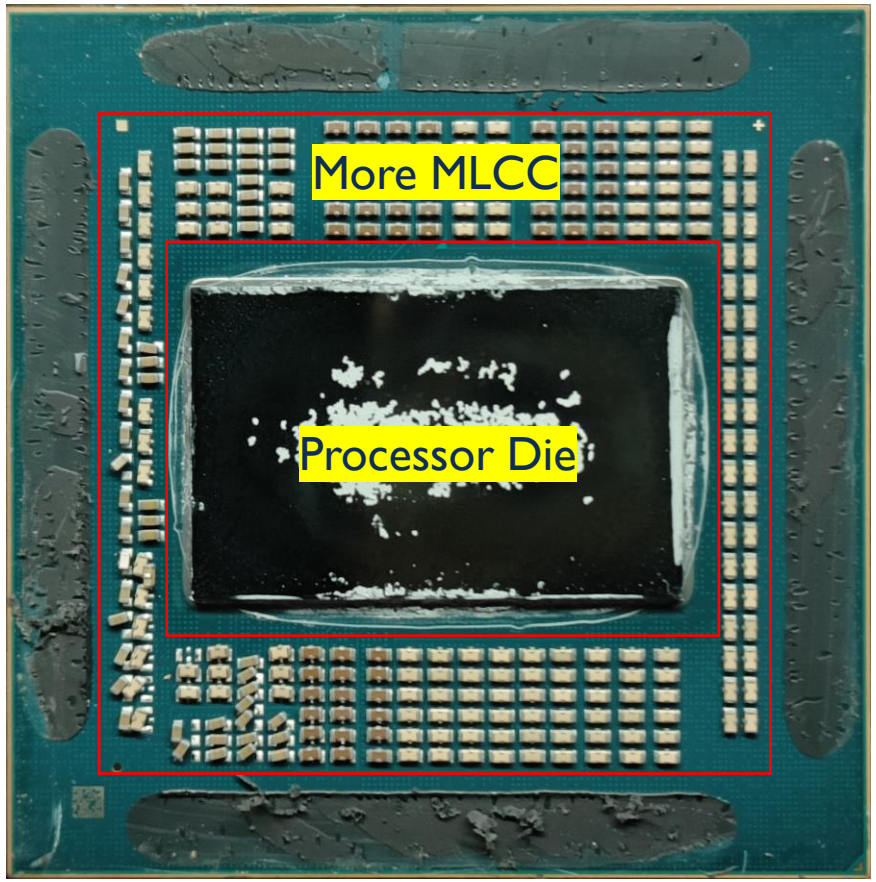
Processor Die

IHS Removal
The IHS was carefully removed to expose the processor die and substrate.

TIM Application
Silicone-based TIM is applied uniformly across the die for optimal thermal performance.

Underfill Observed
Underfiller is present along the die edges, providing structural support and reliability.

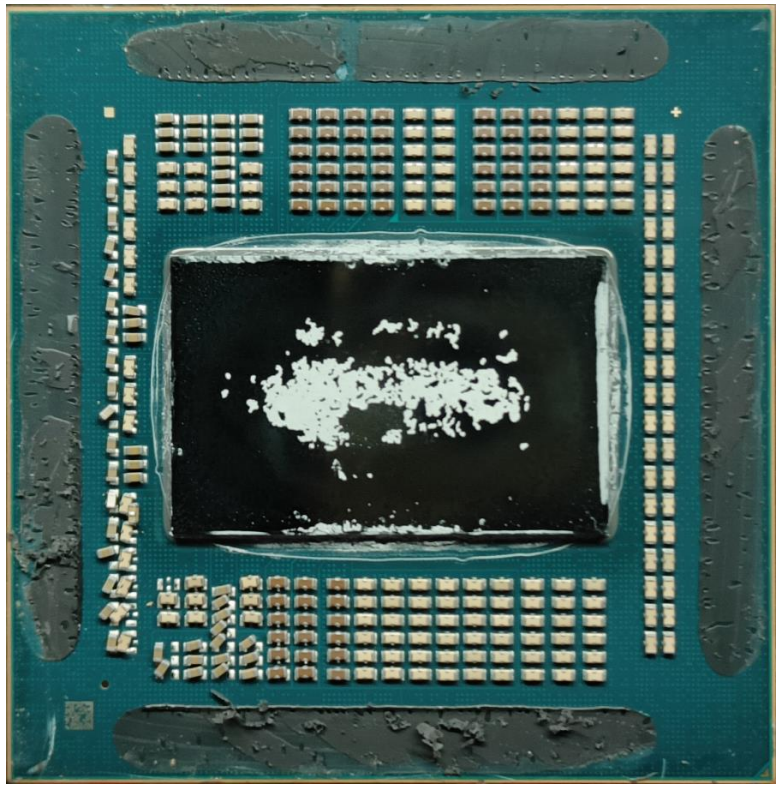
Package analyze-MLCC



M100Ultra-Sub

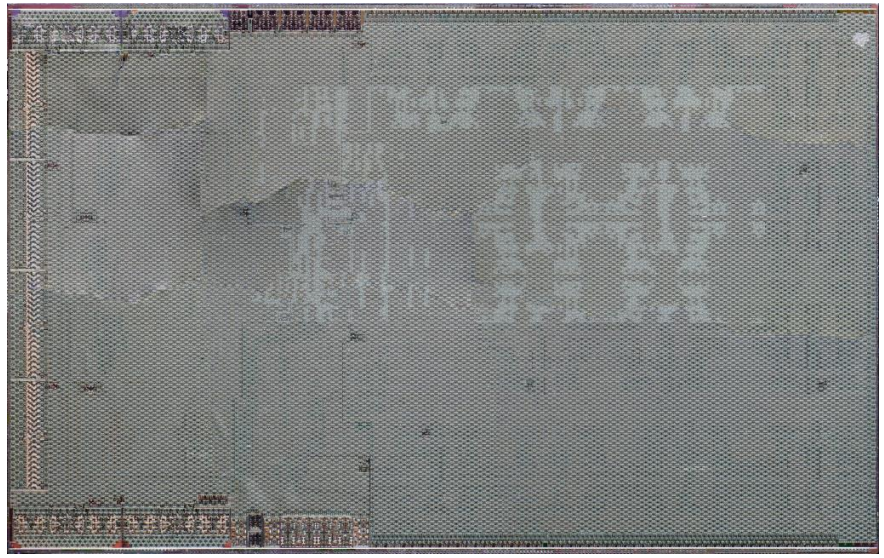
Package analyze

Package (Top View) – Before Decap

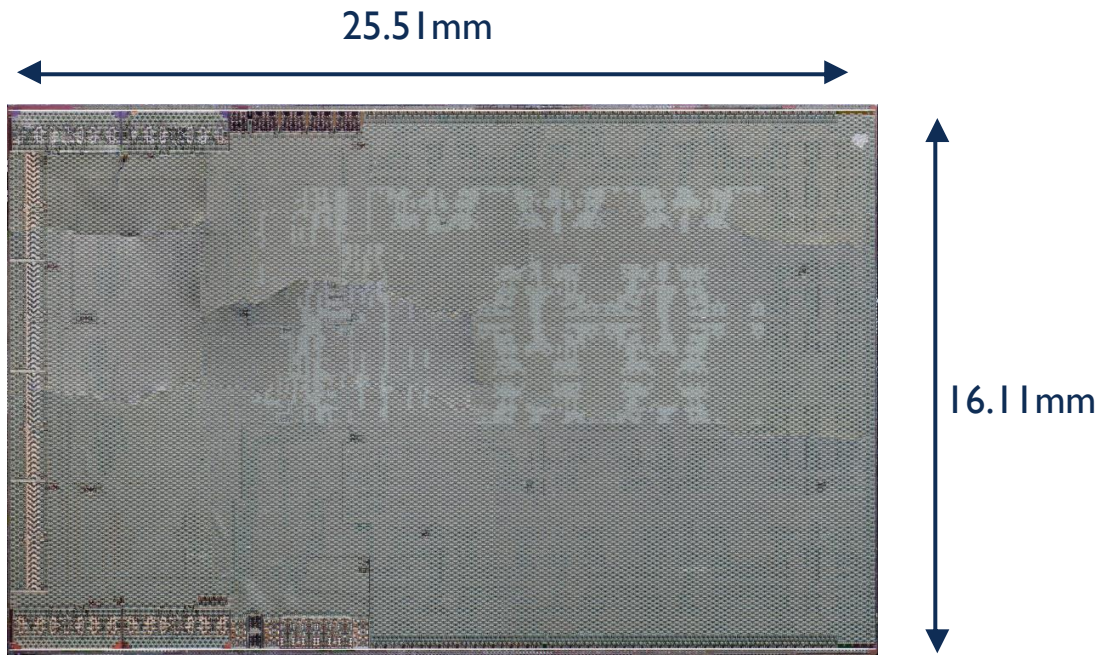


Decaped

Die (Top View) – After Decap

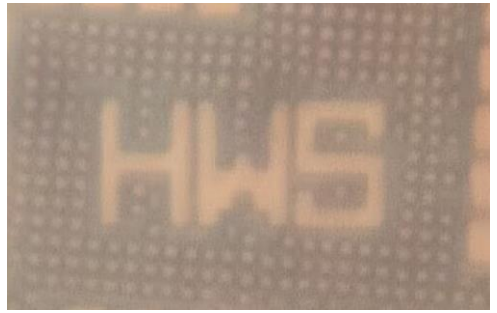


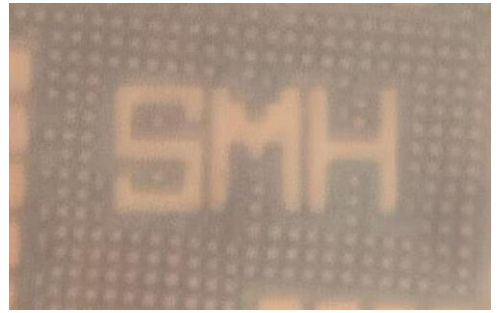
Die-mark



Die shot pics

Die size:	410.966 mm^2
Die Thickness:	780 µm
Die size in used:	10.74 mm × 12.78 mm
Sealing width:	60 µm / 90 µm

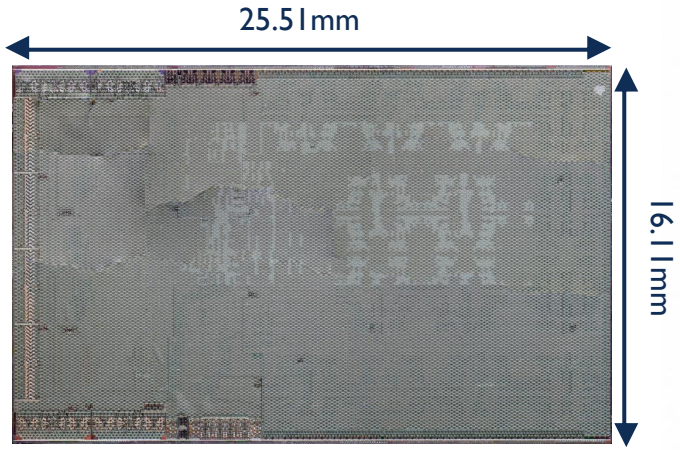




Die Mark	Die Mark : HWS or SMH

DPW(Die-Per-Wafer) Analysis

1. Die Size (From Previous Analysis)



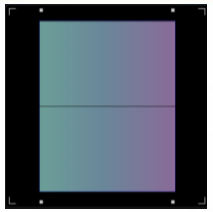
Estimated Die Size	
Width (Horizontal)	25.51mm
Height (Vertical)	16.11mm
Die Area	410.9661mm2

2. DPW Calculation Result

DPW
(Dies Per Wafer)

148
dies / wafer

3. Mask Information



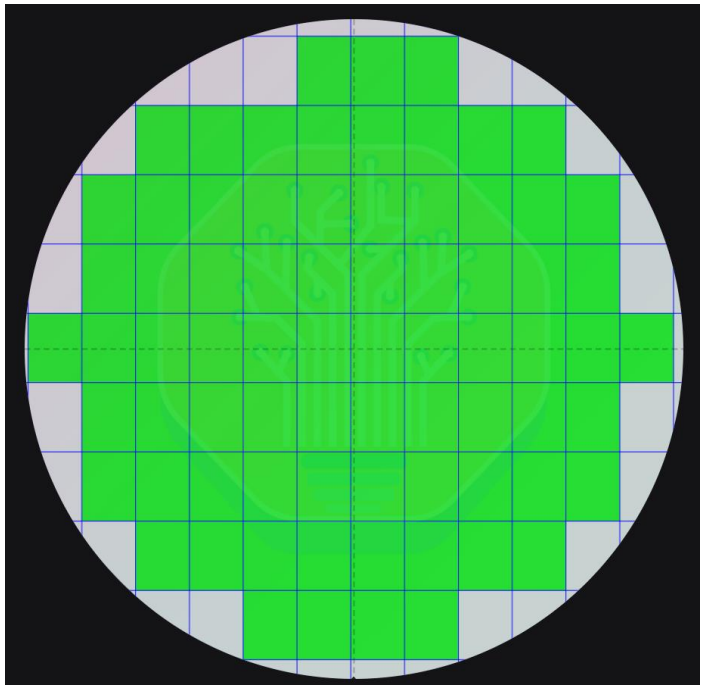
Mask Type

Die Per Mask 2:1

4. Utilization Metrics

Mask Utilization (MFU)	94.828%
Wafer Utilization (OWE)	85.177%
Mask on Wafer Efficiency (MOWE) MFU × OWE	80.778%

5. Wafer Map (Full Mask 2:1)



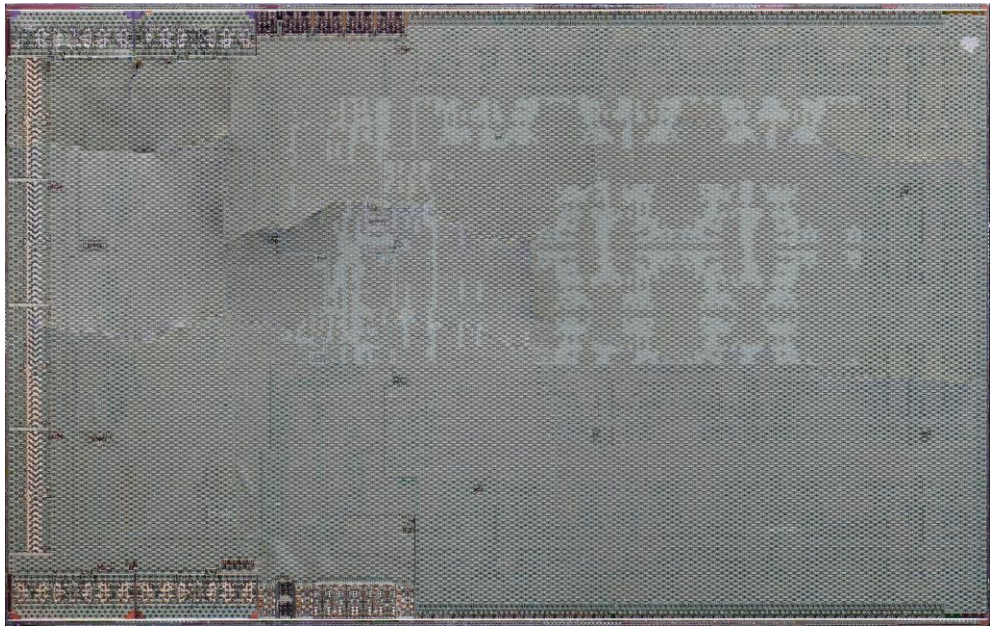
Summary

- Die size of 25.51mm x 16.11mm(410.966mm2)
- Full mask 2:1 is assumed for DPW calculation
- The resulting DPW is 148 dies per wafer
- Overall Wafer efficiency(MOWE) is 80.778%

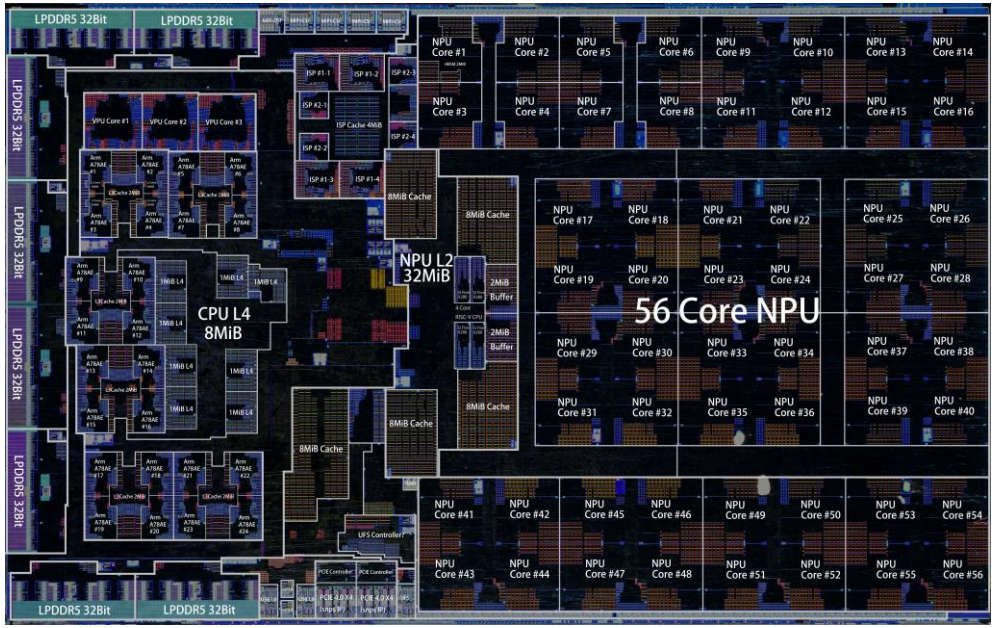
On-Chip Analysis

Li-Auto M100Ultra

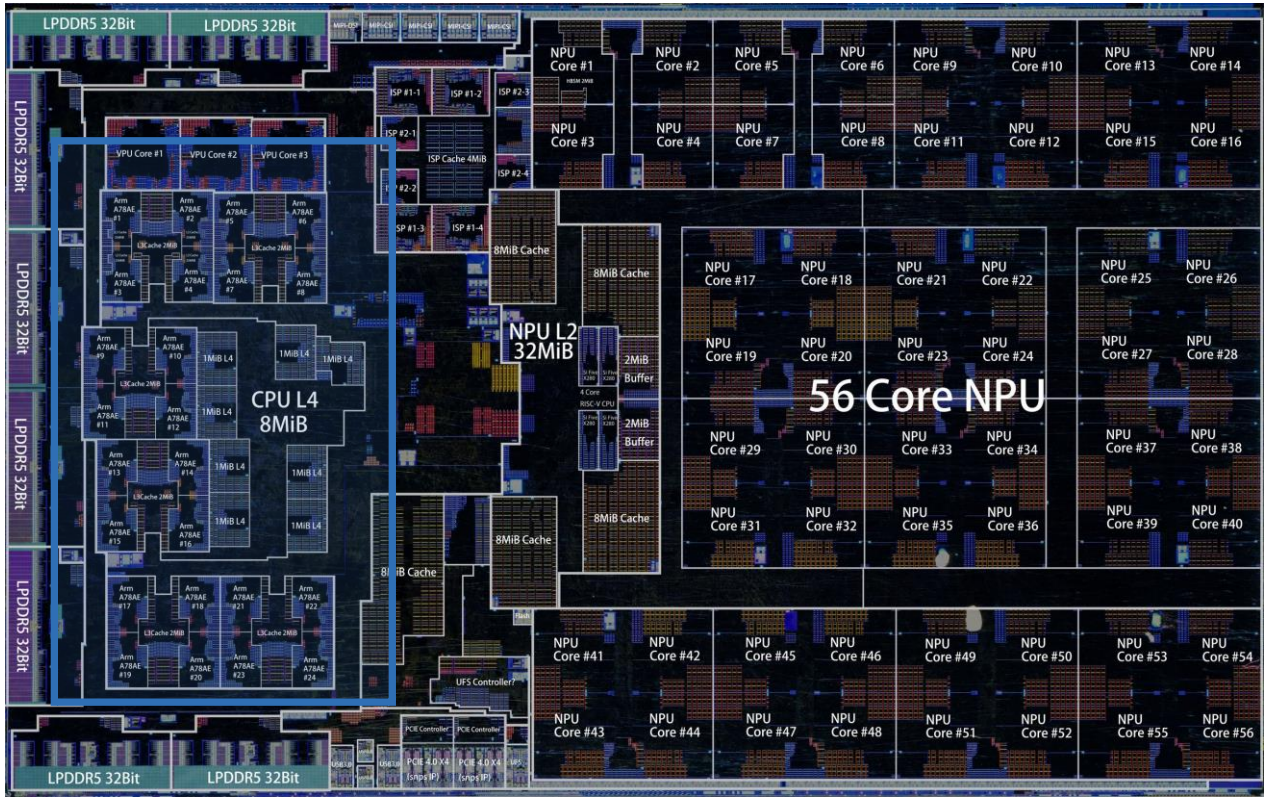
On-Chip Analysis



Remove Metal-Layers

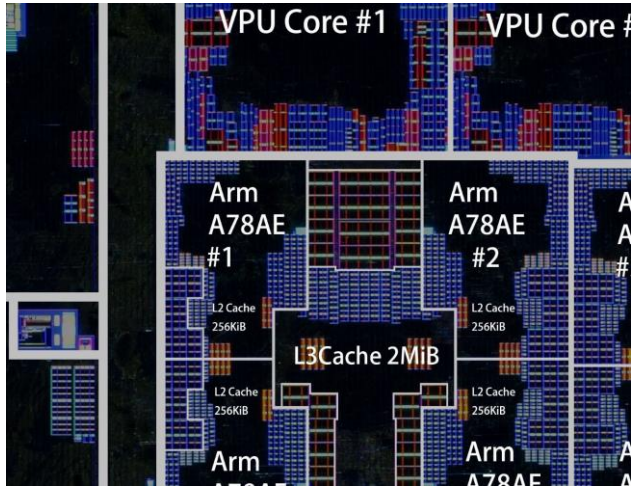


On-Chip Analysis - CPU Subsystem



24-core CPU block (die left)

24 cores - 6 clusters - 4x Arm A78AE



One cluster: 4x A78AE + shared 2 MiB L3

24 cores

6 clusters

4x per cluster

Single A78AE core	**≈ 0.9 mm²**
4-core cluster	**5.088 mm²**
CPU array (total)	**49.796 mm² - 12.12% die**
Clock / perf	**2.3 GHz - ≈ standard A78**

Arm Cortex-A78AE - the automotive workhorse

A78AE

Arm Cortex-A78AE

Released	**Sept 2020**
Segment	**Automotive (split-lock)**
Safety	**ASIL-D capable**
Lineage	**Functional-safety A78**
In service	**~6 years**

Same IP also ships in

- **Qualcomm** SA8295 / SA8540 / SA8530
- **Qualcomm** SA8255 / SA8770 / SA8775 / SA8650P
- **NVIDIA** Orin X
- **Samsung** Exynos Auto V920
- **Black Sesame** A2000
- **Horizon** Journey 6 (J6) series

Same core IP - physical area varies with the process node.

On-Chip Analysis - Process Matters

Same A78AE core, two process nodes

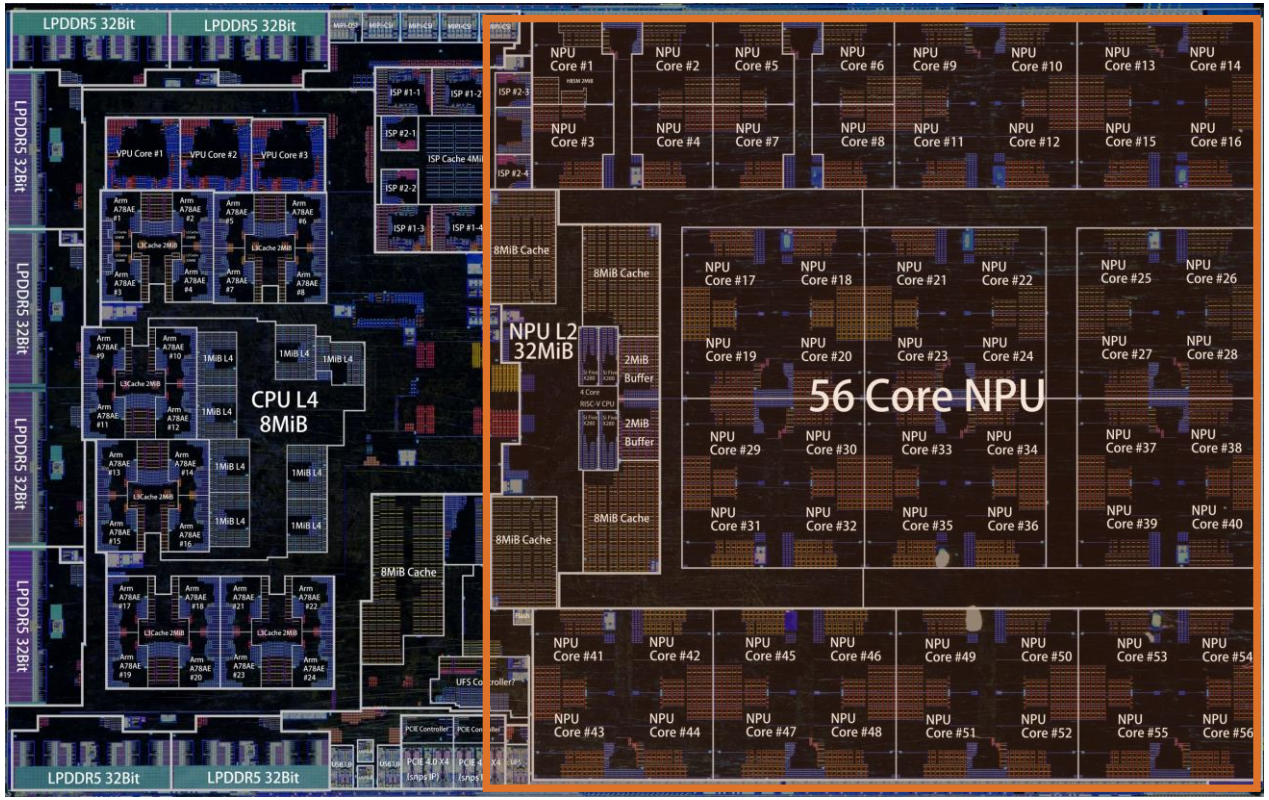
NVIDIA Orin X
Samsung 8 nm
60.92 Mtr/mm²
2.6 mm²
per core

Li-Auto M100
TSMC N5 family
higher density
0.9 mm²
per core

33% of Orin X core area

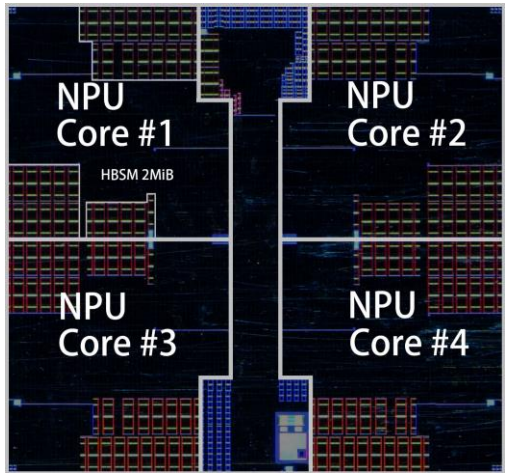
Clock held at 2.3 GHz to keep 24-core thermals in check; A78AE perf ≈ standard A78.

On-Chip Analysis - NPU Subsystem



NPU dominates the die right

14 TPB clusters x 4 tensor units



NPU array - 4 tensor units per cluster

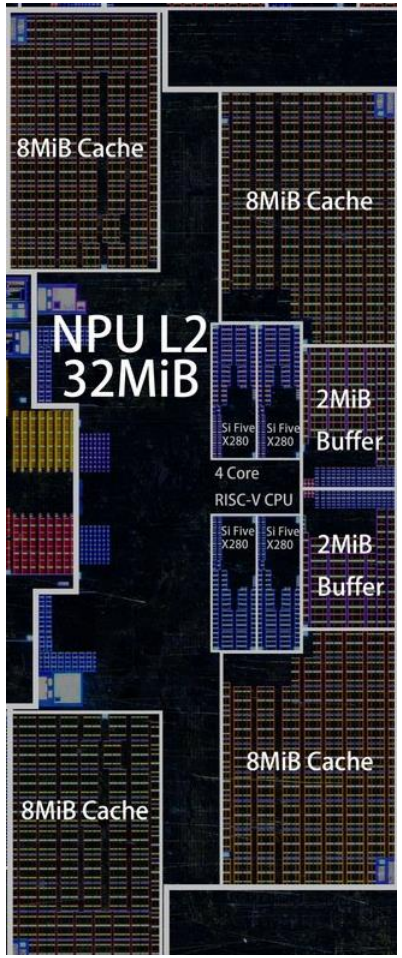
14
TPB clusters

56
tensor cores

2 MiB
HBSM/core

Architecture	**14x TPB + central CCB**
Compute cores	**14 x 4 = 56 cores**
Per-core buffer	**2 MiB HBSM**
Source	**M100 academic paper**

On-Chip Analysis - NPU Control & Memory



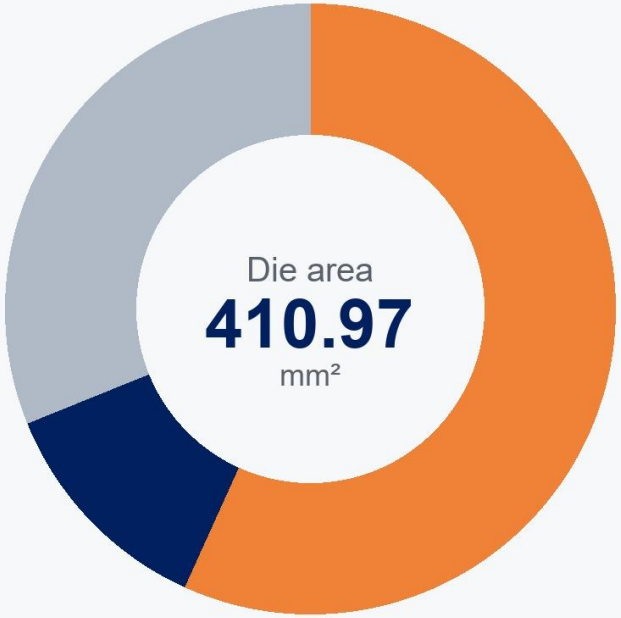
CCB sits at the center of the 32 MiB NPU L2

A RISC-V brain runs the 56 cores

32 MiB	4x	0.46 mm²
NPU L2	SiFive X280	per core

Control module (CCB)	**4-core SiFive X280**
RISC-V IP	**released 2022**
Embedded in	**32 MiB NPU L2**
NPU subsystem total	**233.28 mm²**
Share of die	**56.76%**

On-Chip Analysis - Where the Silicon Goes



Die-area budget by block

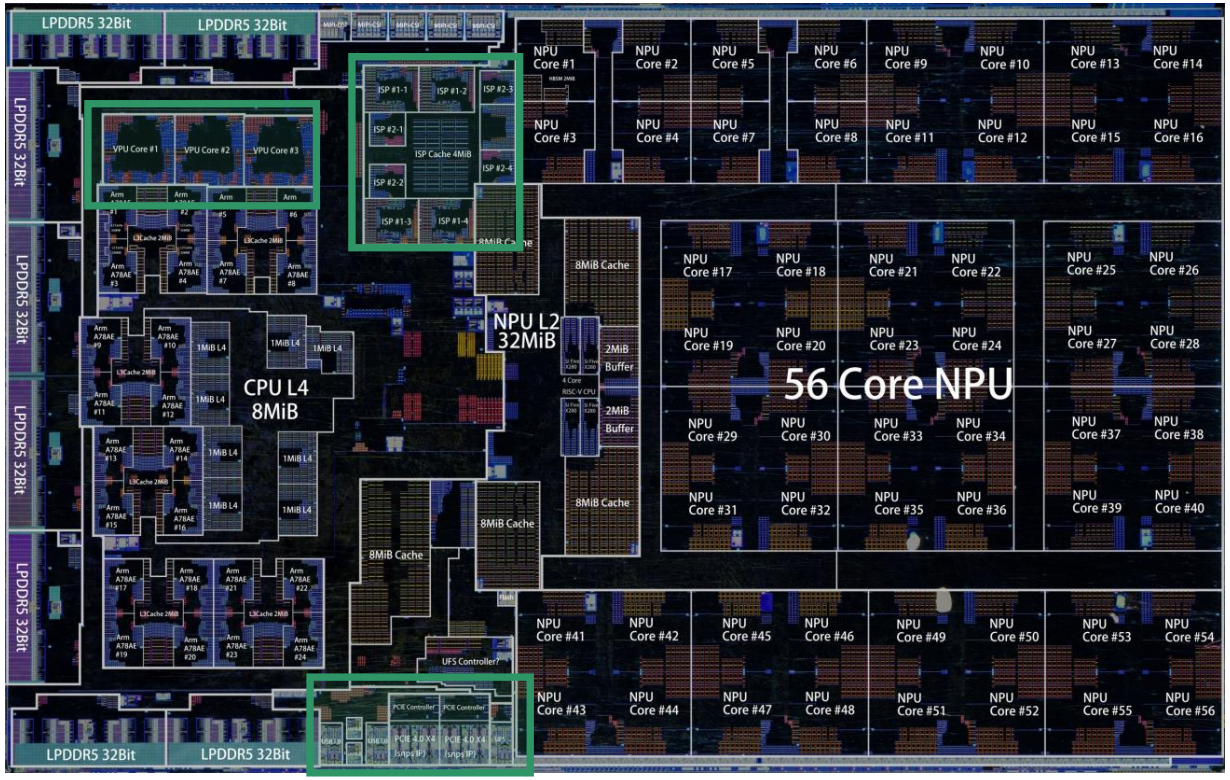
NPU subsystem	56.76%
CPU subsystem	12.12%
Other logic / IO / cache	31.12%

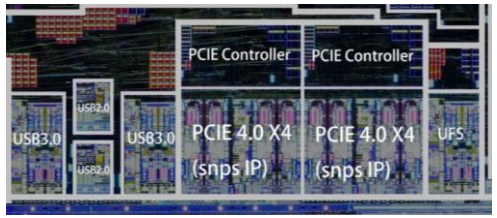
4.68x

NPU silicon cost vs the CPU

The NPU - not the CPU - is the silicon cost center of this chip.

On-Chip Analysis - ISP - VPU - I/O





I/O row: USB - UFS - PCIe (Synopsys IP)

ISP - Image Signal Processor

4-core ISP architecture
4x MIPI-CSI (4-lane each)
-> up to 16 camera sensors

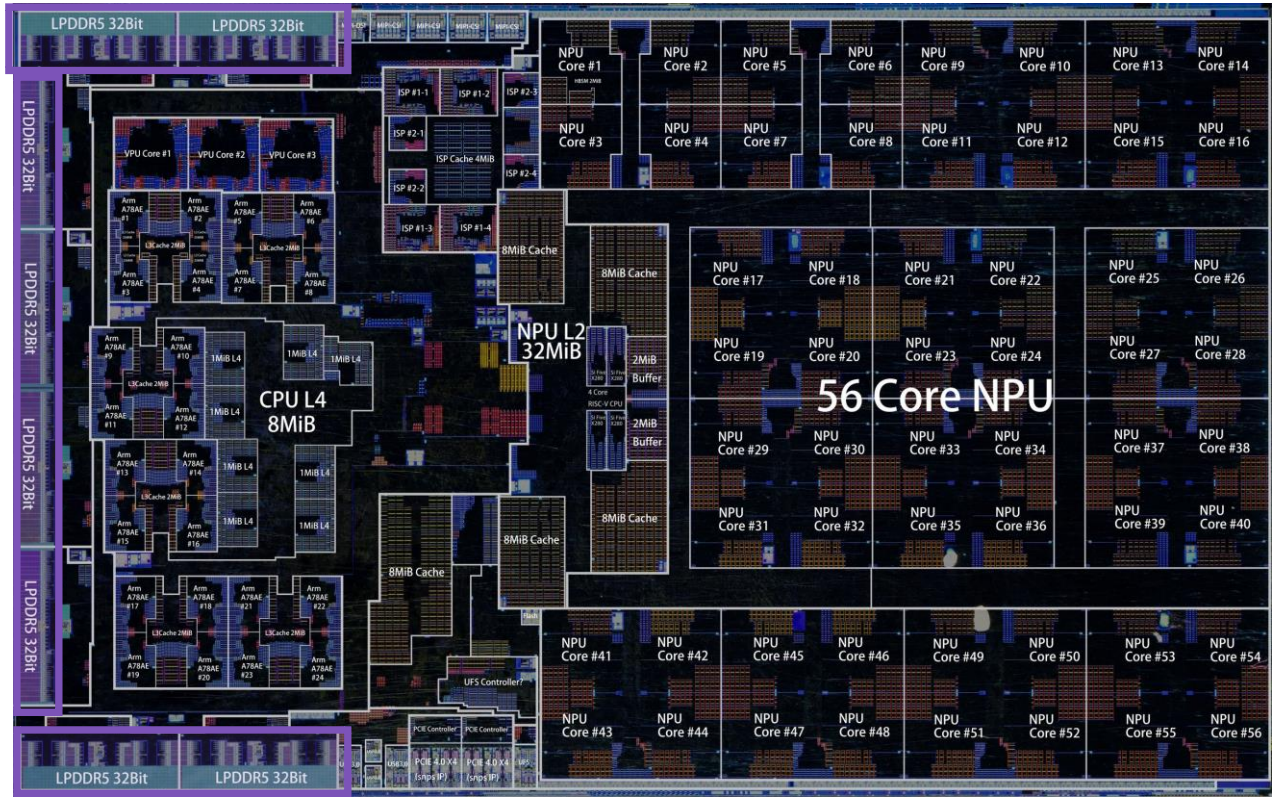
VPU - Video Processor

3-core VPU
1x MIPI-DSI display output

I/O & interconnect

2x USB 2.0 - 2x USB 3.0 - 1x UFS
2x PCIe 4.0 x4 -> repurposed as 10 GbE
Synopsys universal I/O (cf. SemiDrive 龙鹰一号)

On-Chip Analysis - Memory Subsystem



8x LPDDR5 controllers ring the CPU clusters

256-bit LPDDR5 memory interface

8	32-bit	256-bit
controllers	each	total bus

Per controller	**32-bit LPDDR5**
Channel count	**8 x 32-bit**
Aggregate bus	**256-bit**
Placement	**around the CPU clusters**