Samsung 2nm Exynos 2600

Processor analyze

V0

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Version of this Report

Version	Date	Updates	Author
V0	2026/04/22 08:42	Make Processor analyze in SF2	Kurnal
V0.1	2026/05/05 02:37	工艺分析基本写完了	Kurnal
V0.2	2026/06/03 18:29	打水印+发布	Kurnal

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Overview

Intel Panther Lake

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Physical Analysis

BOM Data

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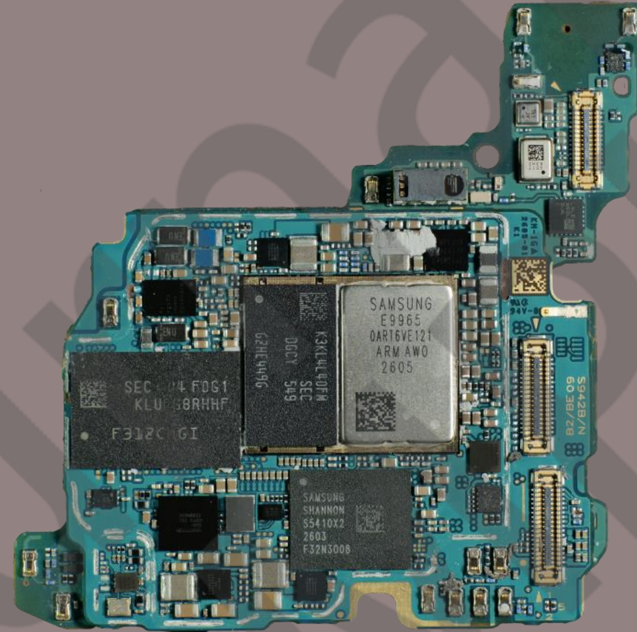
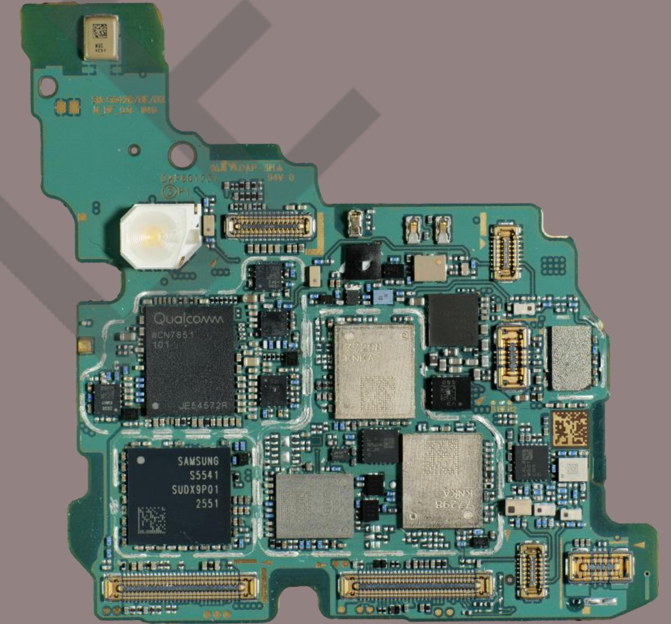
Mother Board-View



Galaxy S26 MB Topside View



Galaxy S26 MB Backside View

Exynos 2600 will be limited to Korea and Europe

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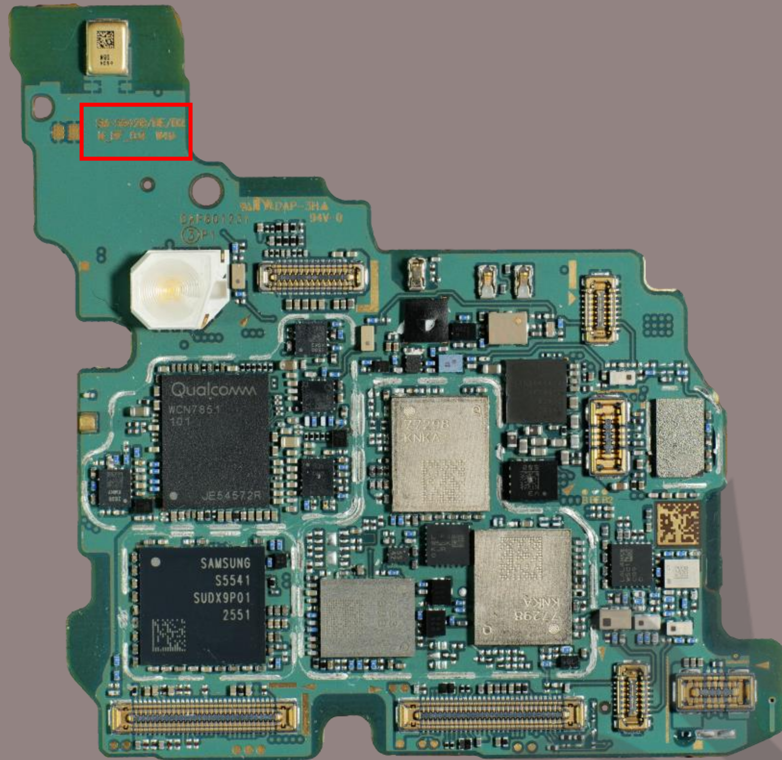
Mother Board-PCB Mark



Galaxy S26 MB Backside View

SM-S942B/BE/B2 —— Samsung Galaxy S26 5G

M-RF-0.9-W49 —— Main-RF Vision 0.9

DAP601231 —— Samsung Galaxy S26 5G

3-P1 —— Panel Position 3-Phase 1

PCB Made by DAP-Korea

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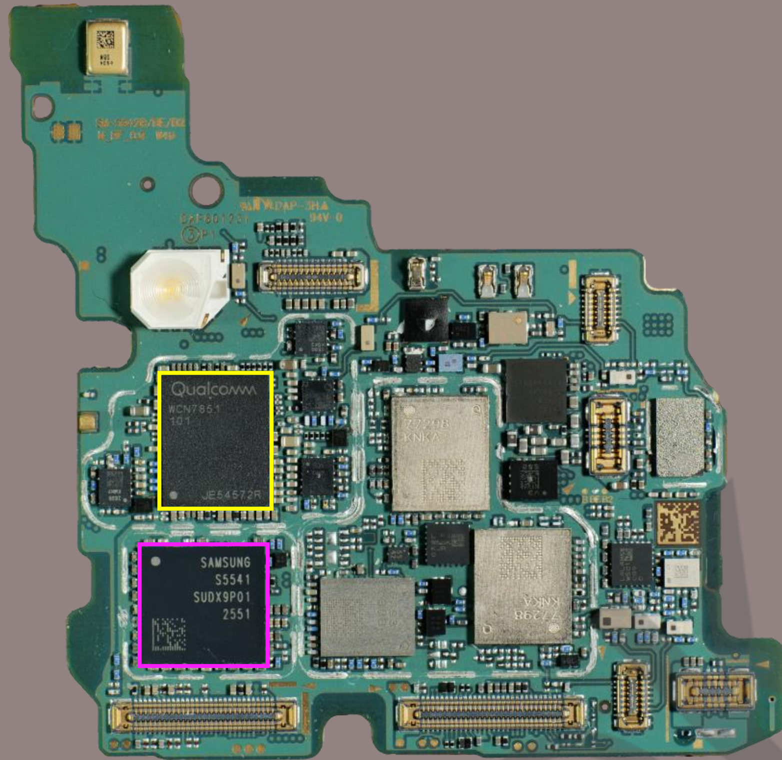
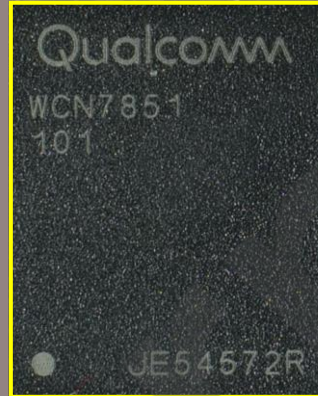
Mother Board-BOM Mark



Galaxy S26 MB Backside View



Galaxy S26 WIFI/BT

WIFI/BT-Mark

Quacomm —— Made By Qualcomm
WCN7851 —— FastConnect 7800 WIFI 7 & BT 5.4
JE546572R —— J= Made By Samsung
E= Package By ASE Taiwan
546= Made in Year 2025 Week 46

RF Transceiver

Samsung —— Made by Samsung
S5541 —— Samsung RF Transceiver
SUDX9P01 —— Lot Number
2551 —— Made in Year 2025 Week 51

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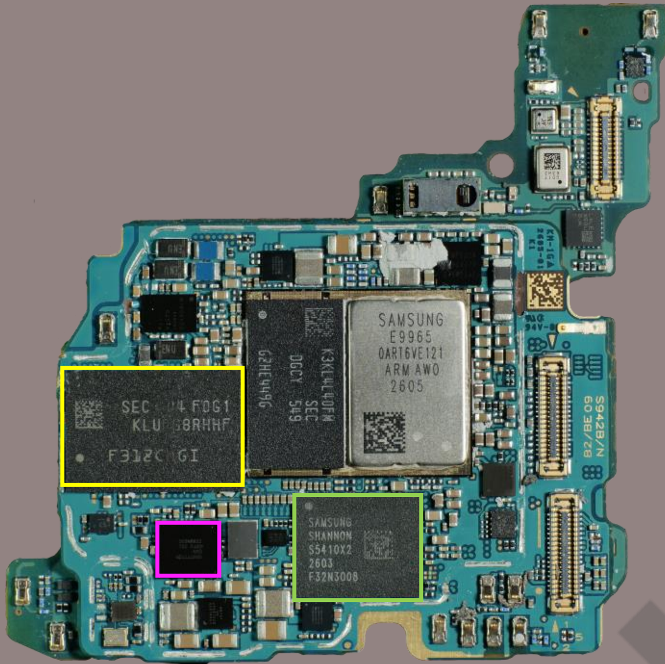
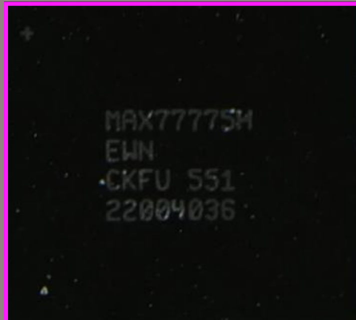
Mother Board-BOM Mark



Galaxy S26 MB Topside View

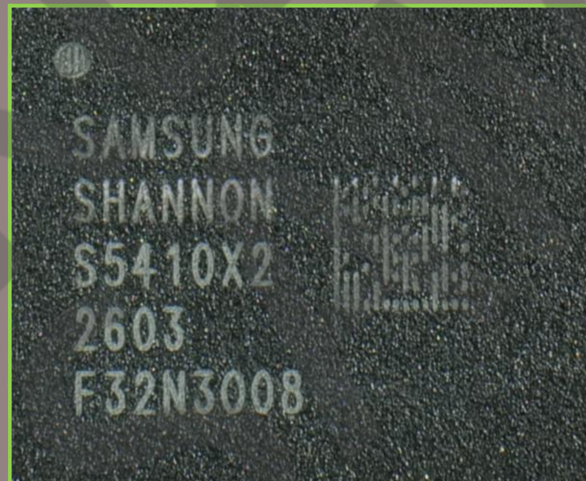


Maxim Integrated

MAX77775H

is a DC-DC
Fast charging IC

Galaxy S26 UFS Mark



Galaxy S26 BaseBand

UFS-Mark

SEC 604 F0G1	Made in Year 2026 Week 04
KLUFG8RHHF	UFS4.0 512GByte
F31ZCHGI	Lot Number

BaseBand-Mark

Samsung	Made by Samsung
Shannon	Samsung Baseband Product Line
S5410X2	name S5410,Verson 2
2603	Made in Year 2026 Week 03
F32N3008	Lot Number

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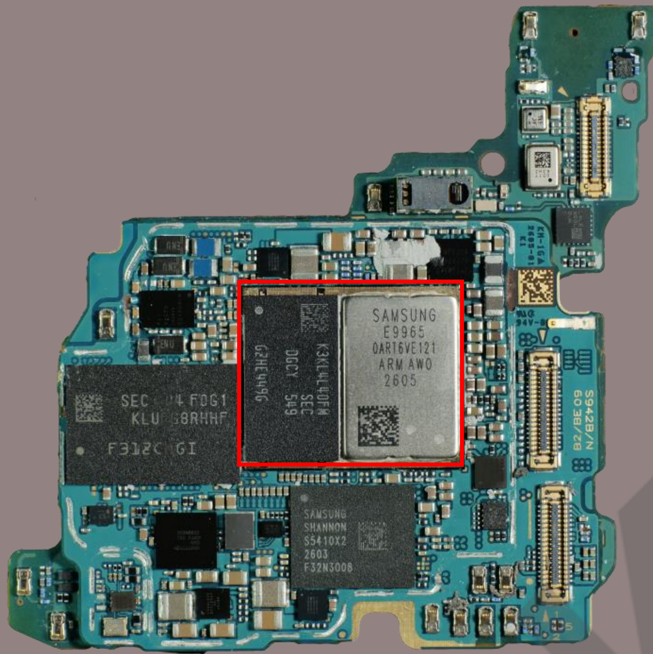
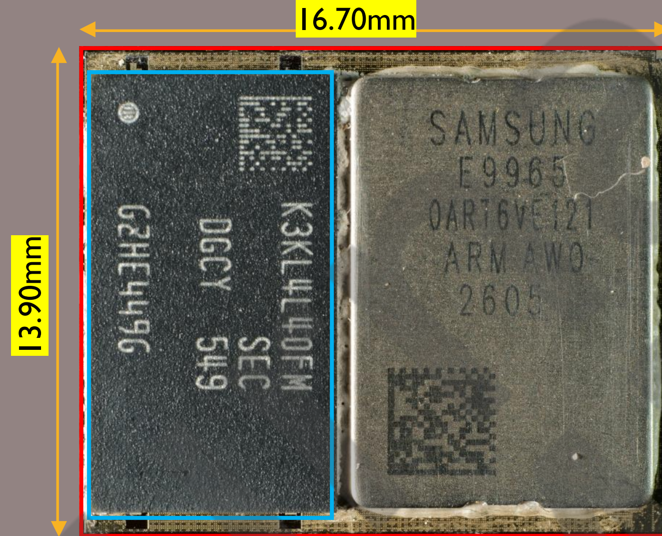
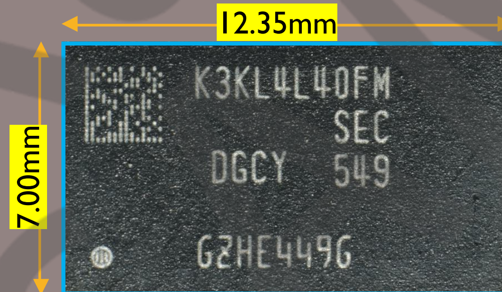
Mother Board-BOM Mark



Galaxy S26 MB Topside View



Galaxy S26 Exynos 2600 chip



Galaxy S26 DRAM-LPDDR

Chip-TopMark

Package size: 16.70mm x 13.90mm

Samsung	Samsung Foundry
E9965	S5E9965=Exynos 2600
0AR76VE121	Lot number+ Version 121
ARM AW0	Arm IP
2605	Made in Year 2026 Week 05

DRAM-Mark

Package size: 12.35mm x 7.00mm

K3KL4L40FM	Lpddr5x 12Gbyte 9600Mbps
SEC	Samsung DRAM
DGCY	BGA 563
549	Made in Year 2025 Week 49
GZHE4496	Lot Number

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Package Analyze

Exynos 2600

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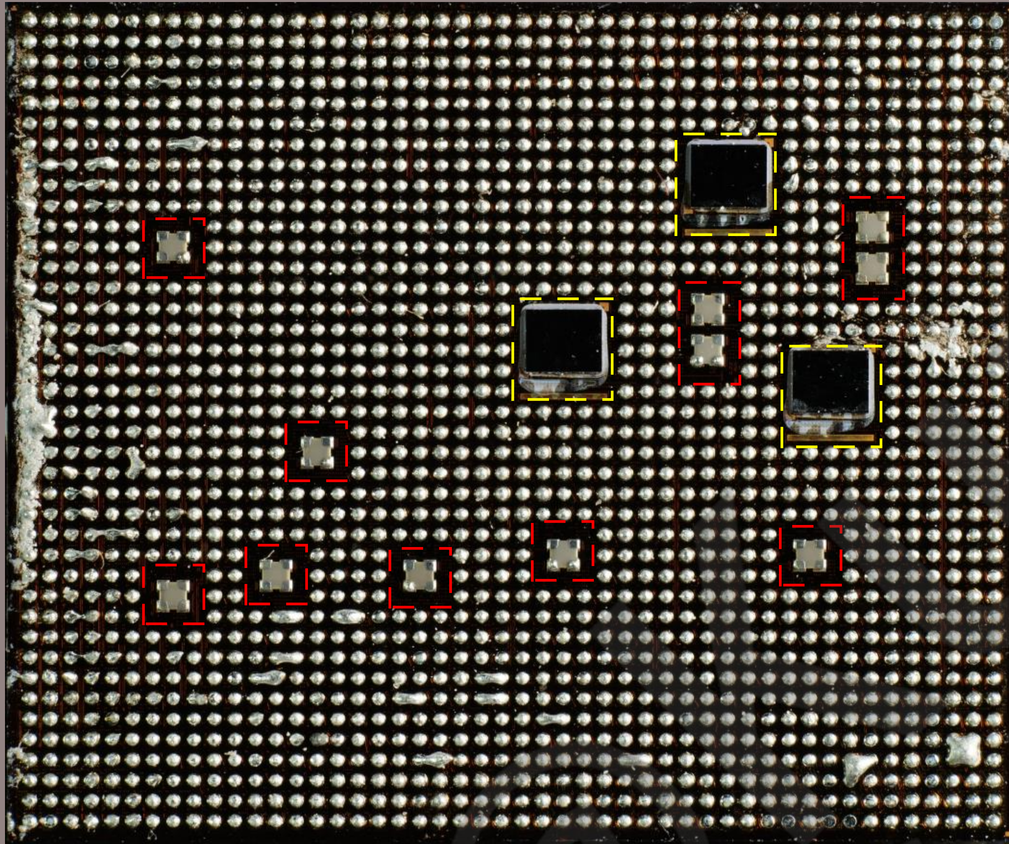
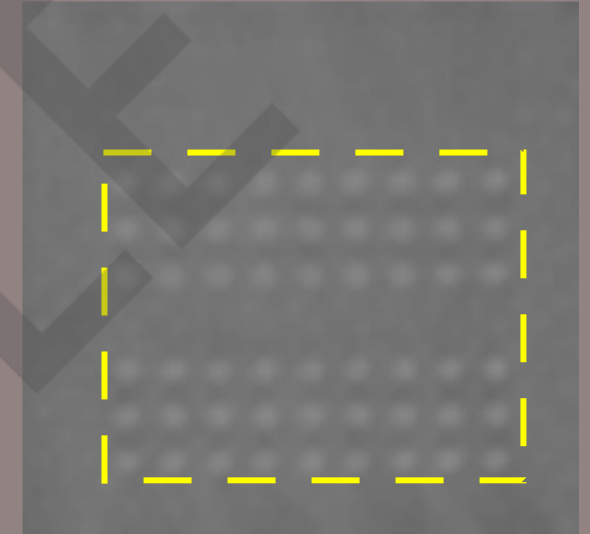
Package Analyze-IPDs



Exynos 2600 Backside

Exynos 2600 Si IPDs

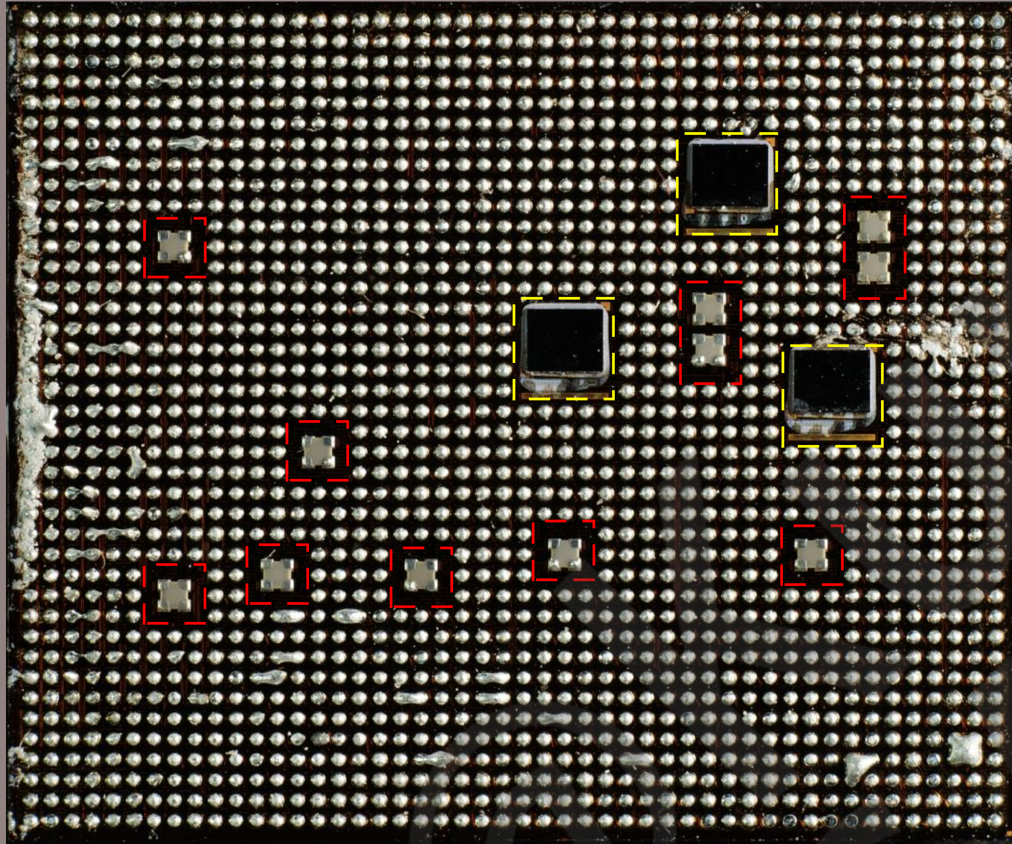


Exynos 2600 Si IPDs pad

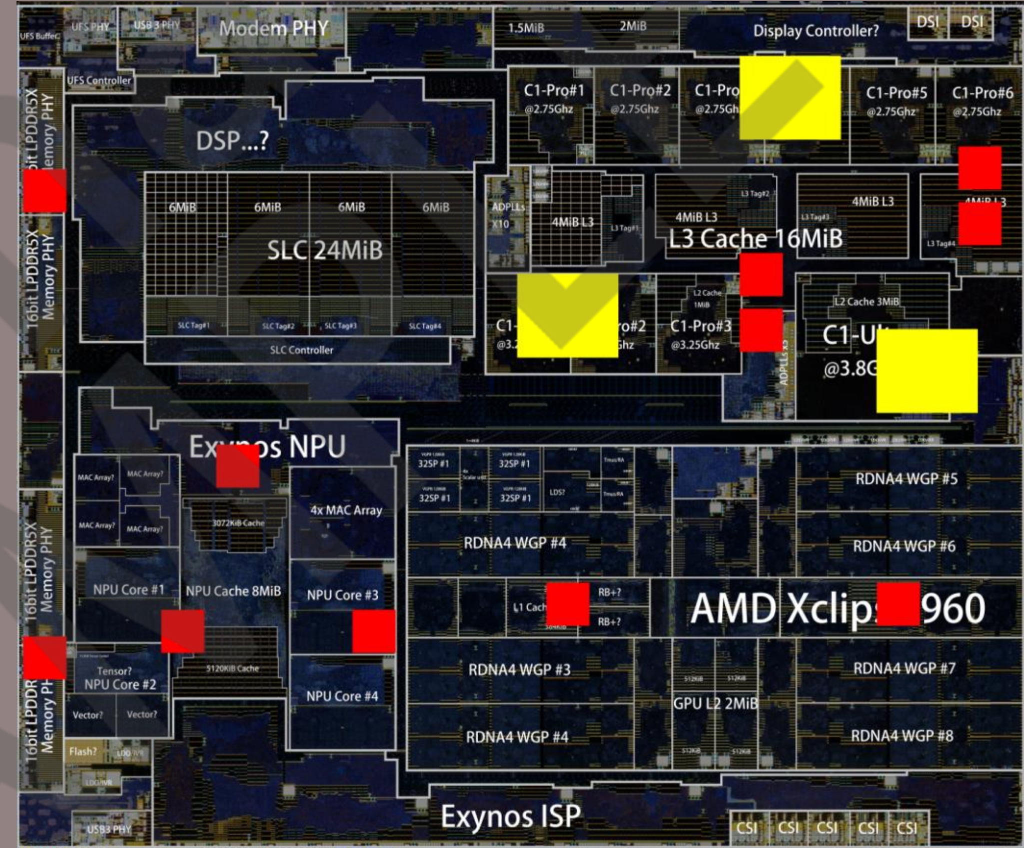
- **MLCCs**: 11 units
- **Si IPDs**: 3 units

- **Si IPDs** pad Nb : 54

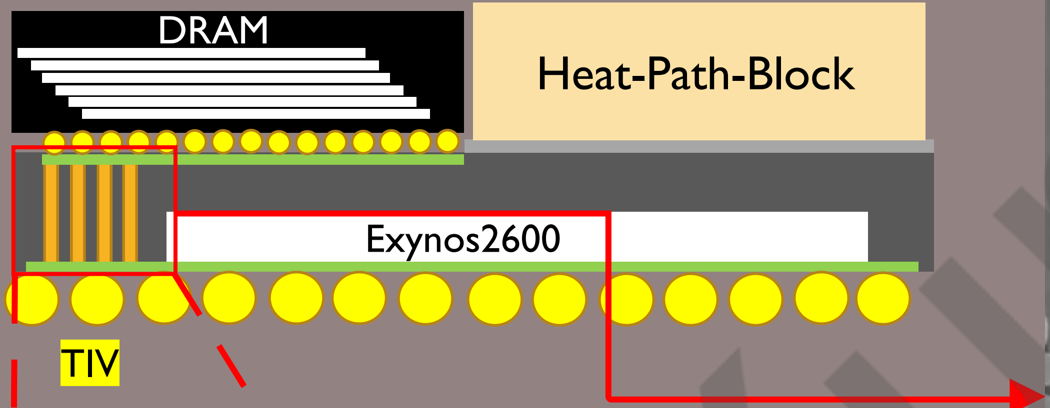
Package Analyze-IPDs

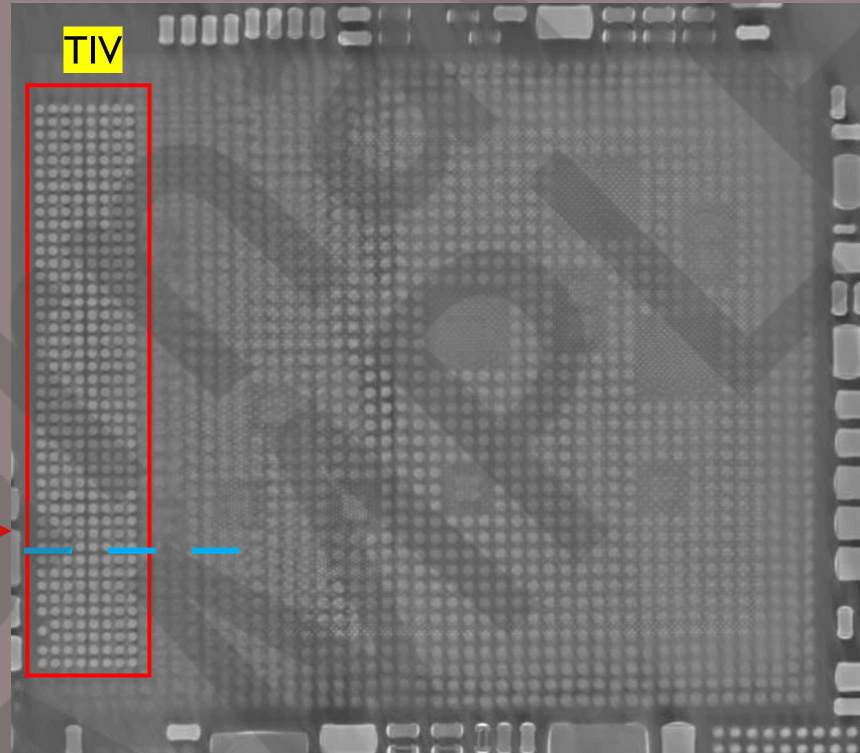


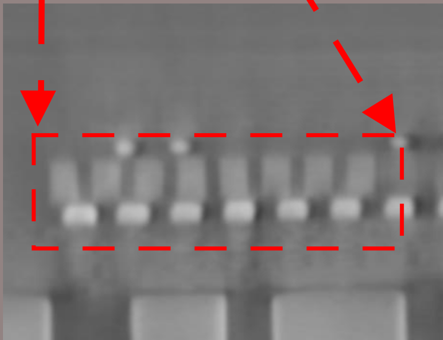
Exynos 2600 Backside



Package Analyze-TIV







All TIVs are arranged on one side

TIV number :350

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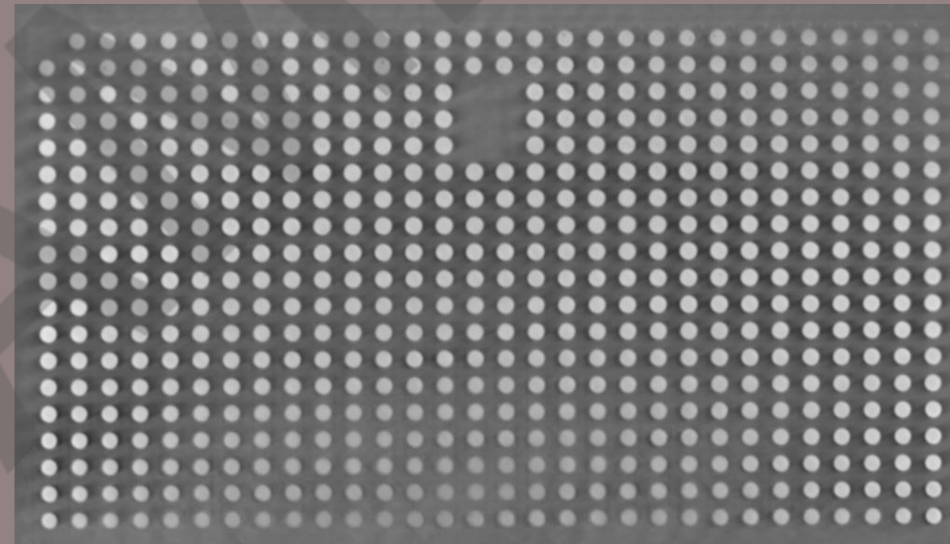
Package Analyze-DRAM Package



Pad number :563

DRAM Die Nb:8

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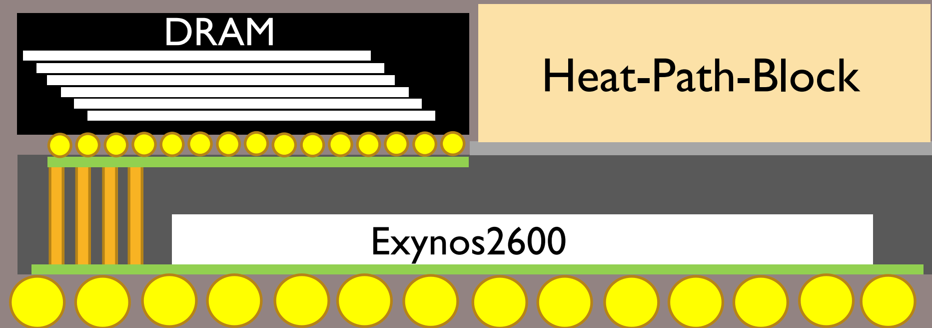

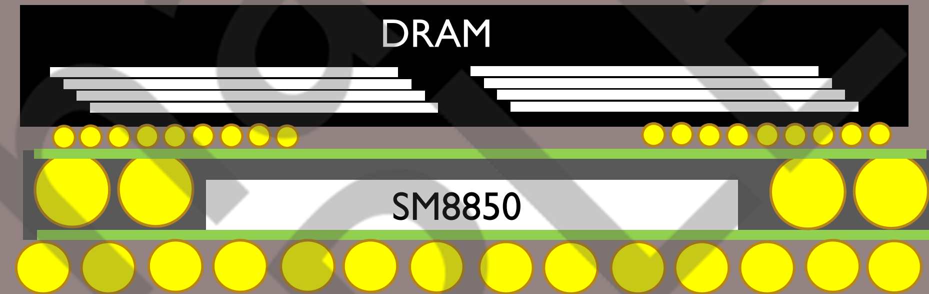

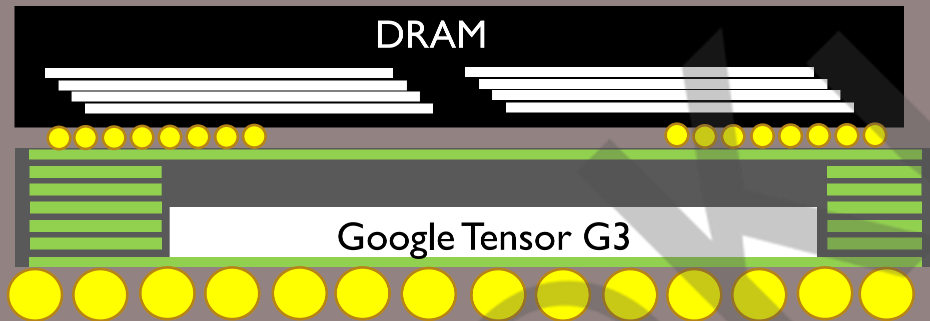

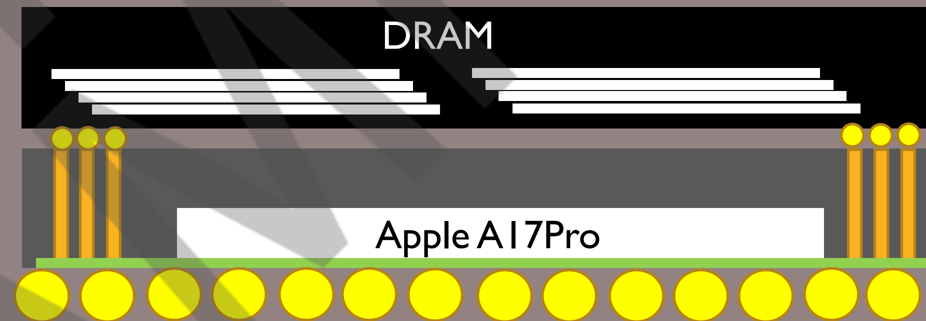

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HPB Analyze

Heat-Path-Block

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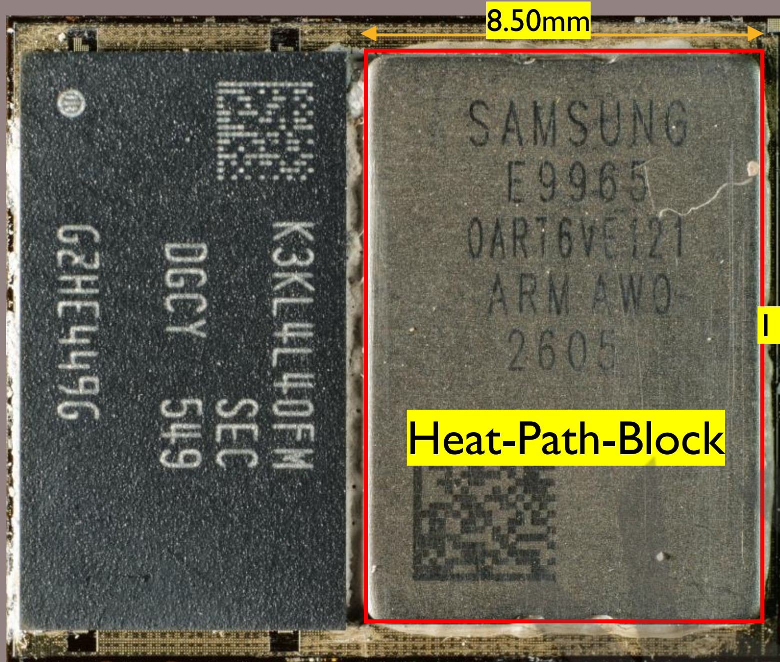
SAMPLE

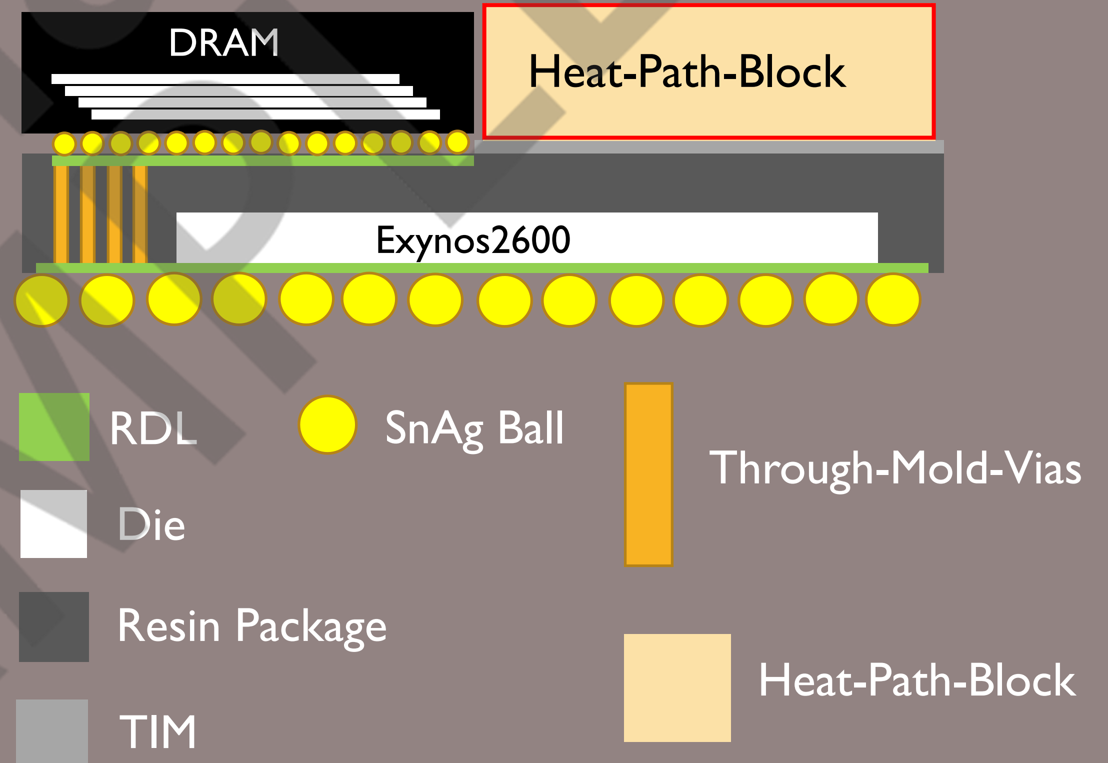
HPB Analyze



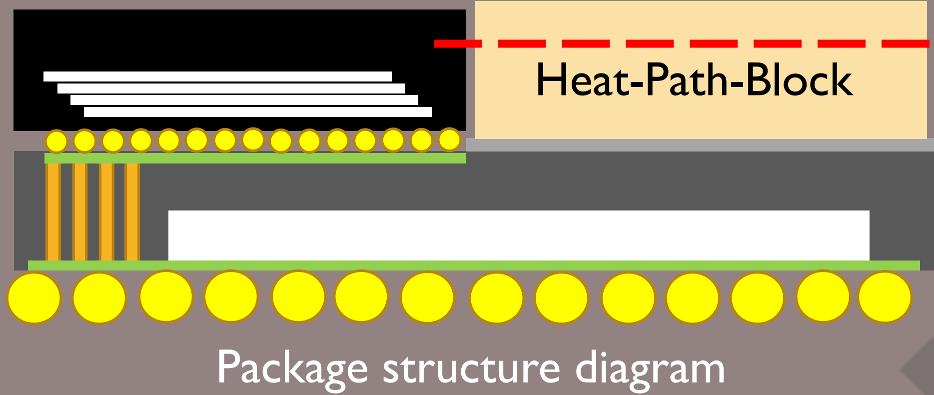
Galaxy S26 Exynos 2600 chip

HPB Field area: 11.21mm x 8.50mm

95.29mm2

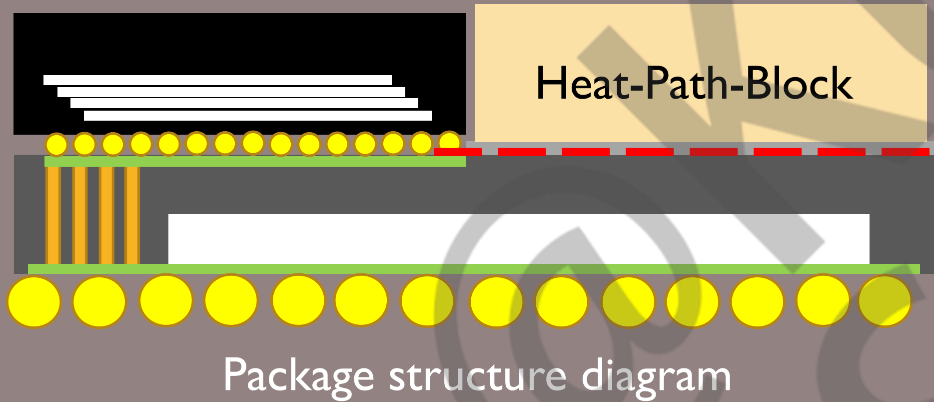


@Kurnal SAMPLE

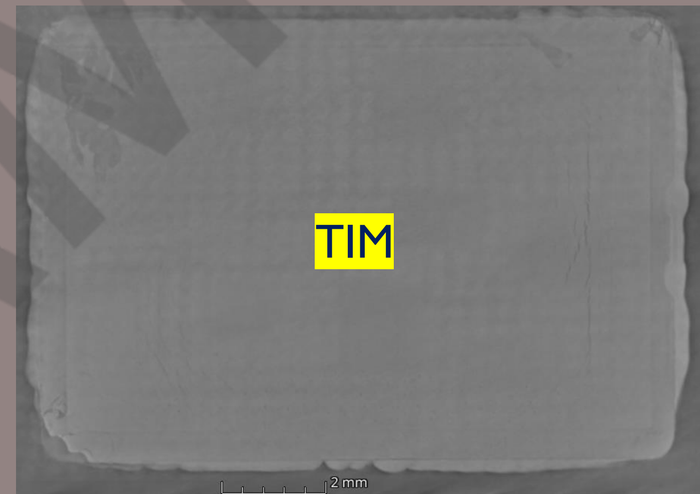


HBM Layers

Package structure diagram



TIM Layers



Package structure diagram

Looks like use Silicone grease For TIM

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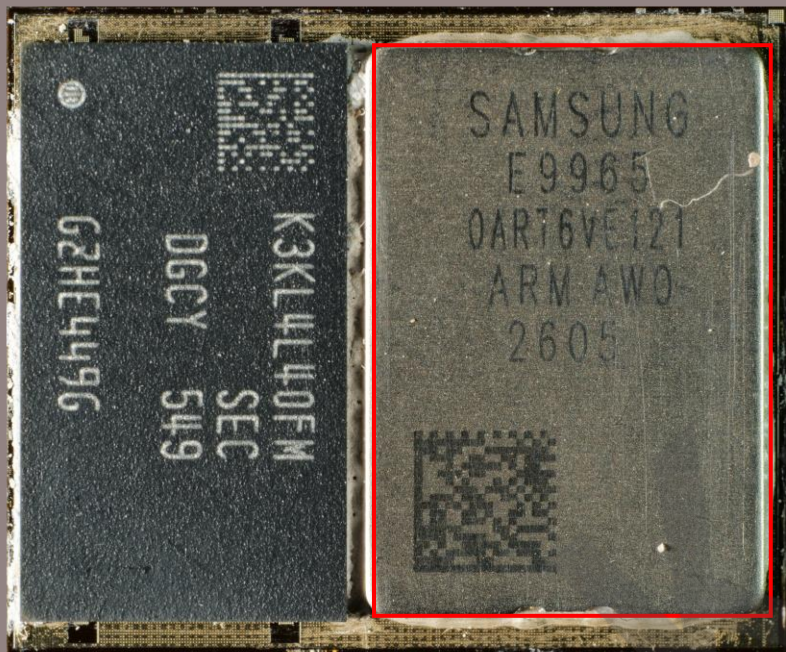
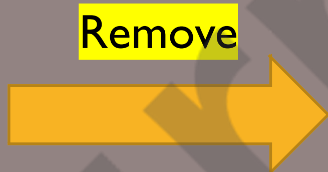
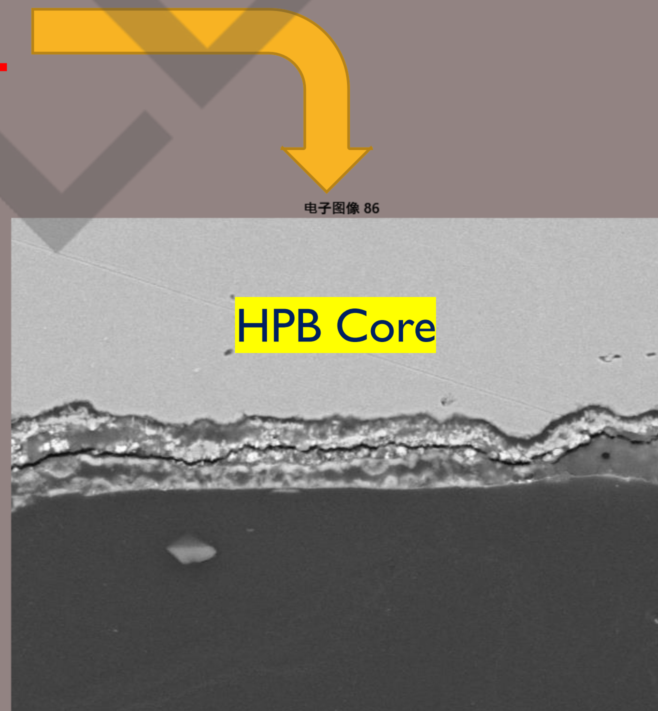
HPB Analyze



Galaxy S26 Exynos 2600 chip



Exynos 2600 HPB



HPB materials need to be confirmed.

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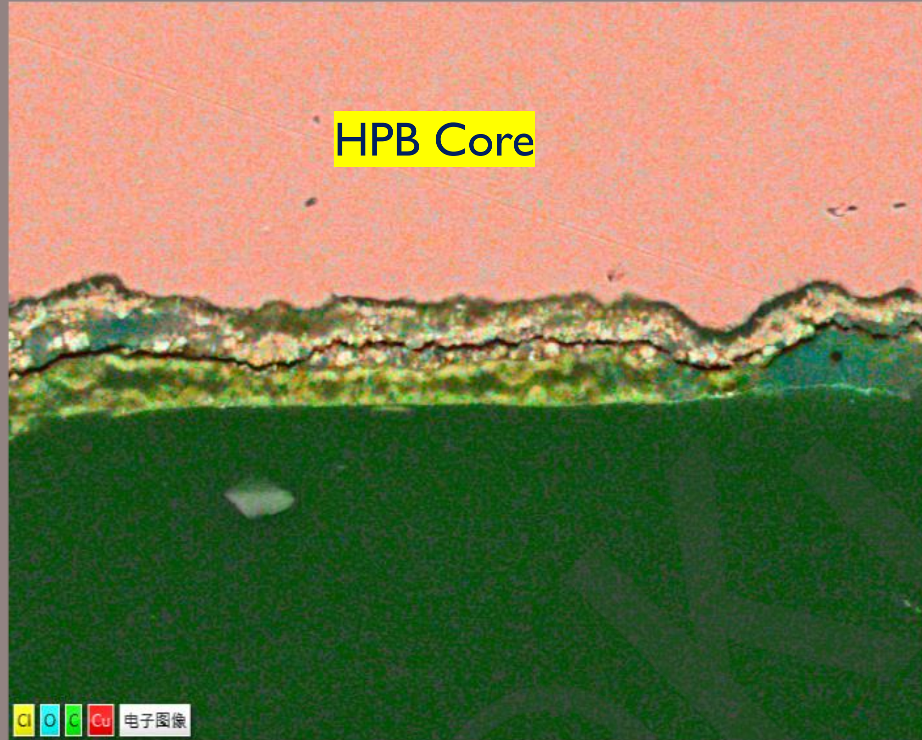
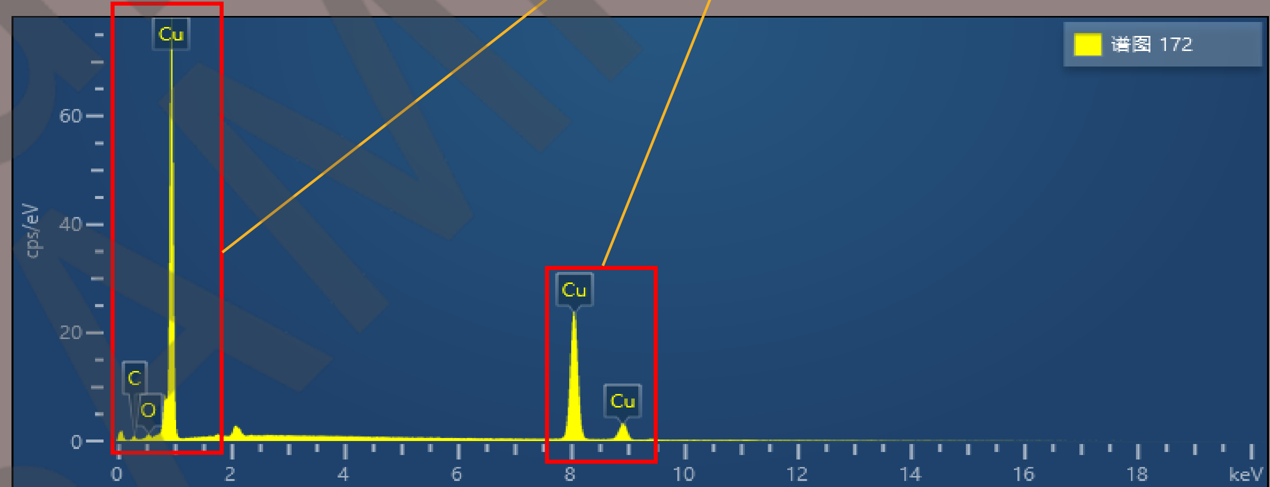


Exynos 2600 HPB Cross EDS



HPB core uses copper elements in its format.

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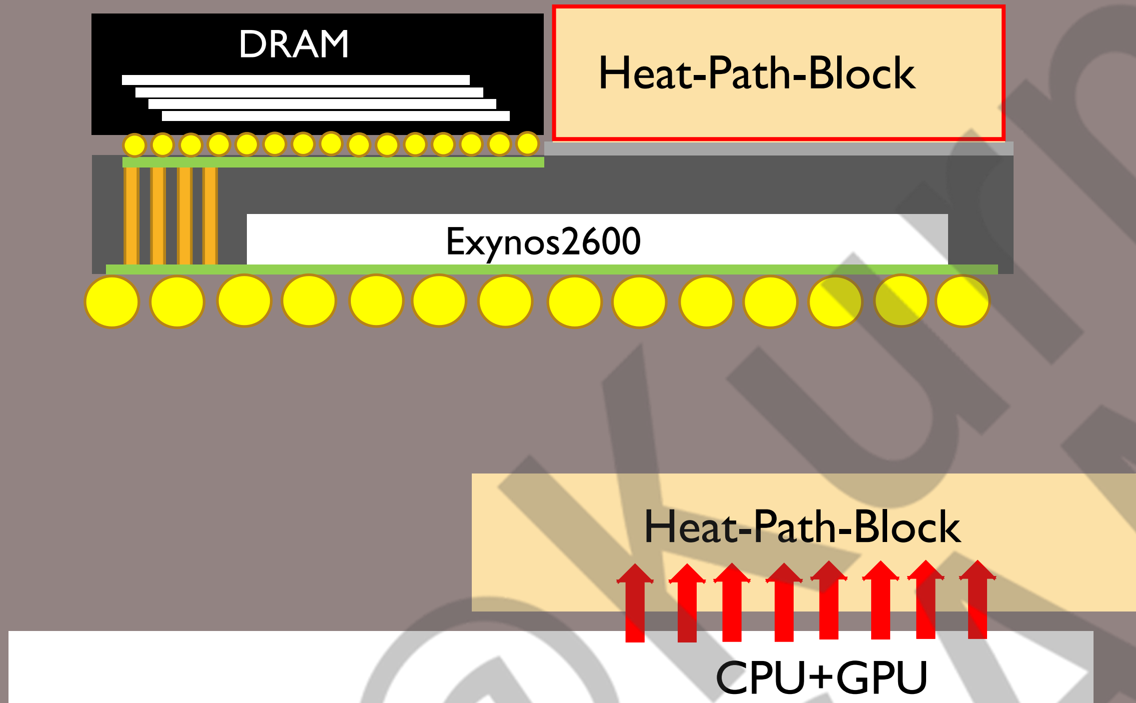

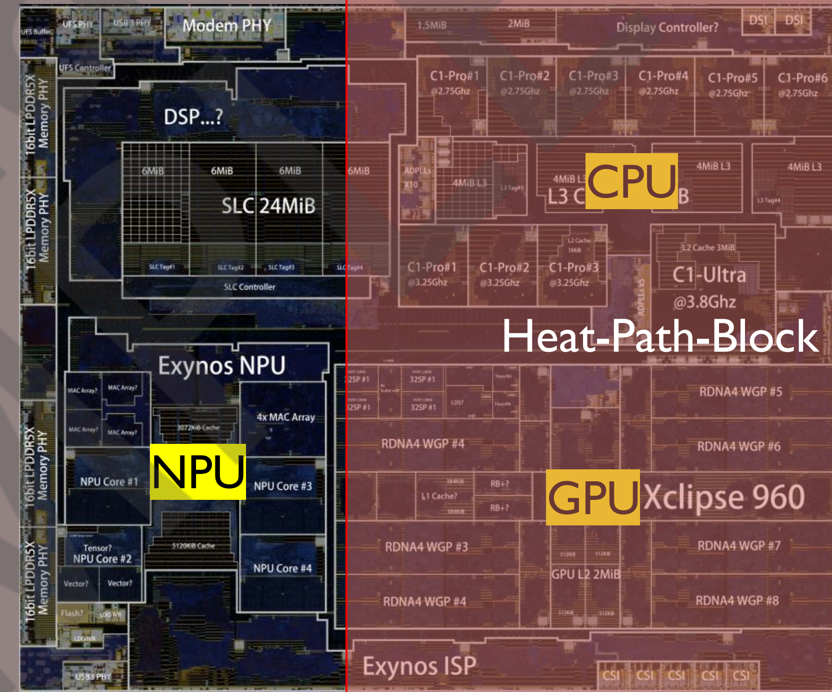

@Kurnal SAMA

Samsung 2nm GAA

Processor analyze

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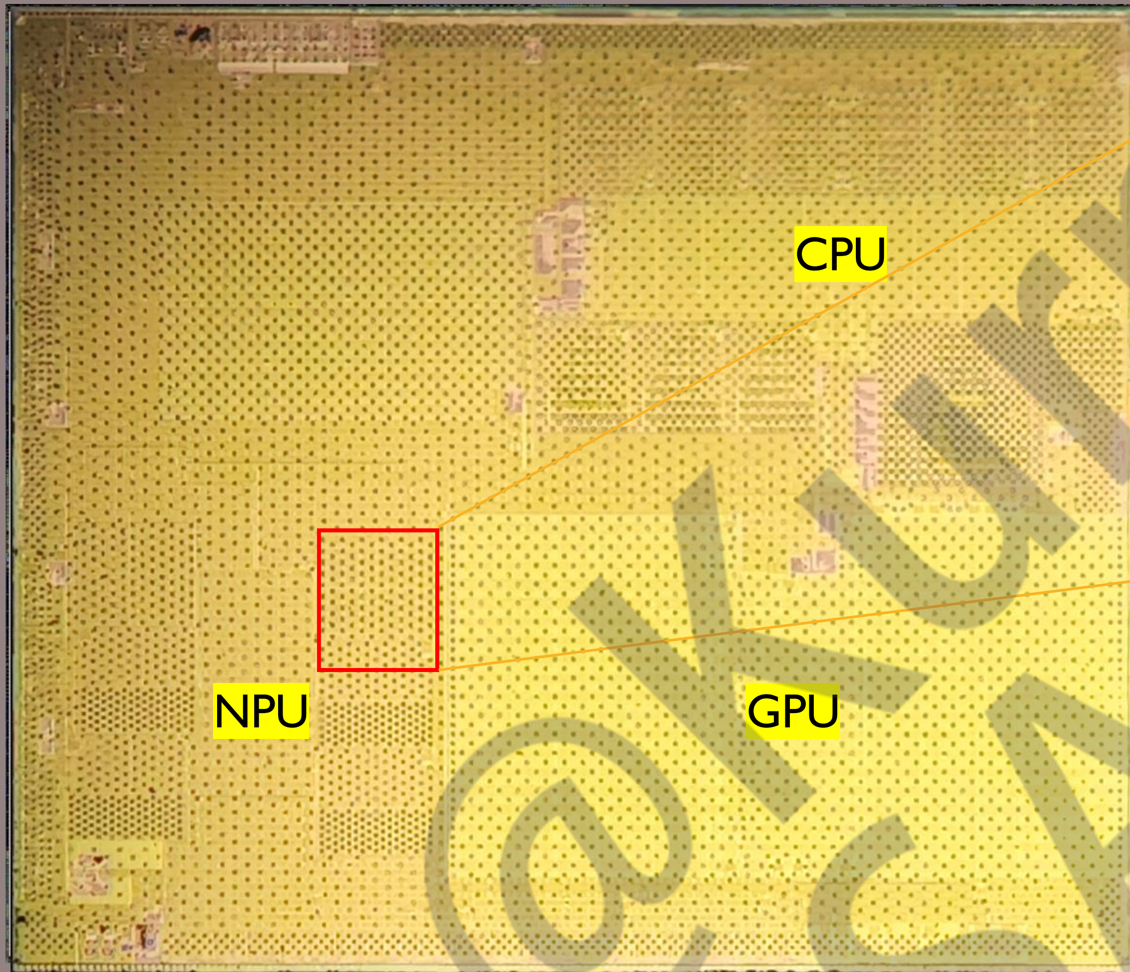
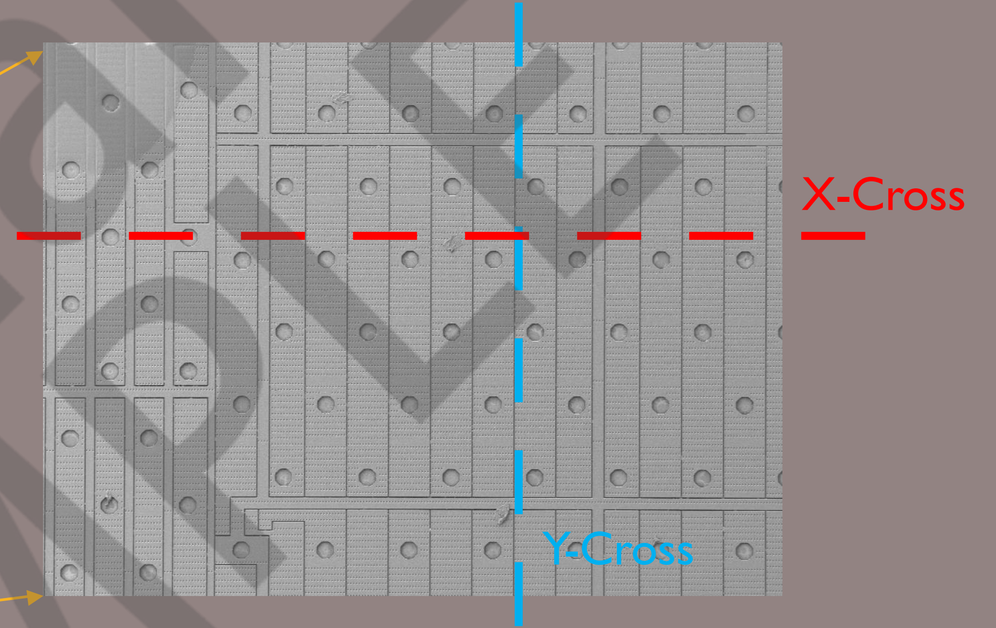
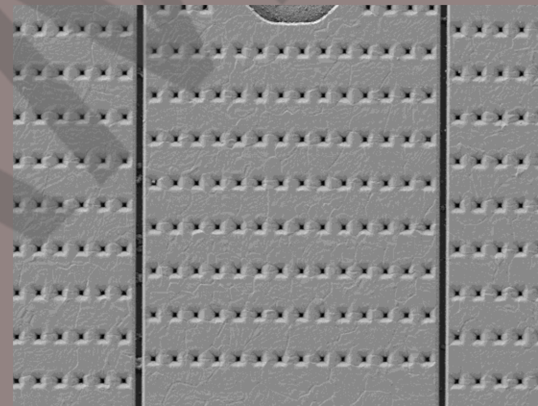
Processor analyze

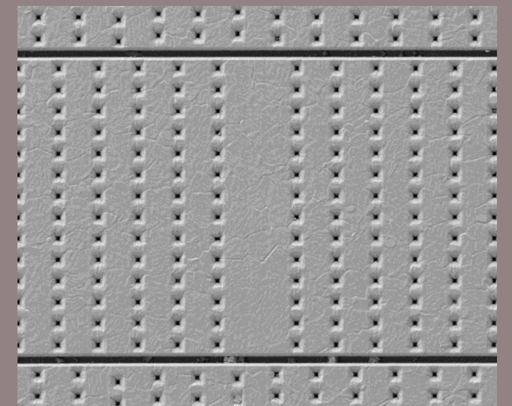


Exynos 2600 Metal Layer Pics





X-Cross



Y-Cross

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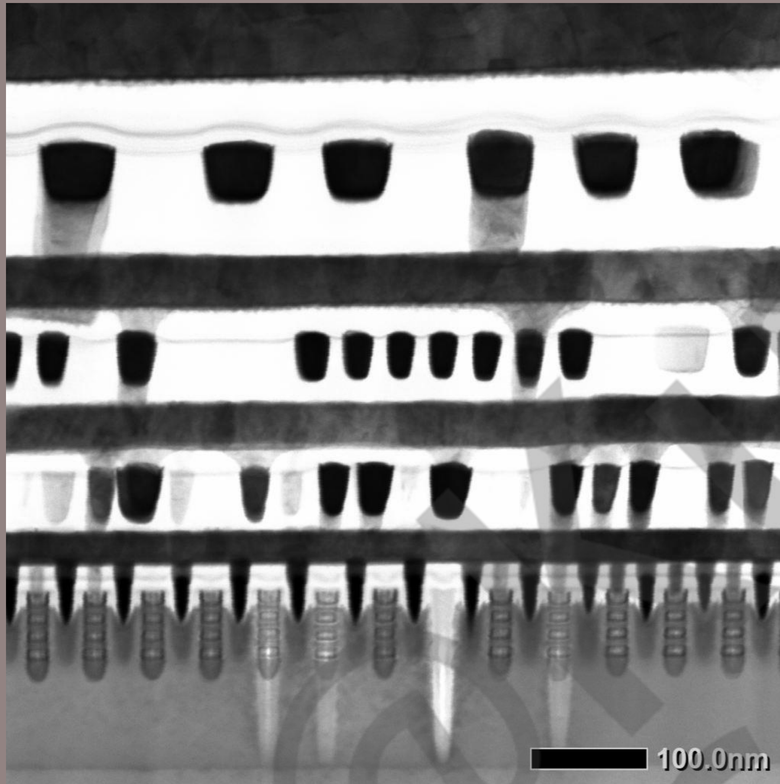
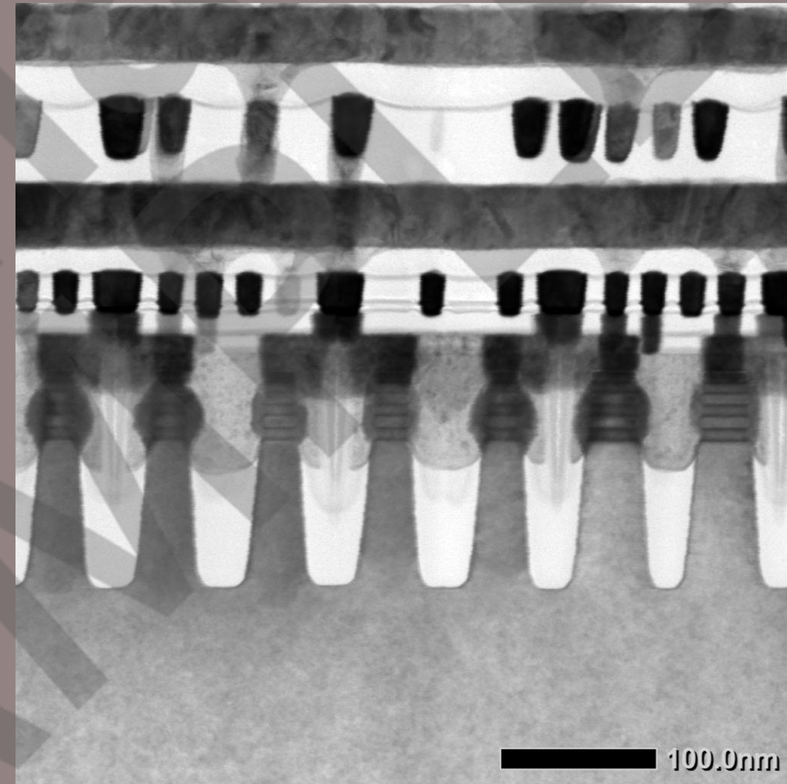
X-Cross

Y-Cross



0421-1 X Cross 2-004



0421-1 Y Cross 1-007

Gate Cross

Sheet Cross

Transistor Analyze

Samsung SF2-Sheet Cross

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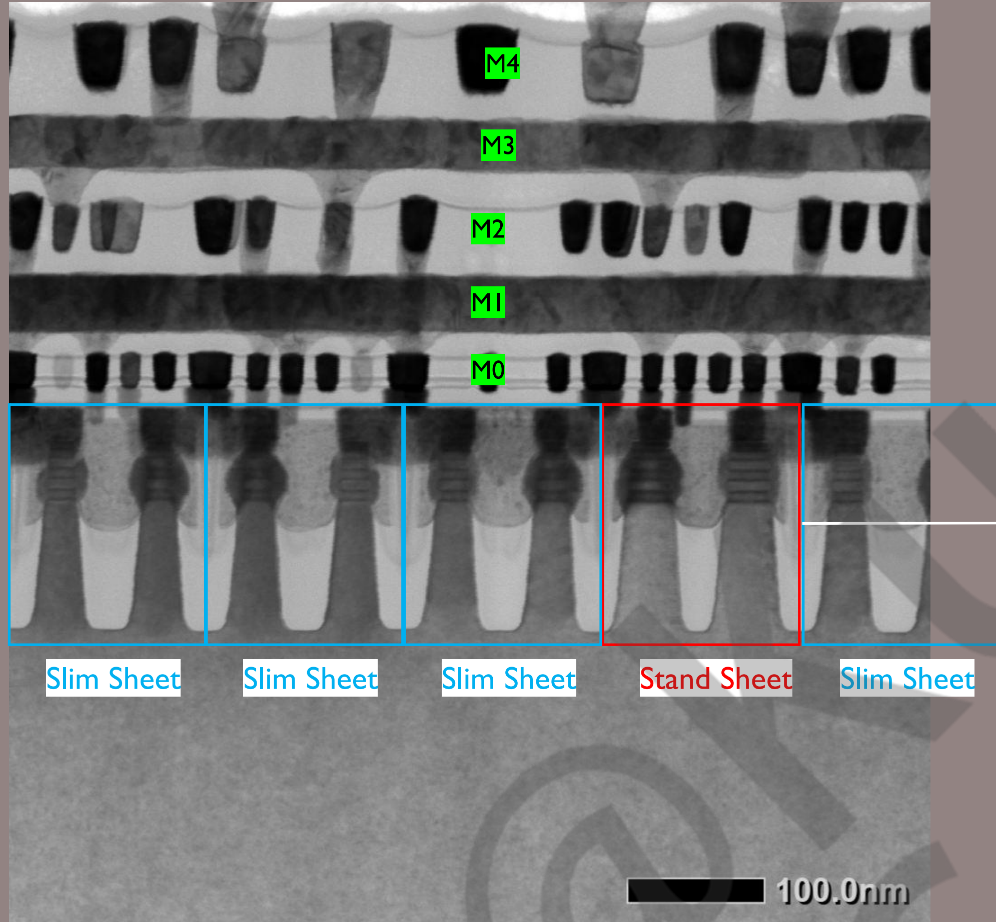
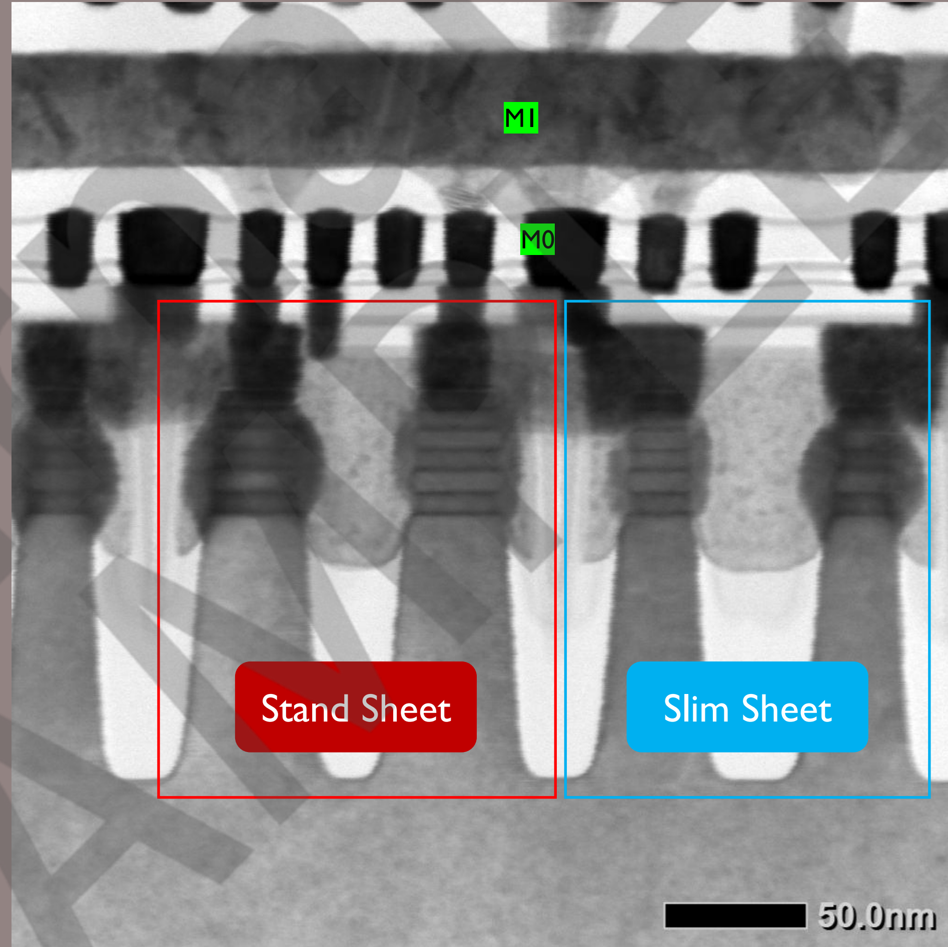
Processor analyze-Sheet Cross

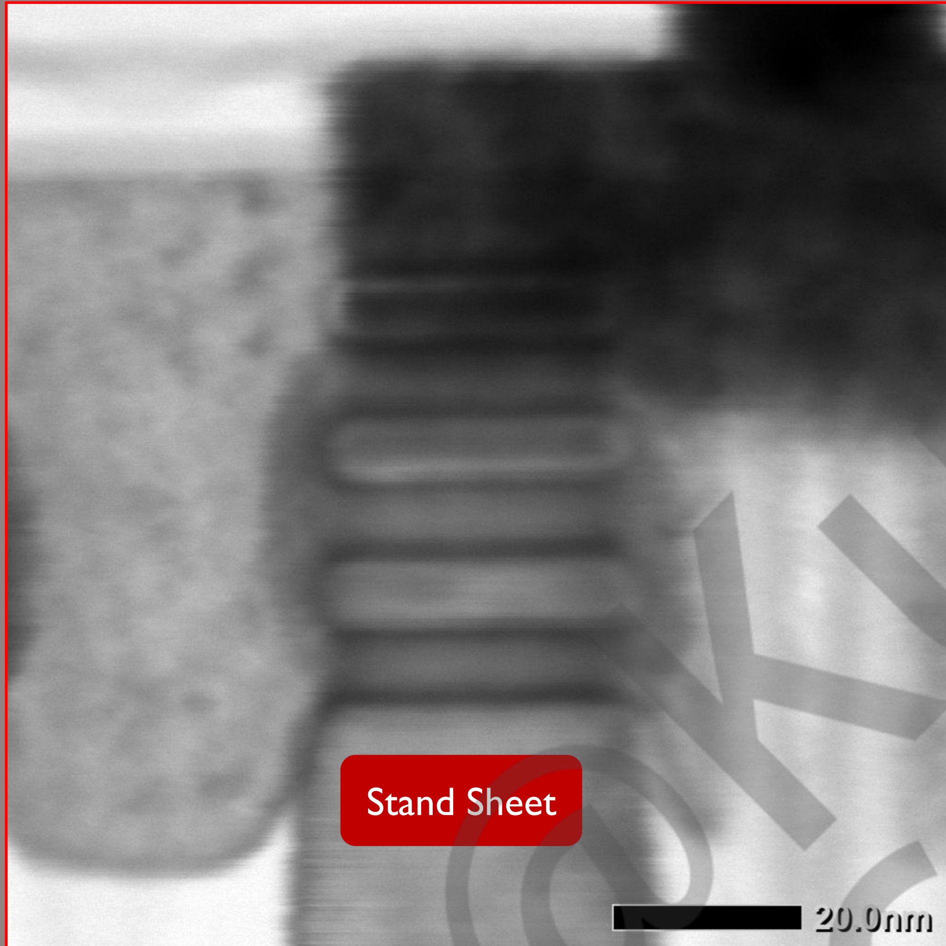


0421-1 Y Cross 1-008

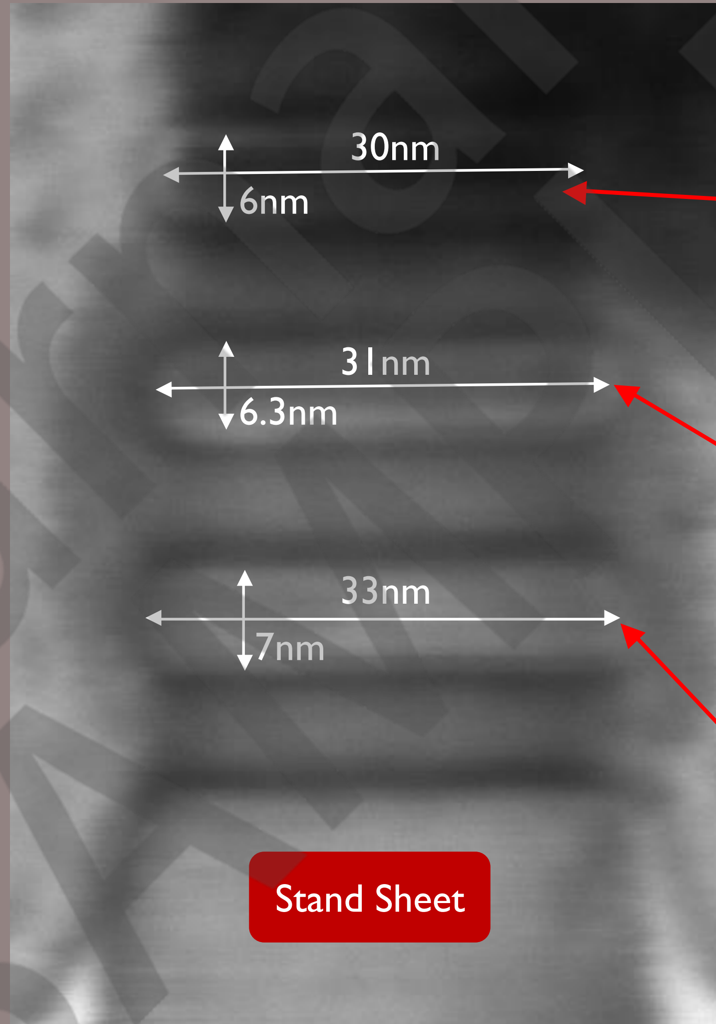


0421-1 Y Cross 1-006

Processor analyze-Sheet Cross-Stand Sheet



0421-1 Y Cross 1-016



Nanosheet #1

Stand sheet Thickness : 30nm
Wide : 6nm
Aspect Ratio : 5:1

Nanosheet #2

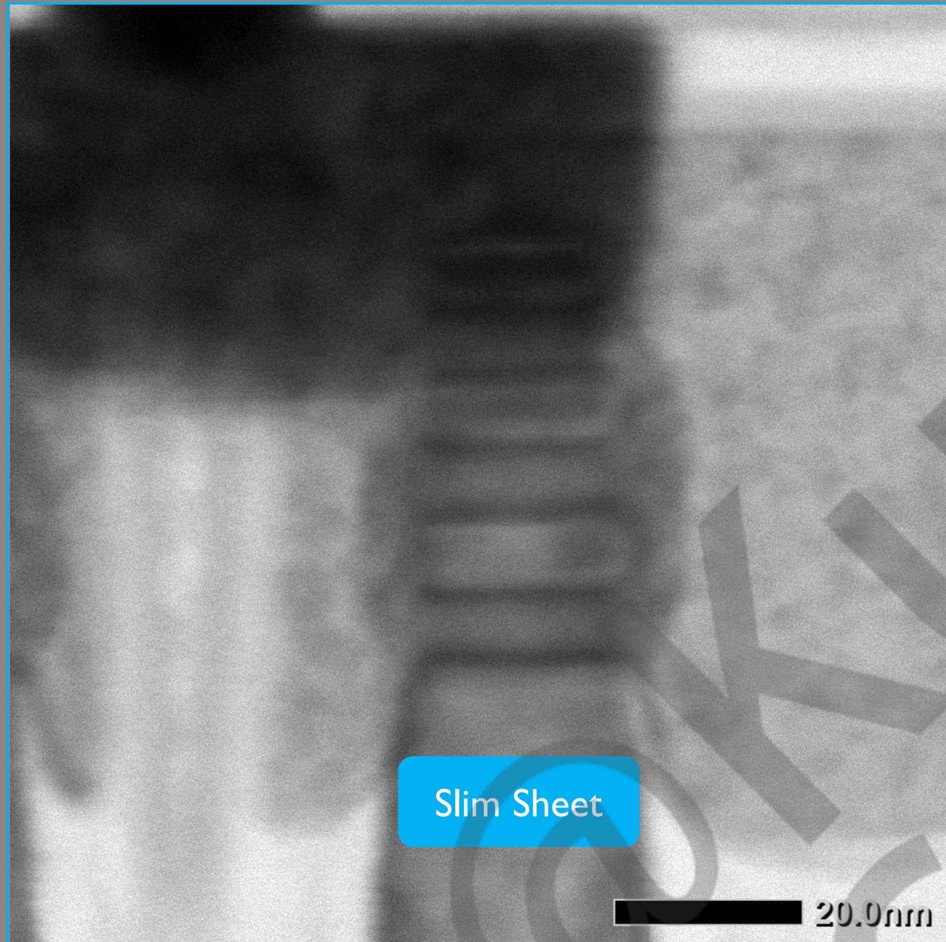
Stand sheet Thickness : 31nm
Wide : 6.3nm
Aspect Ratio : 4.92:1

Nanosheet #3

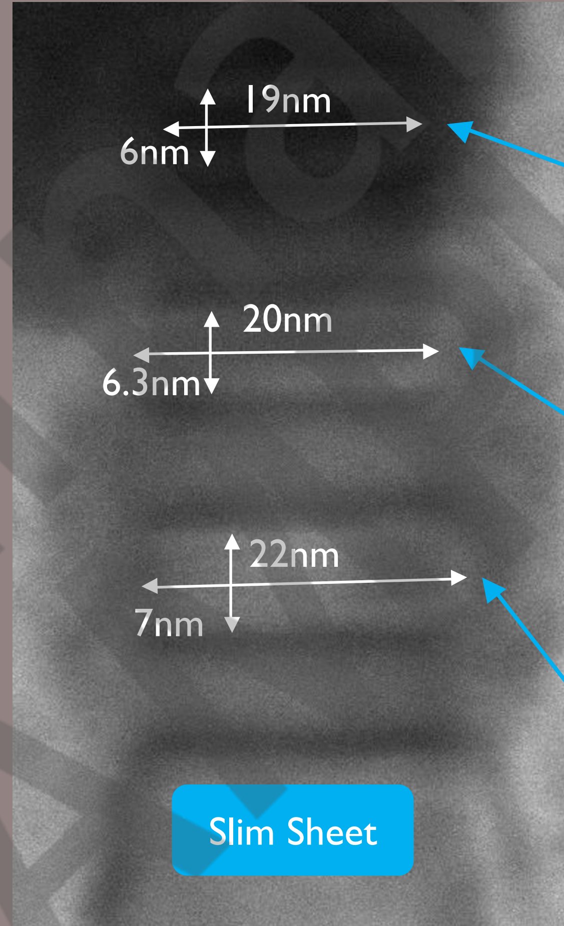
Stand sheet Thickness : 33nm
Wide : 7nm
Aspect Ratio : 4.71:1

Stand Sheet Thickness 30-33nm
Avg 31.3nm

Processor analyze-Sheet Cross-Slim Sheet



0421-1 Y Cross 1-017



Nanosheet #1

Slim sheet Thickness : 19nm
Wide : 6nm
Aspect Ratio : 3.16:1

Nanosheet #2

Slim sheet Thickness : 20nm
Wide : 6.3nm
Aspect Ratio : 3.17:1

Nanosheet #3

Slim sheet Thickness : 22nm
Wide : 7nm
Aspect Ratio : 3.14:1

Slim Sheet Thickness 19-22nm
Avg 20.3nm

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Processor analyze-Sheet Cross

Stand sheet Thickness: 30nm
Wide: 7nm
Aspect Ratio: 5:1

Std #1

Stand sheet Thickness: 31nm
Wide: 7nm
Aspect Ratio: 4.92:1

Std #2

Stand sheet Thickness: 33nm
Wide: 7nm
Aspect Ratio: 4.71:1

Std #3

Stand Sheet

Slim Sheet

50.0nm

Slim #1

Slim sheet Thickness: 19nm
Wide: 6nm
Aspect Ratio: 3.16:1

Slim #2

Slim sheet Thickness: 20nm
Wide: 6.3nm
Aspect Ratio: 3.17:1

Slim #3

Slim sheet Thickness: 22nm
Wide: 7nm
Aspect Ratio: 3.14:1

Stand Sheet Thickness 30-33nm

Avg 31.3nm

Slim Sheet Thickness 19-22nm

Avg 20.3nm

Stand vs Slim Thickness = 3:2

Slim sheet achieves a 35% reduction in thickness,with a 3:2 Ratio over Std Sheet

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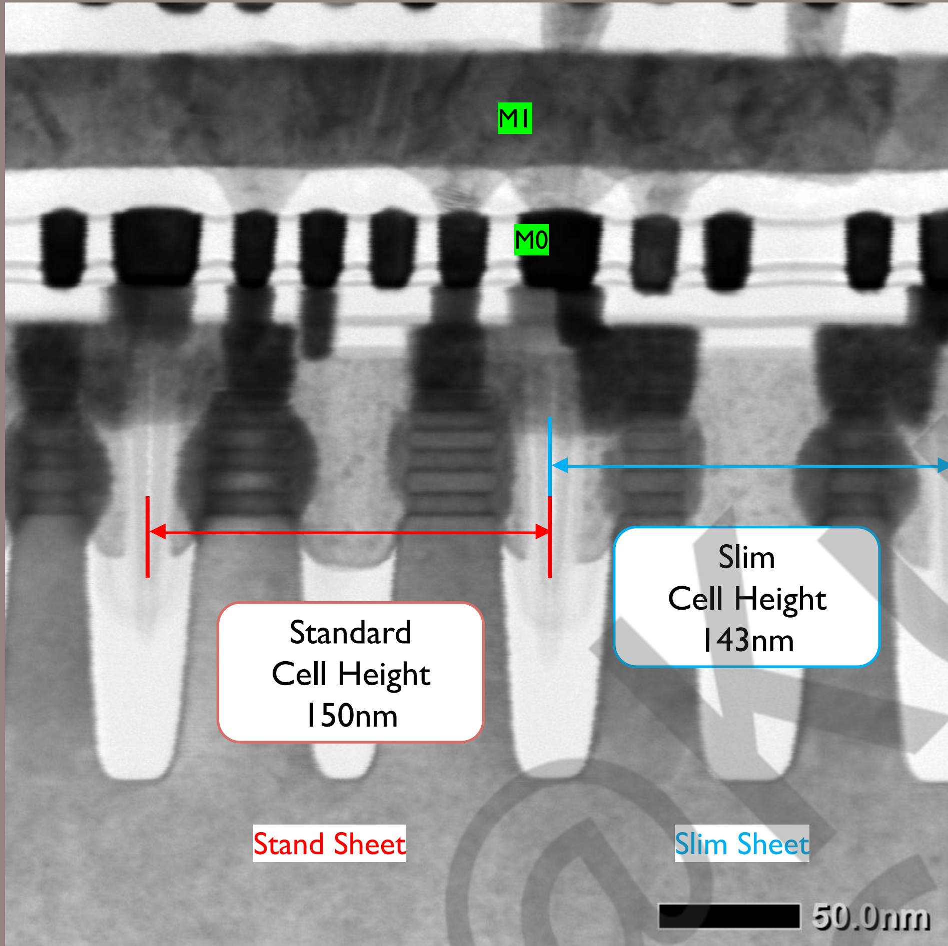
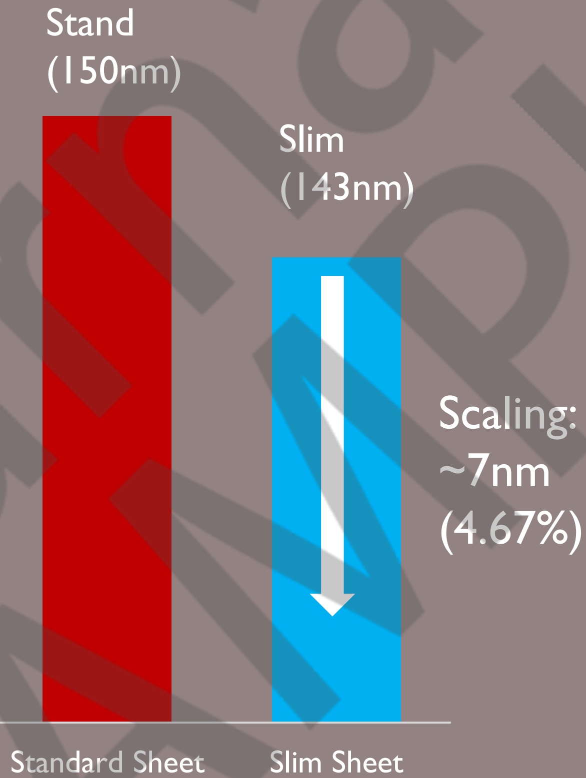
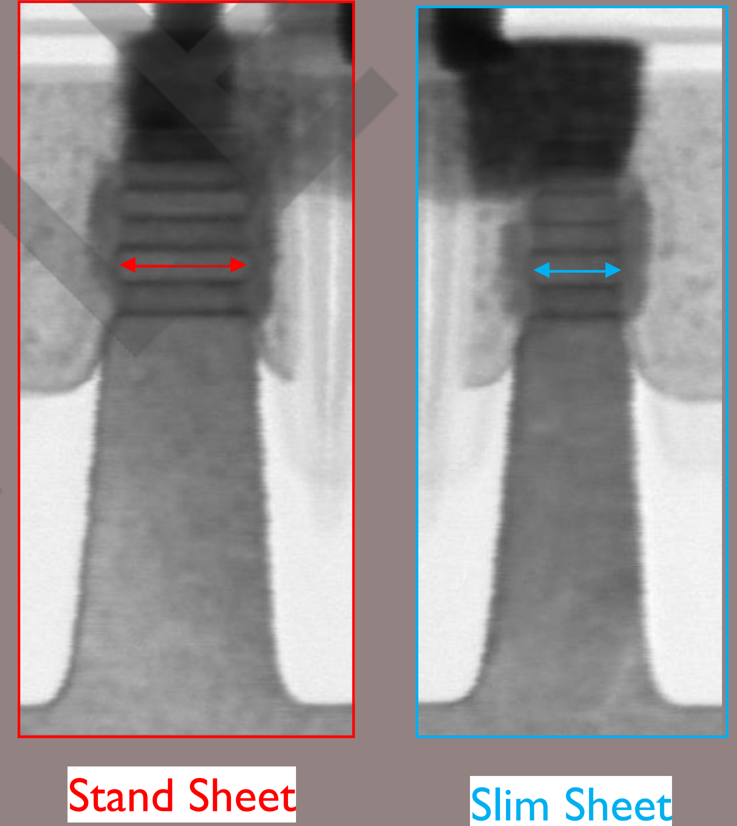
Processor analyze-Sheet Cross



0421-1 Y Cross 1-006



Std vs slim Height
Ratio= 150 : 143
(~1.05:1)



Cell Height 150nm Cell Height 143nm

Δ = -7nm (-4.6%)

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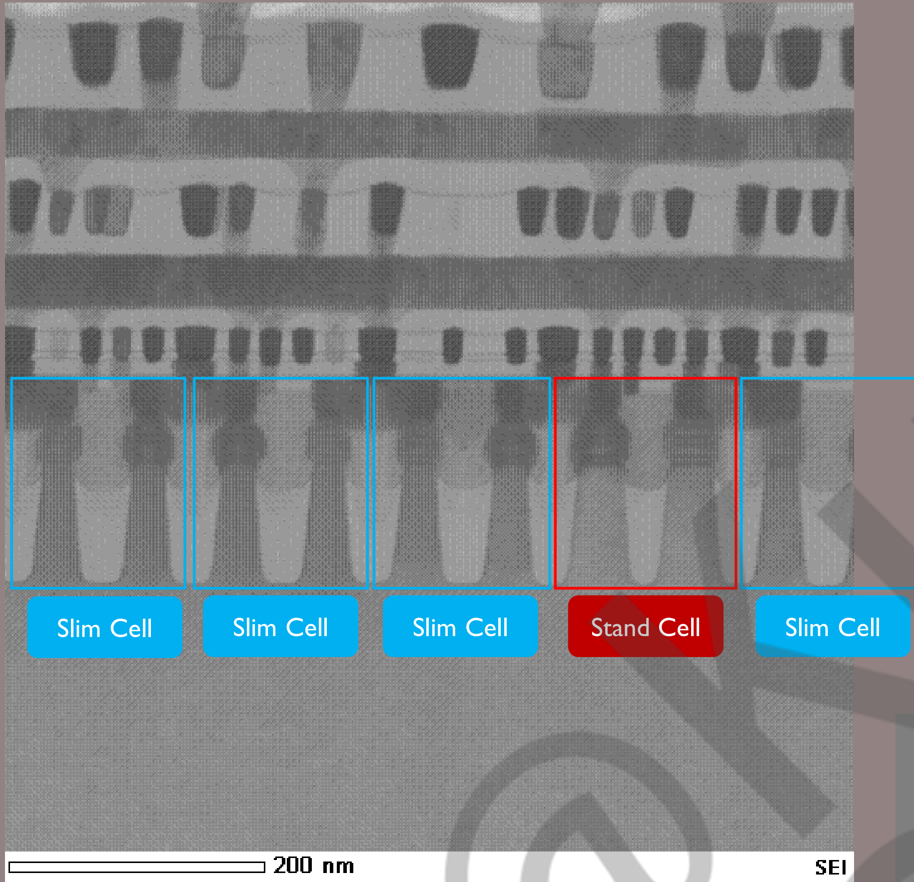
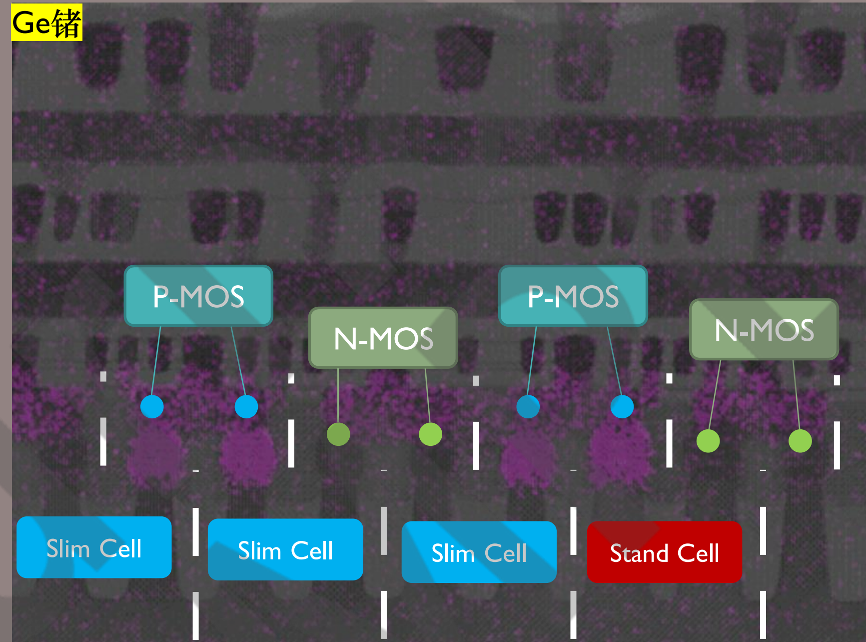
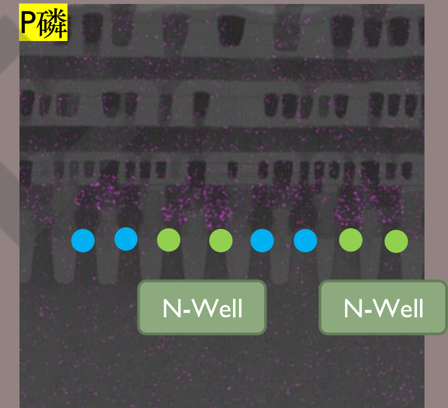
Processor analyze-Sheet Cross-EDS



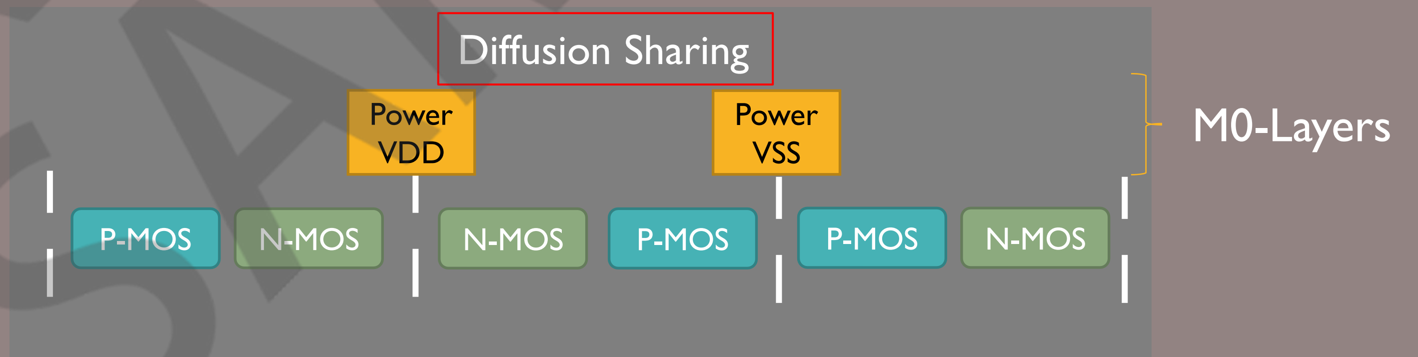
0421-1 Y Cross EDS-4



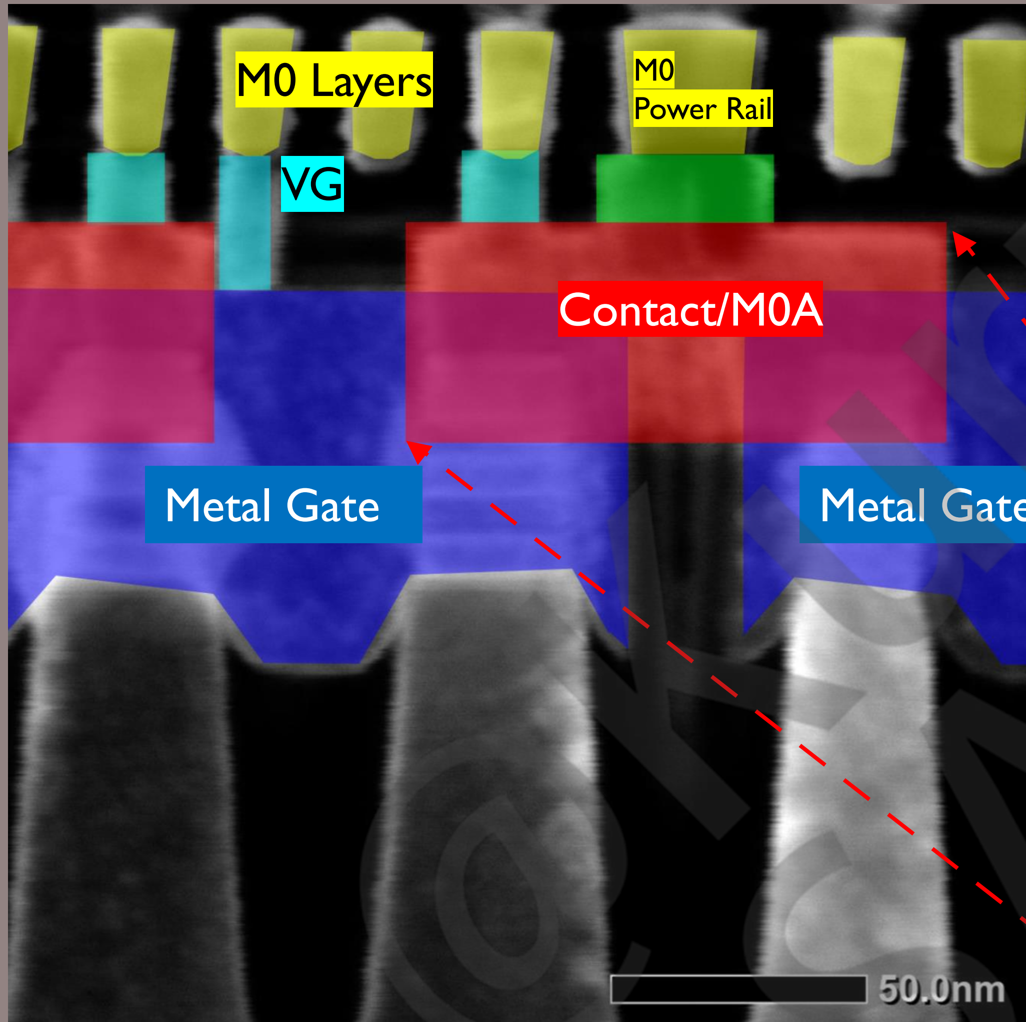


P-MOS — Ge (Germanium) in PMOS Channels

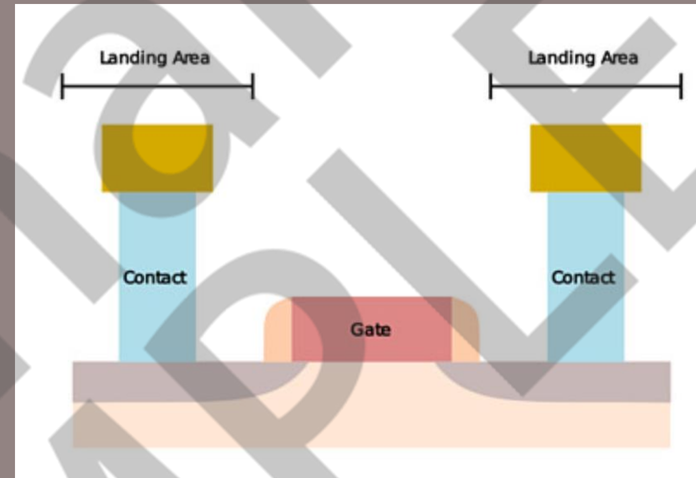
N-MOS — Phosphorus (P) Doping for NMOS Source/Drain



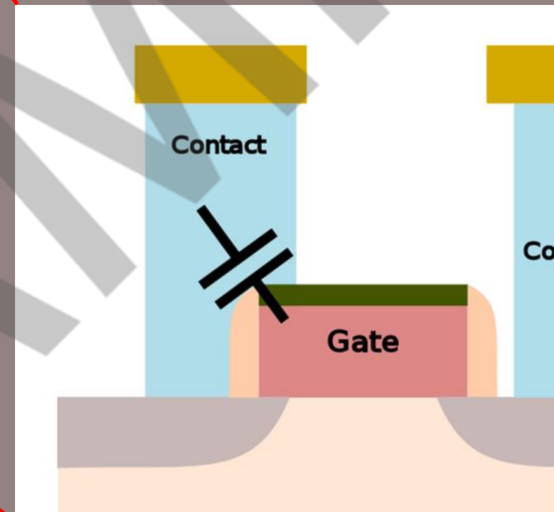
M0-Layers



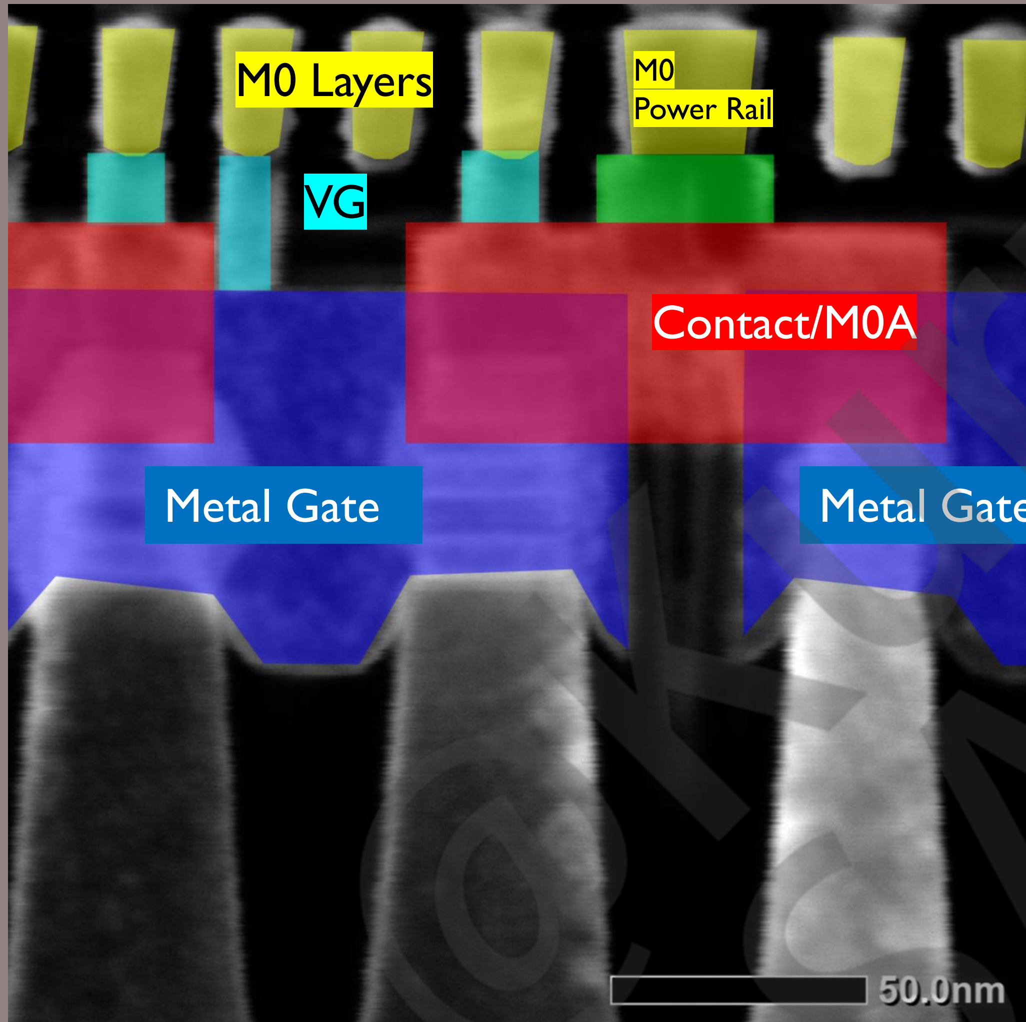
0421-1 Y Cross 1-011



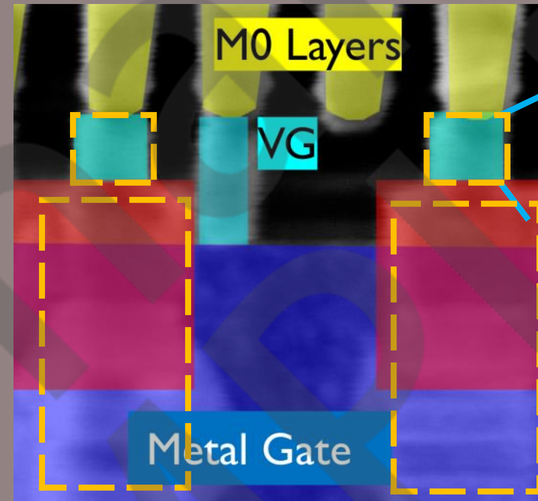
non
Self-Aligned Contact

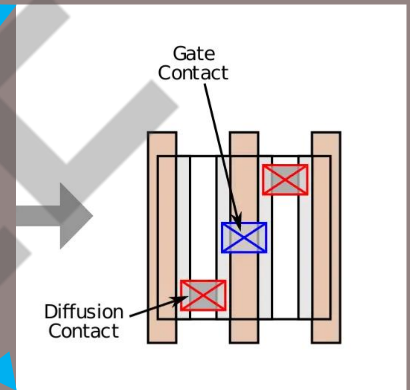


Self-Aligned Contact



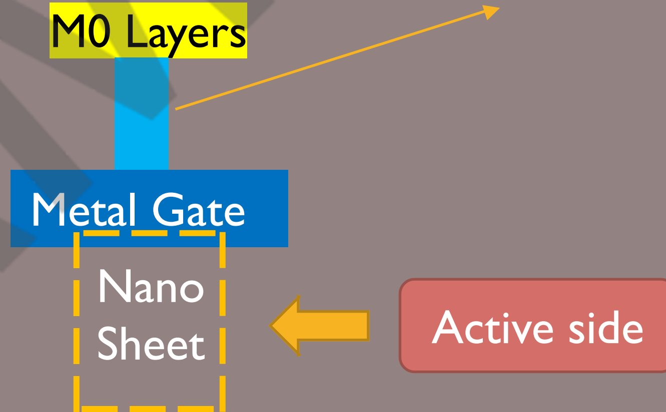
0421-1 Y Cross 1-011





Use COAG

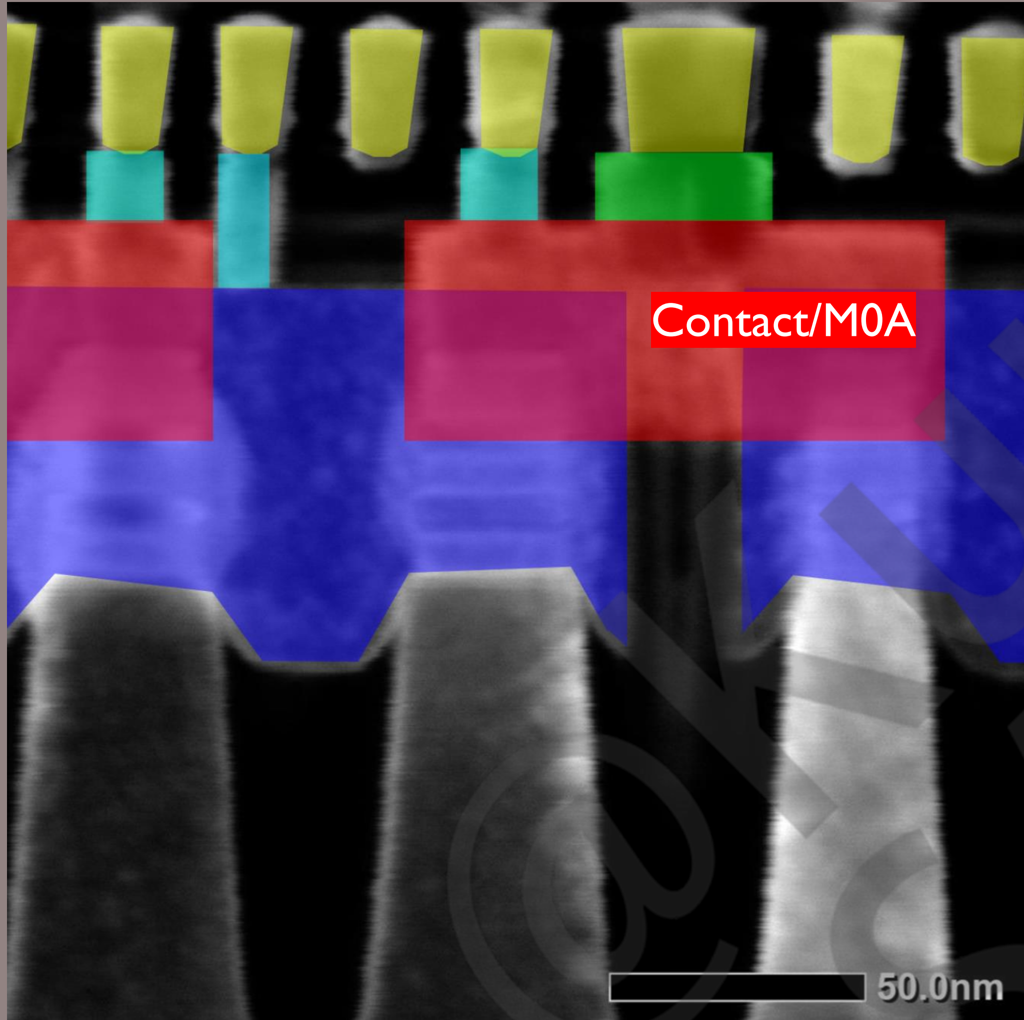
Contact Over Active Gate



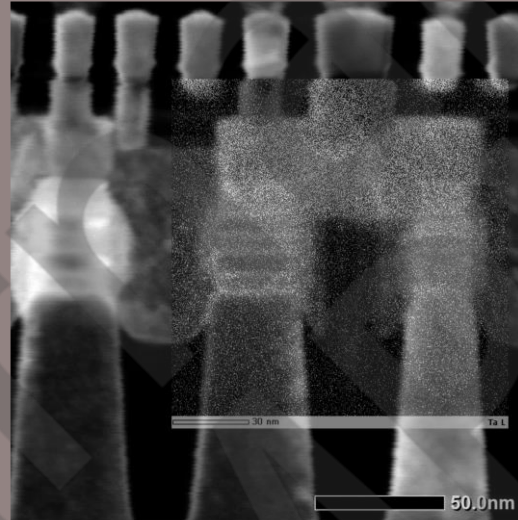
Active side

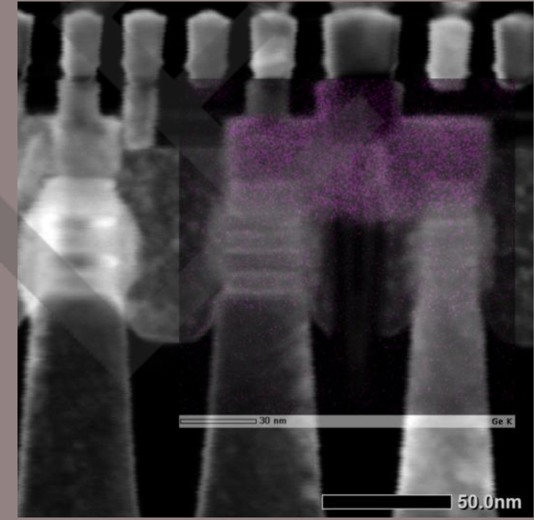
SAMPLE

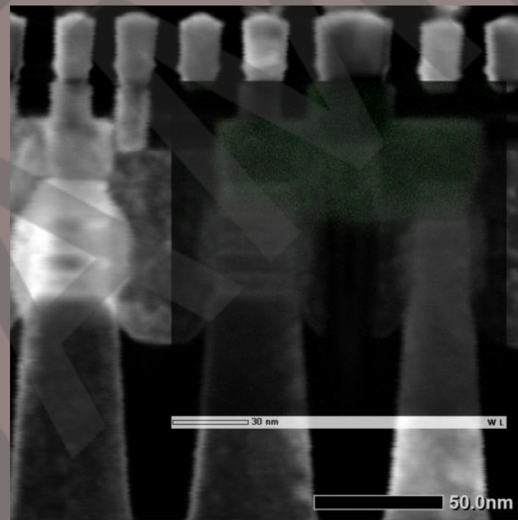
Processor analyze-Sheet Cross-EDS-Contact/M0A



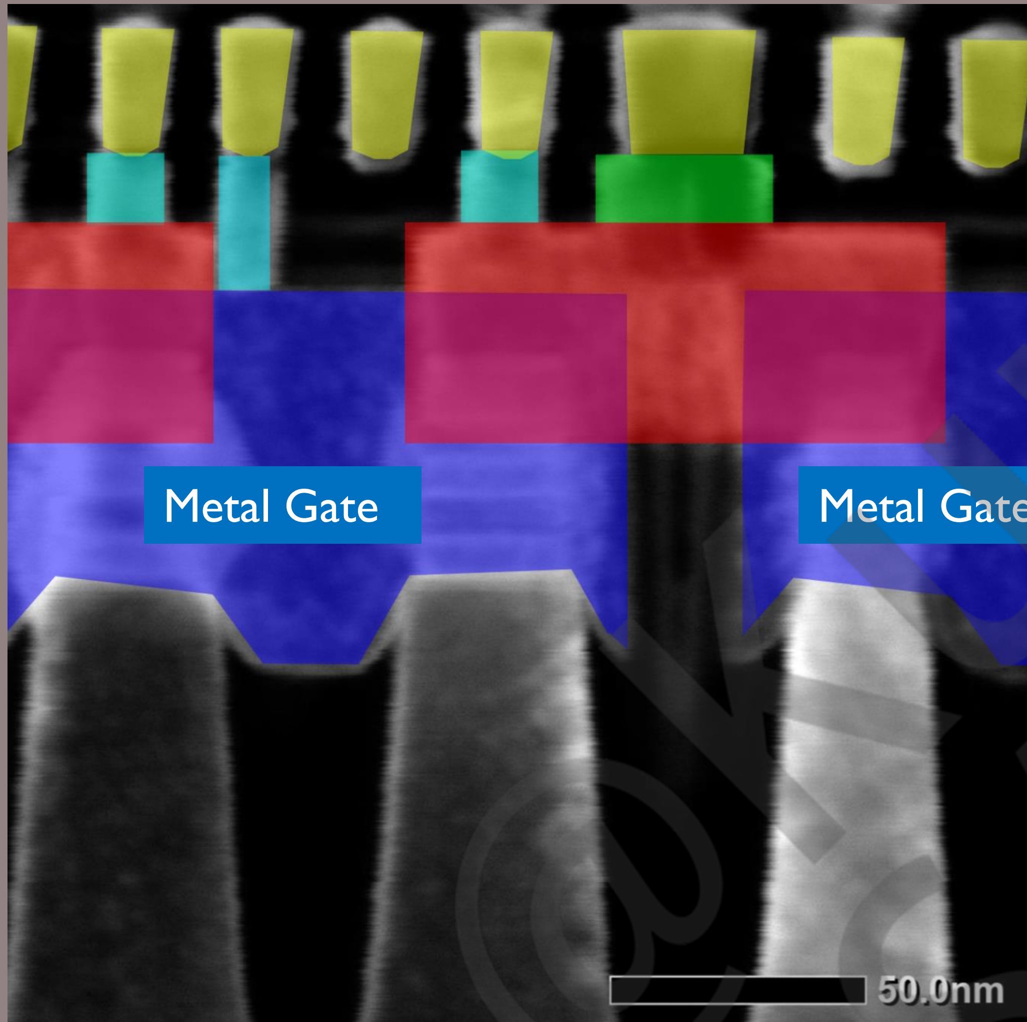
0421-1 Y Cross 1-011



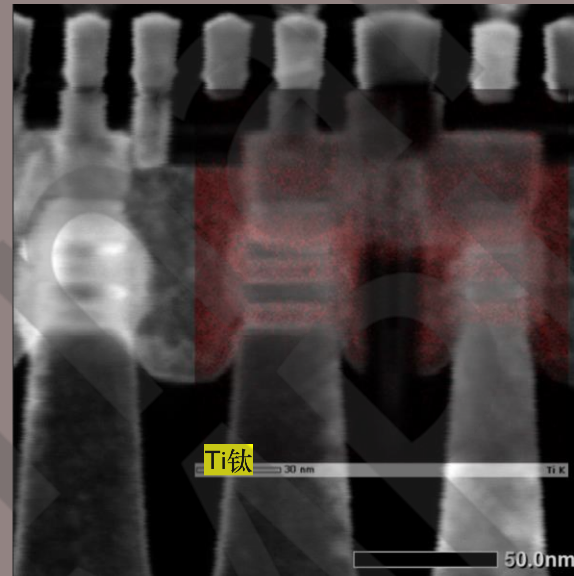


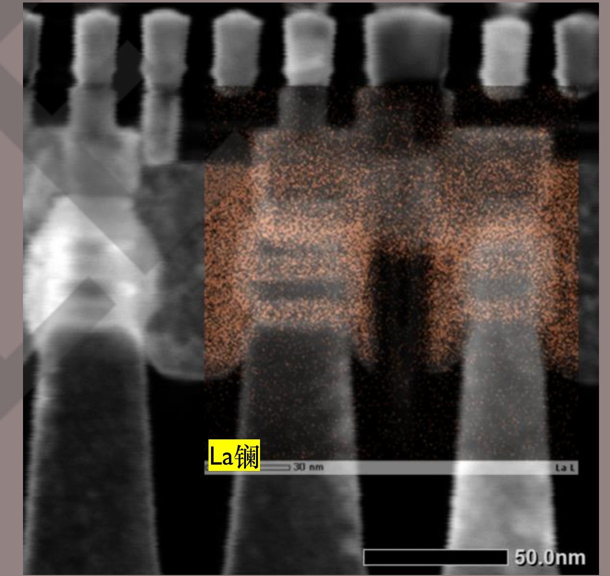


Contact/M0A
•Materials : W (Tungsten) + Ta (Tantalum)
•Observation: Traces of Ge (Germanium) detected,likely due to deposition failure or unintended precursor residuals.



0421-1 Y Cross 1-011





HKMG Implementation:Ti and La

Ti (Titanium):

•Acts as the **primary structural layer** for the Metal Gate.

•Serves as the **conductive fill material** to ensure low resistivity and robust gate metallization.

La (Lanthanum):

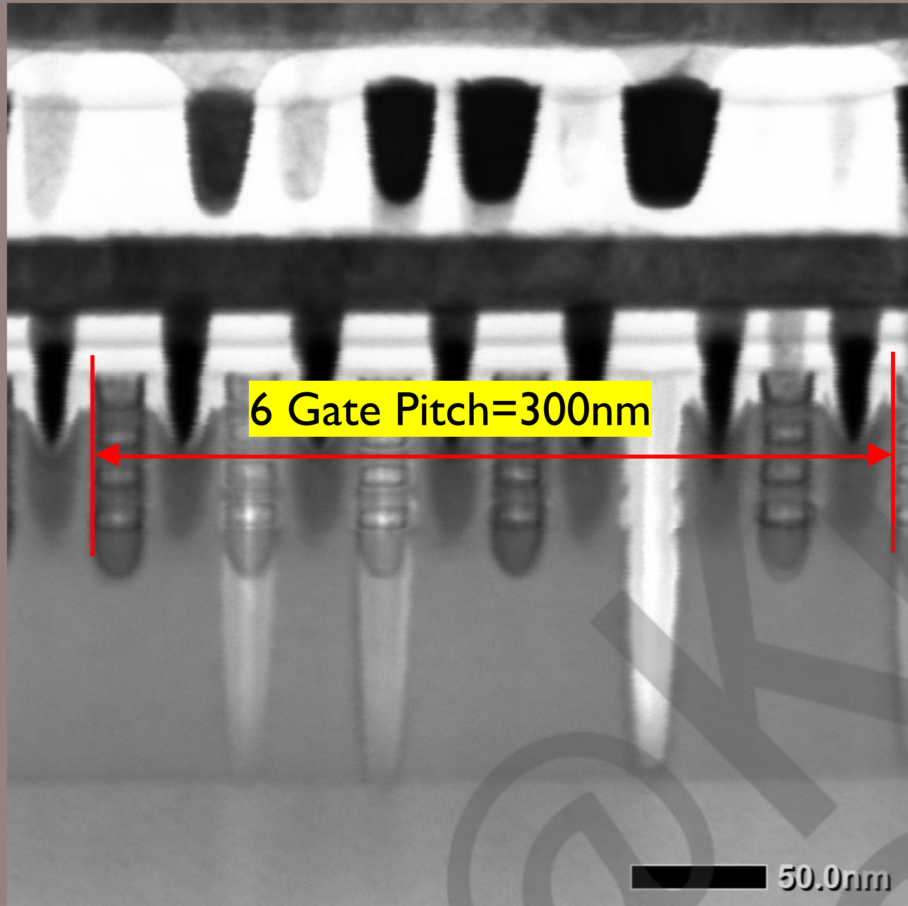
•Acts as a **Work Function Tuning** element,.

•Forms a **Dipole Layer** at the HighK interface to effectively lower the threshold voltage Vth

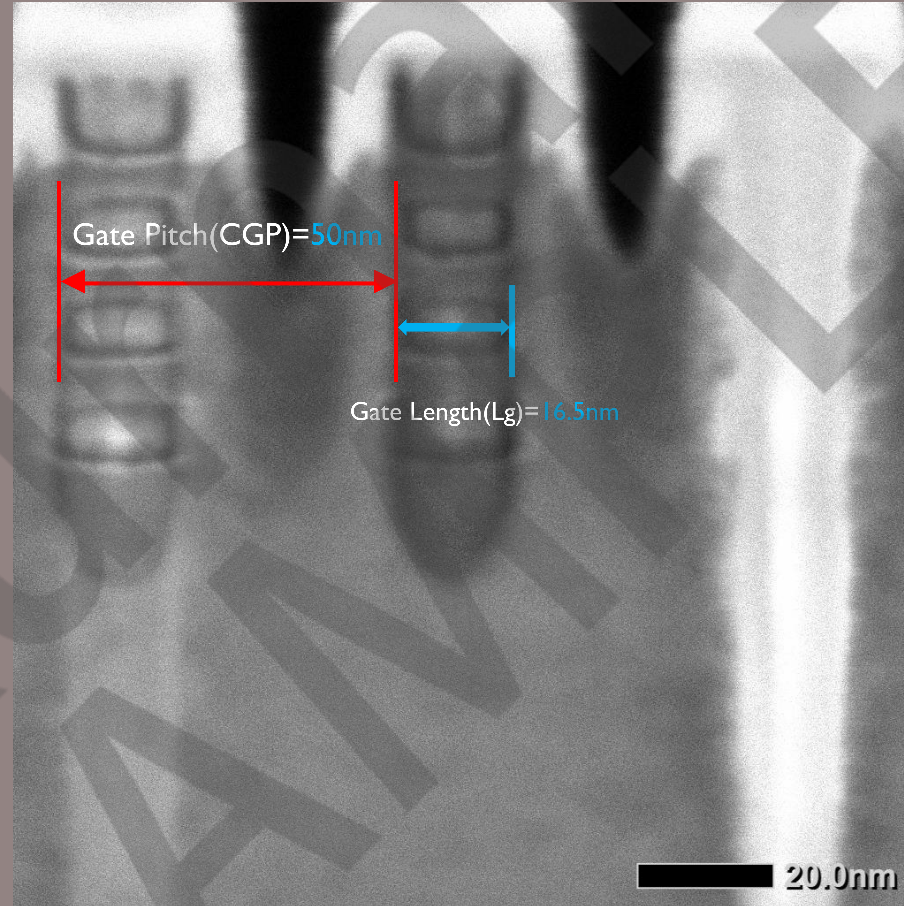
Transistor Analyze

Samsung SF2-Gate Cross

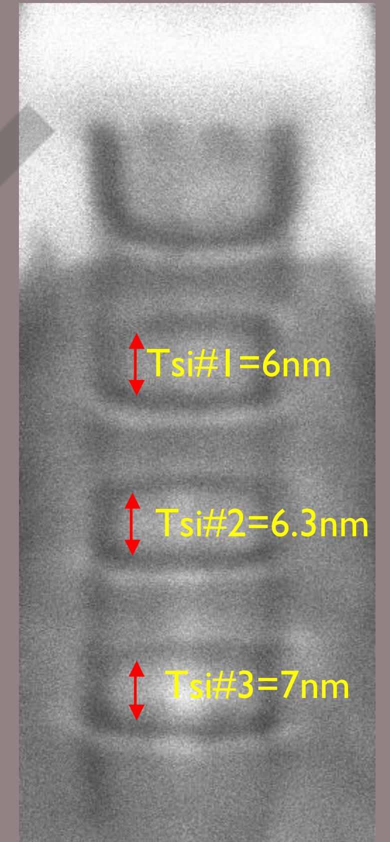
@Kurnal SAMPLE



0421-1 X Cross 2-002



0421-1 X Cross 2-003



Gate Pitch=50nm

Gate Length=16.5nm

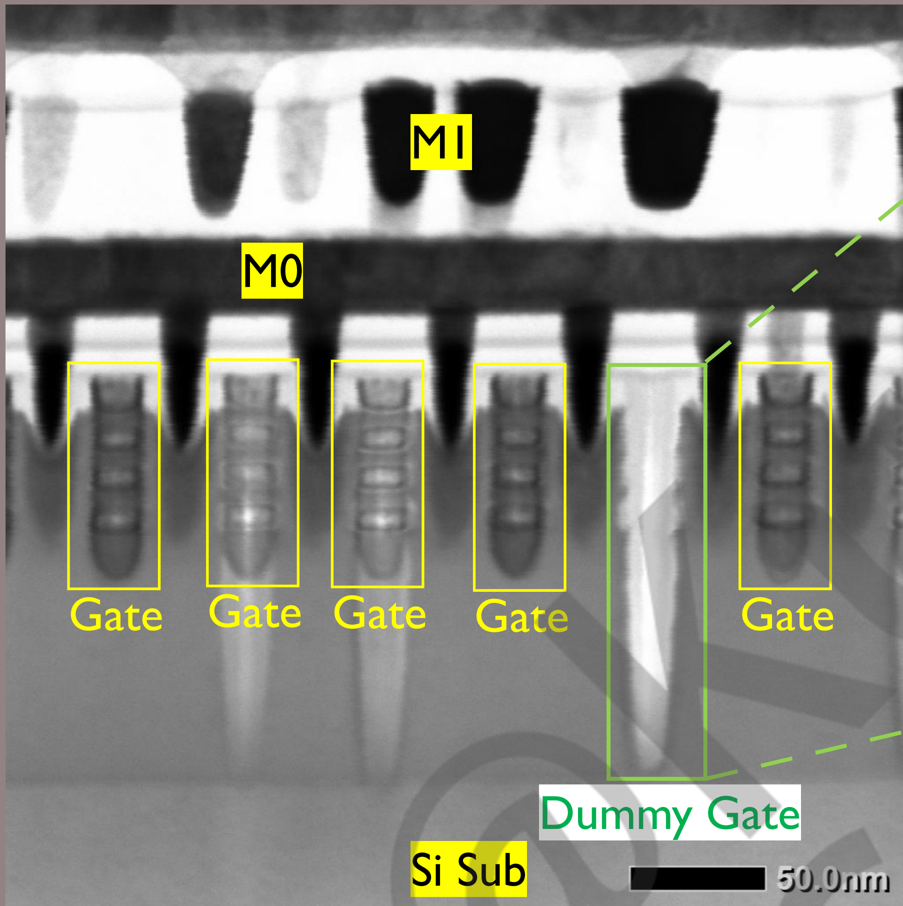
Tsi#1=6nm

Tsi#2=6.3nm

Tsi#3=7nm

@Kurnal SAMPLE

Processor analyze-Gate Cross-Diffusion Break



0421-1 X Cross 2-002

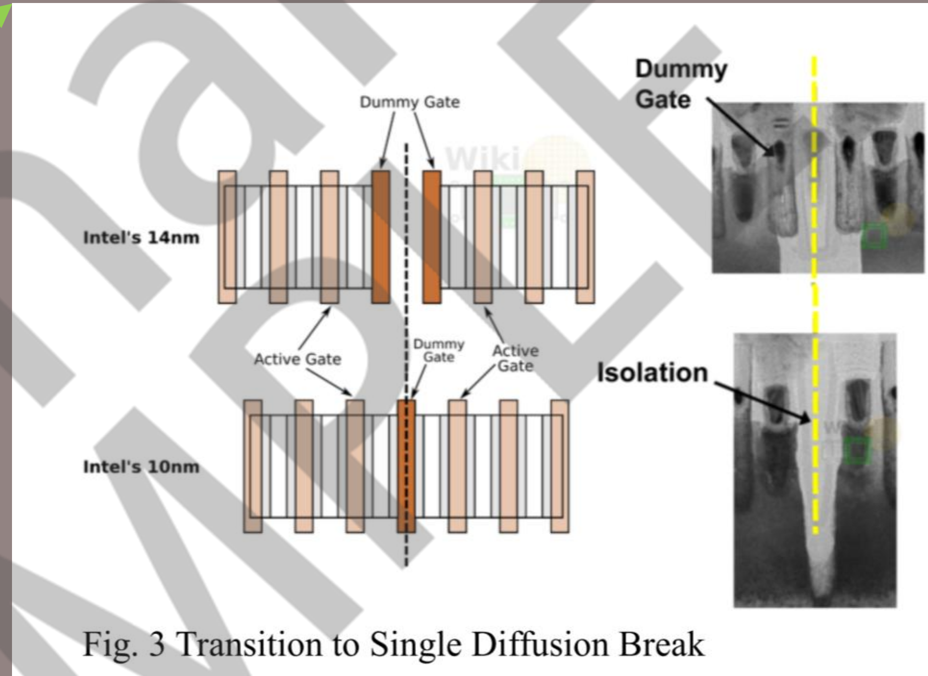
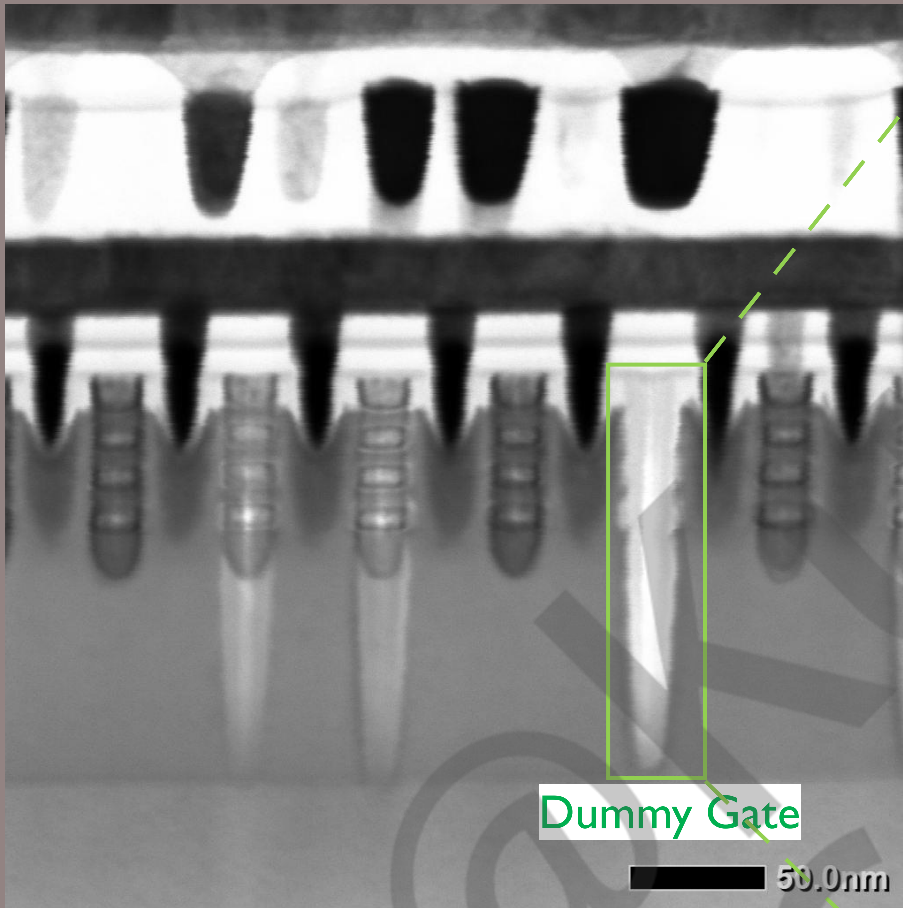


Fig. 3 Transition to Single Diffusion Break

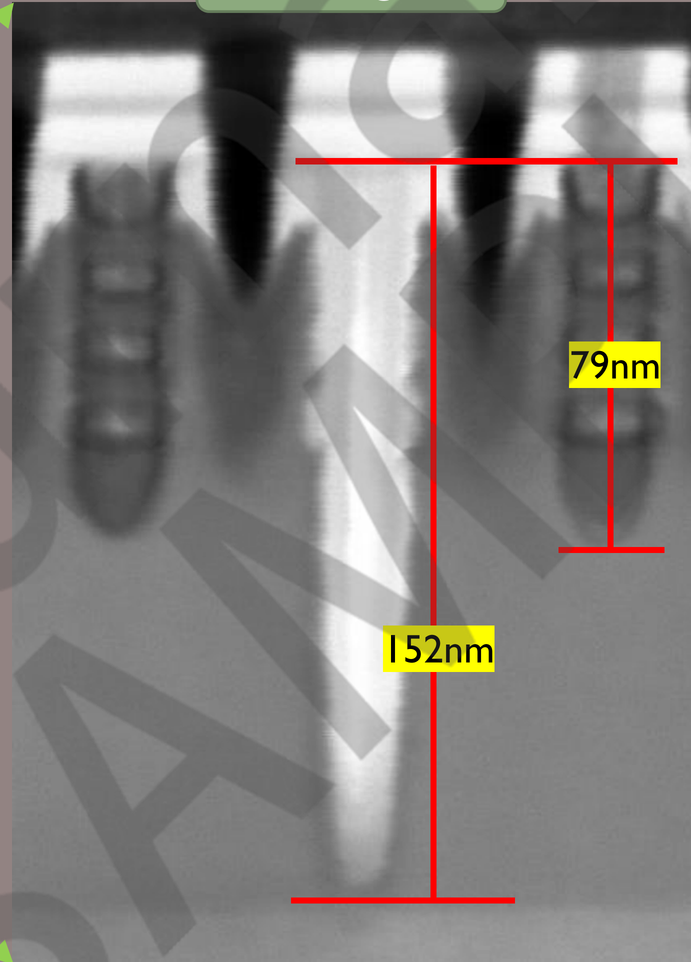
Use Single Diffusion Break in SF2

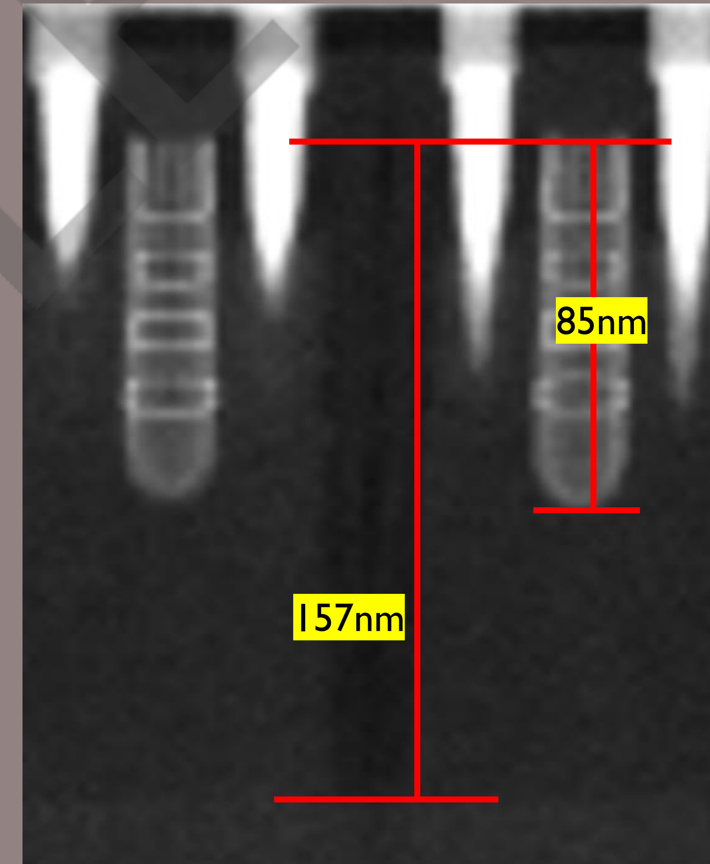
©Kurnal SAMPLE

Processor analyze-Gate Cross-Dummy Gate

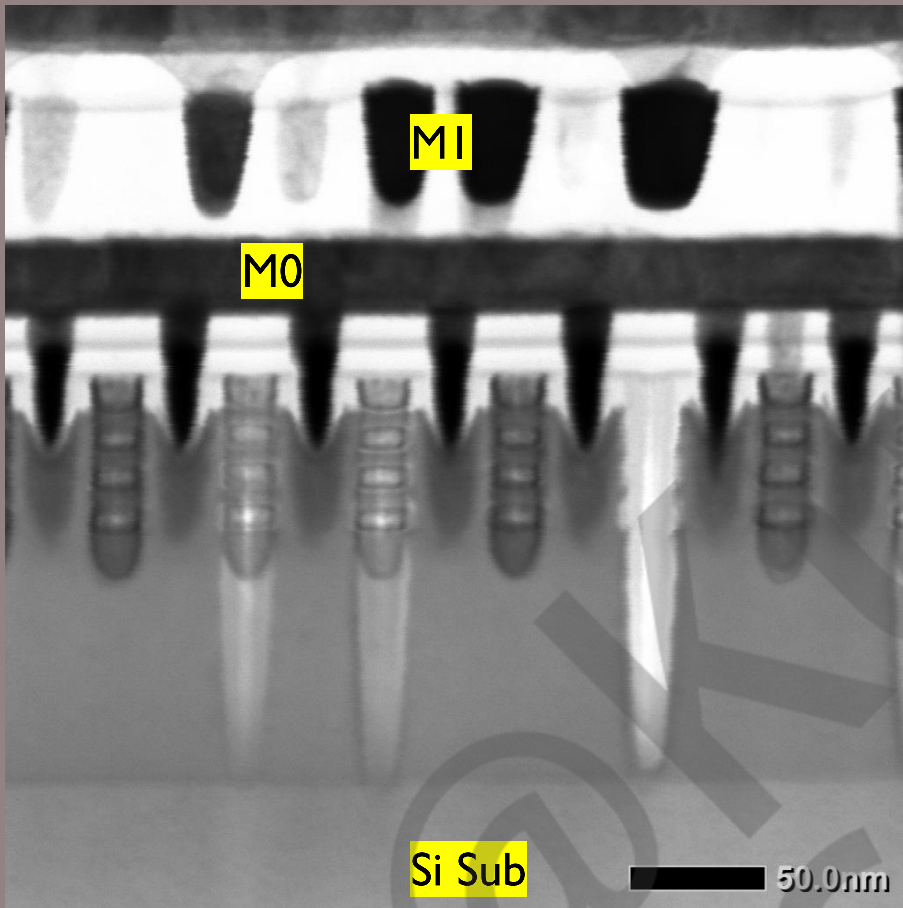


0421-1 X Cross 2-002

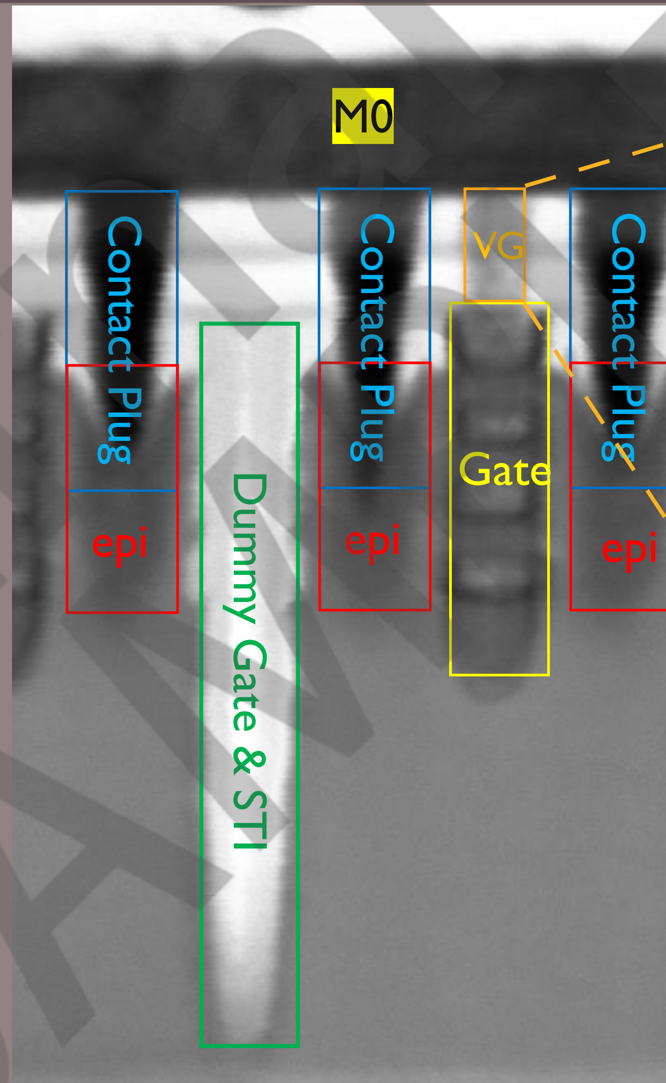




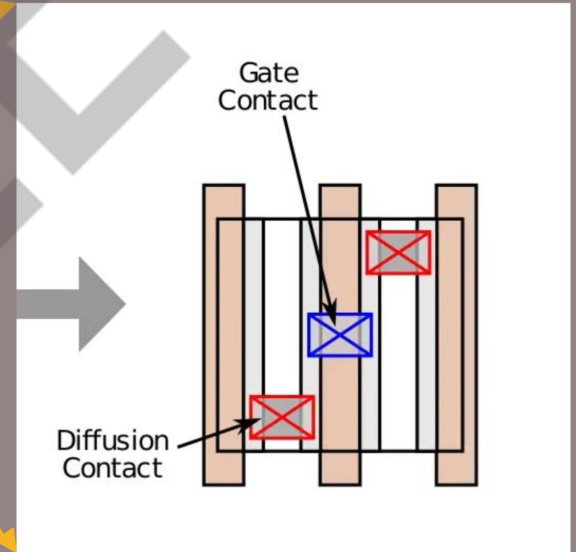
©Kurnal SAMPLE



0421-1 X Cross 2-002



Use COAG



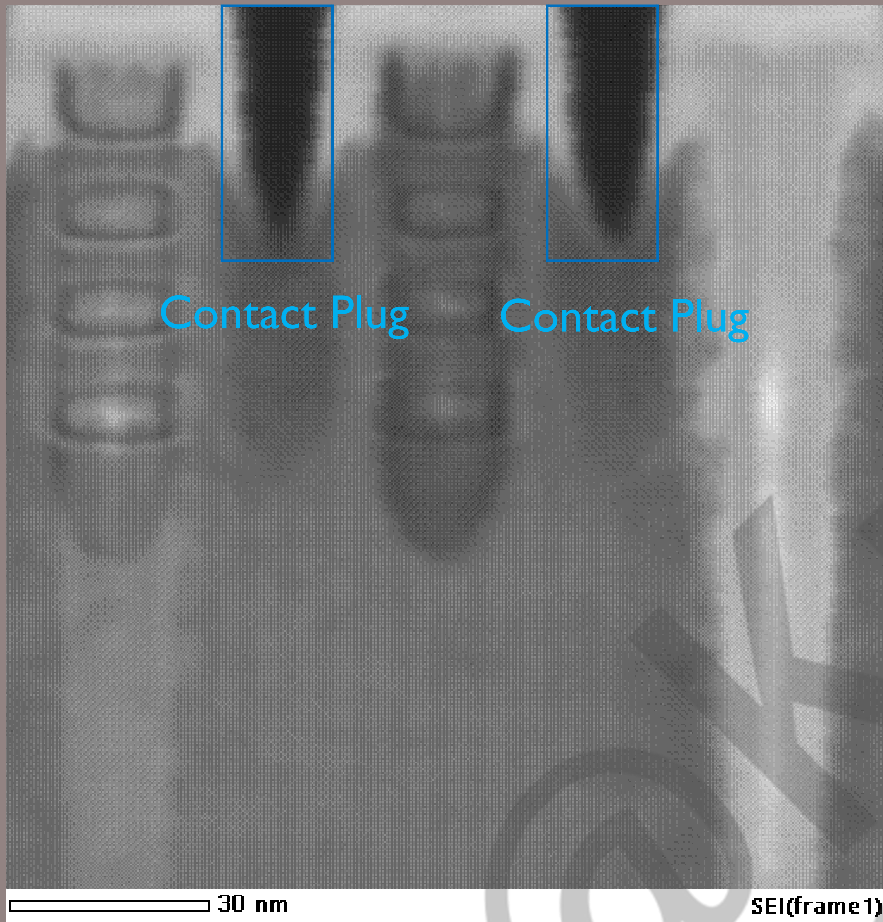
Yellow Box (Gate): Identifies the **3-stack nanosheet** GAAFET gate stack.

Epitaxial S/D: Crystalline structure with potential strain-inducing material alloys

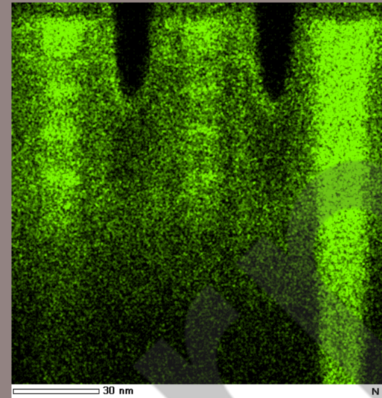
Blue Box (Contact): Locates theplug interfacing the epi with upper metal layers.

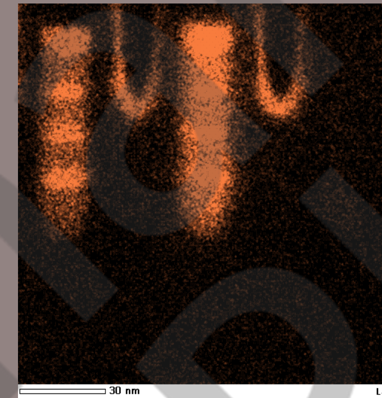
@Kurnal SAMPLE

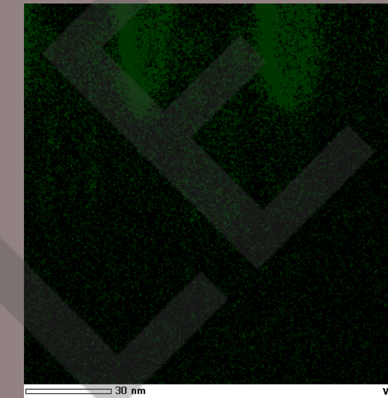
Processor analyze-Gate Cross-Contact Plug

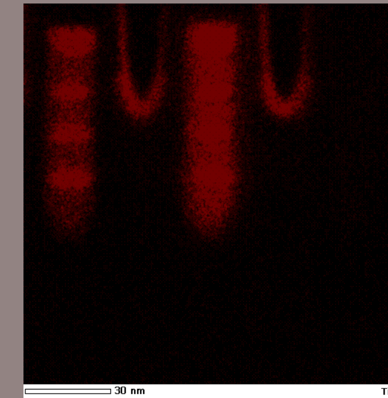


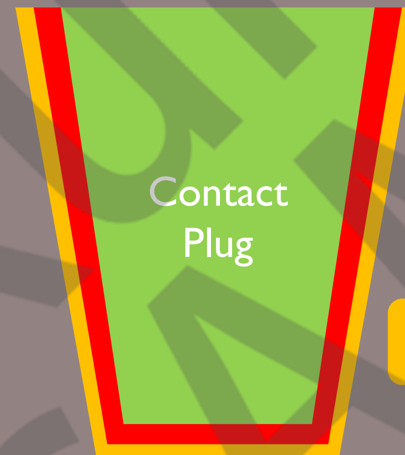
0421-1 X Cross EDS-3











W-Plug

TiN Barrier
Ti Liner

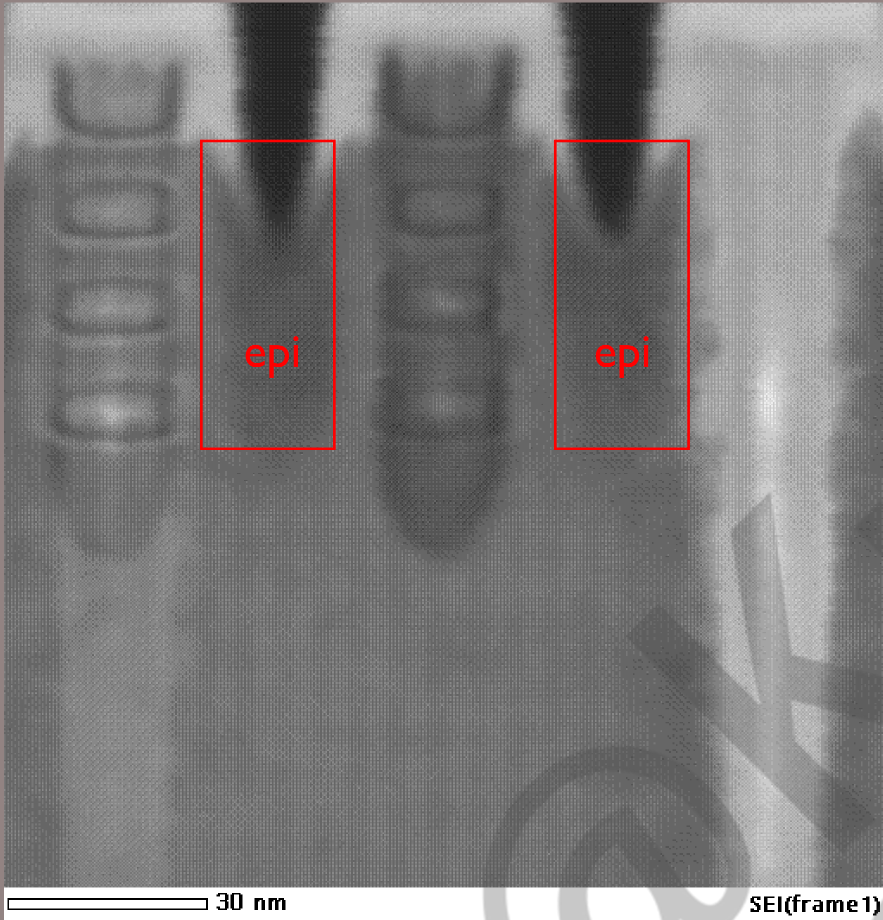
La Dipole

W (Tungsten Core): Fills the contact holes and connects the transistor to the metal layer.

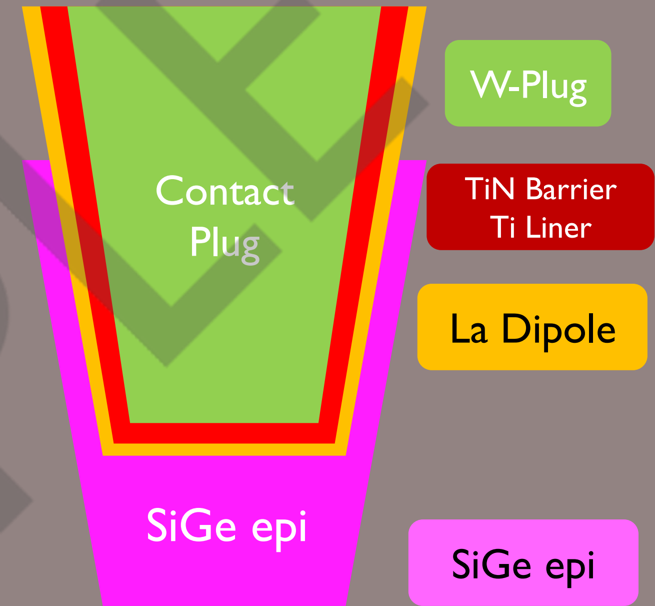
TiN (Barrier Layer): A protective layer that prevents chemical damage to the structure and prevents metal atom leakage.

Ti (Substrate): A gel-like layer that helps the tungsten core adhere and reduces resistance, resulting in better connectivity.

La (Dipole Layer): A special layer used to fine-tune the transistor's switching voltage and improve chip performance.



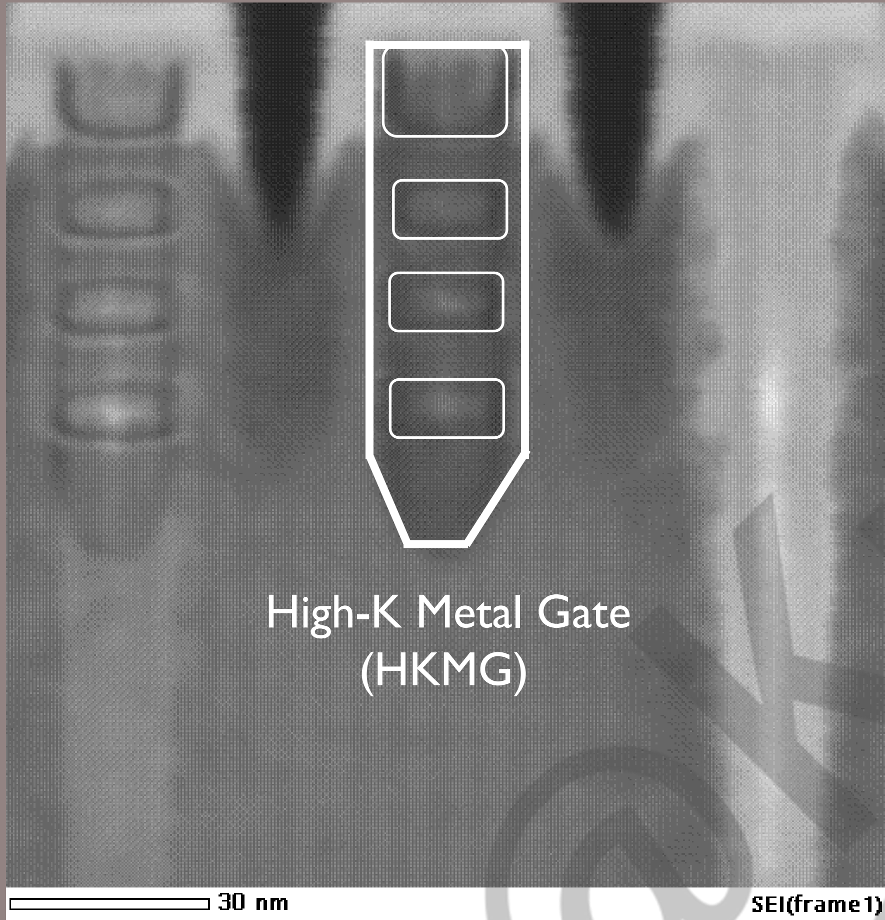
0421-1 X Cross EDS-3



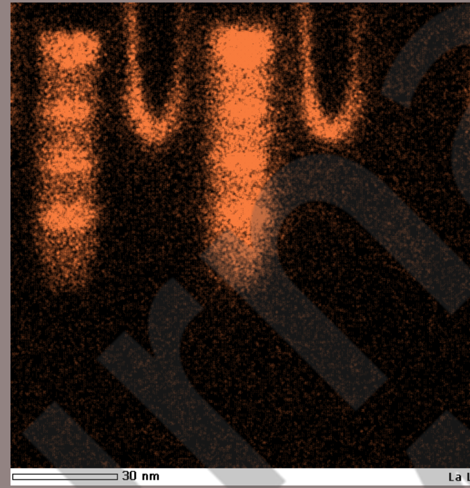
SiGe epi (Epitaxial Layer): A strained crystal layer grown in the source/drain areas to increase hole mobility and significantly enhance pFET speed.

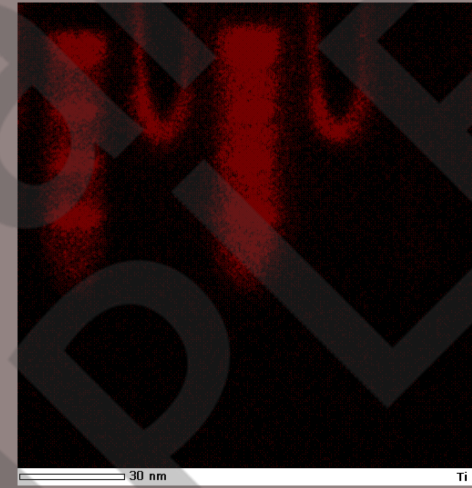
@Kurnal SAMPLE

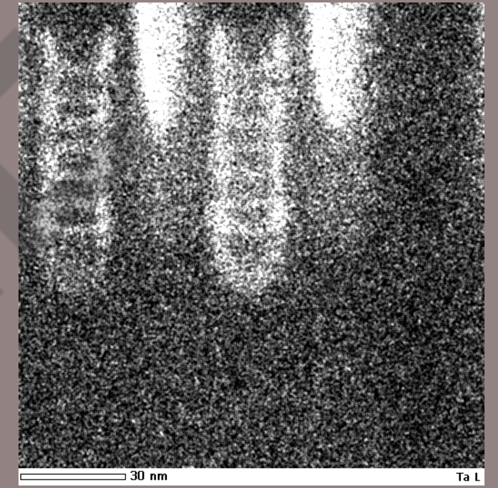
Processor analyze-Gate Cross-Gate

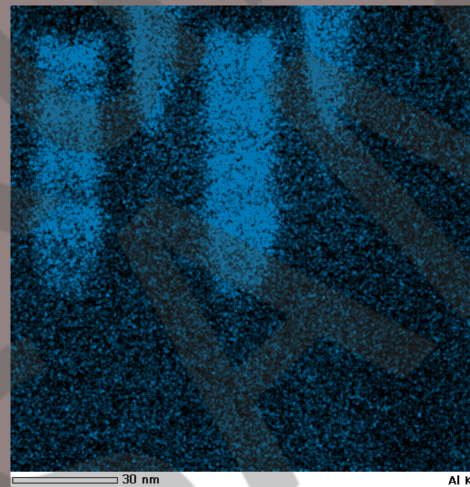


0421-1 X Cross EDS-3







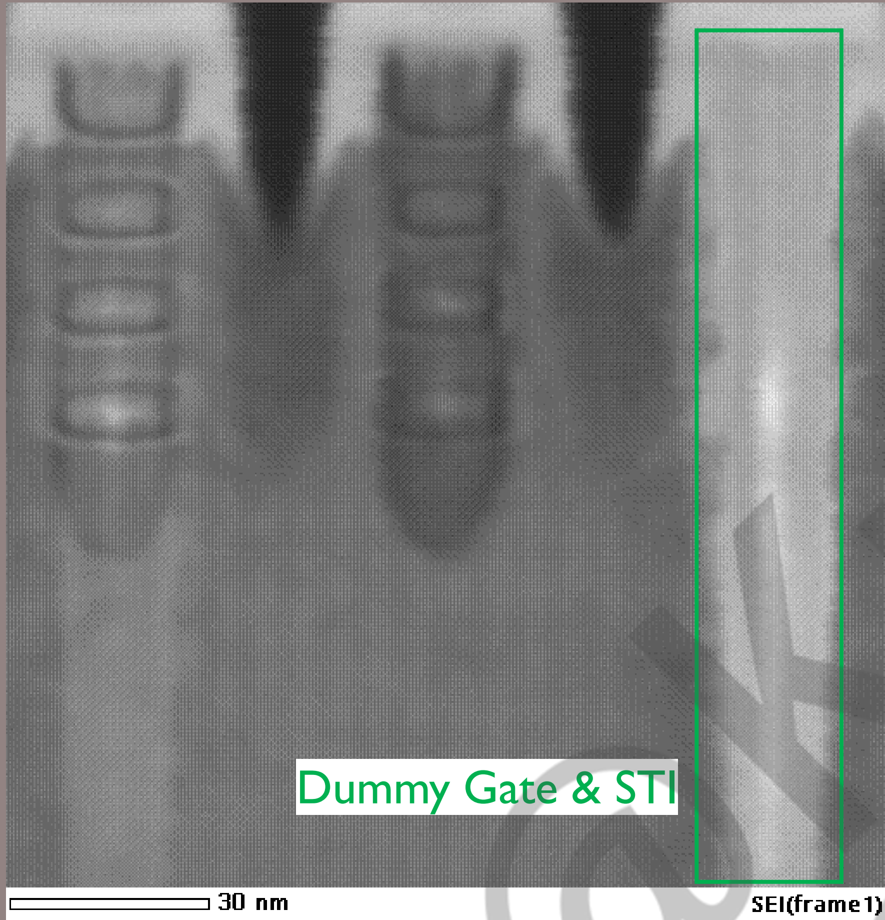


这里写一下建模

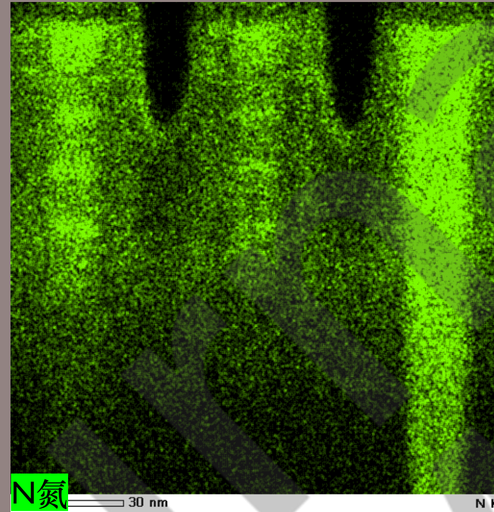
SiO2/HfO2/Al2O3/TiN/TaN/W

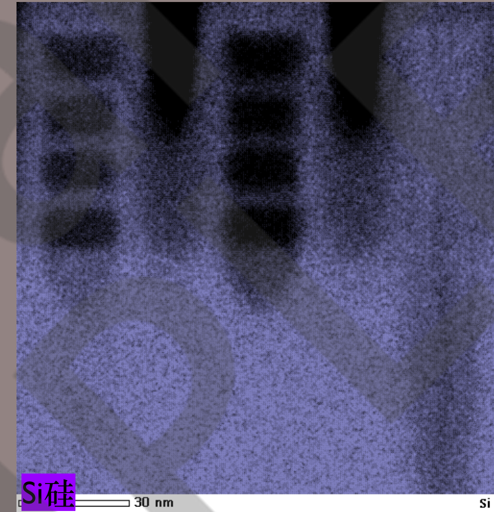
@Kurnal SiPL

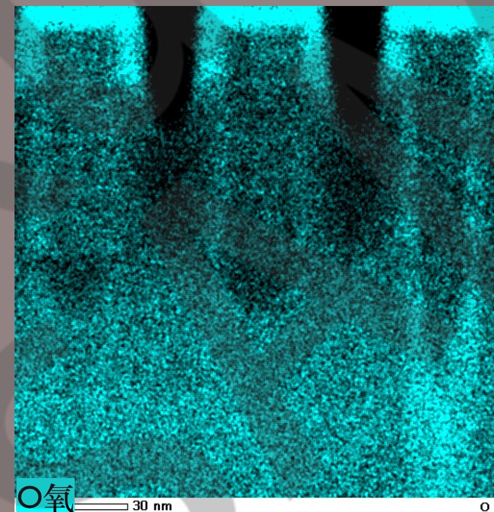
Processor analyze-Gate Cross-Dummy Gate

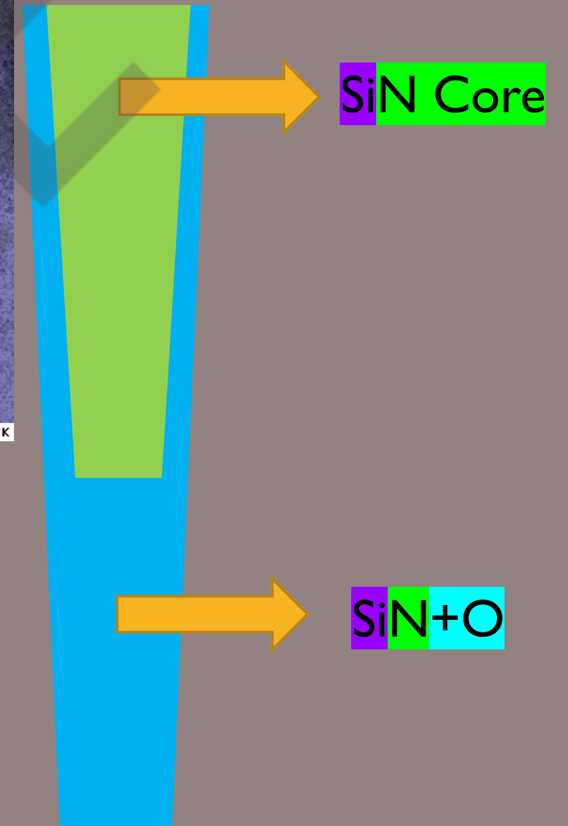


0421-1 X Cross EDS-3







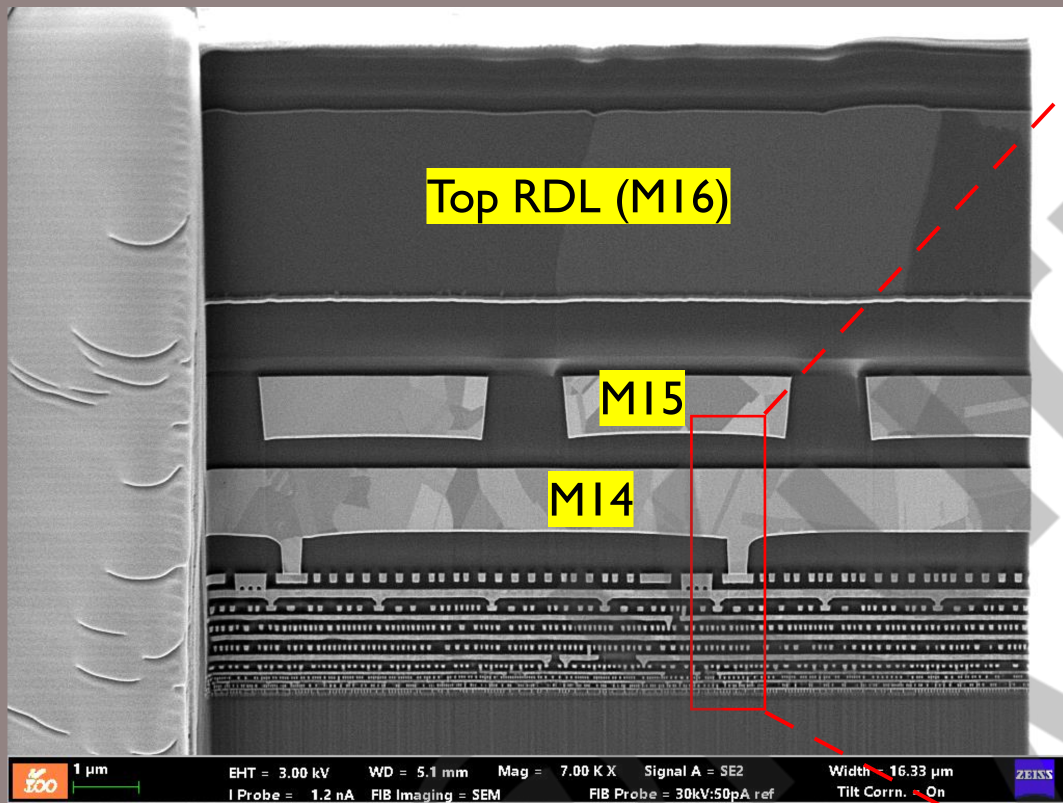


Metal Layers

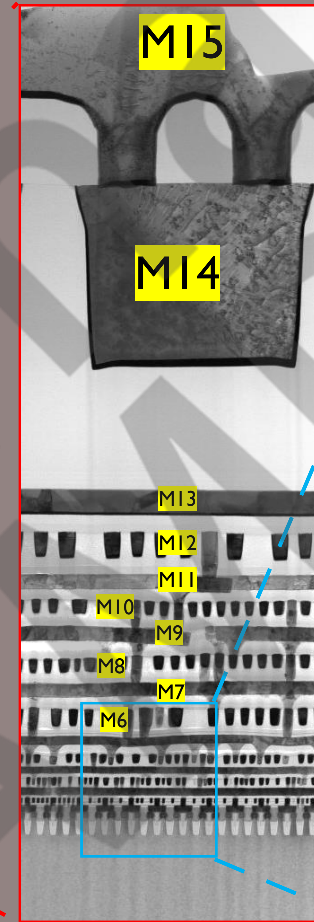
Exynos2600(Samsung 2nm) BEOL

@Kurnal SAMPLE

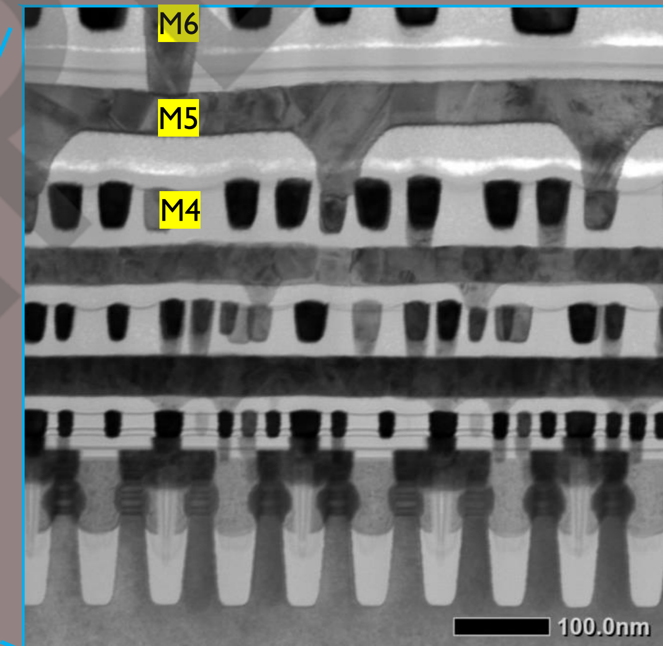
Exynos2600(Samsung 2nm) BEOL



0420-2-02



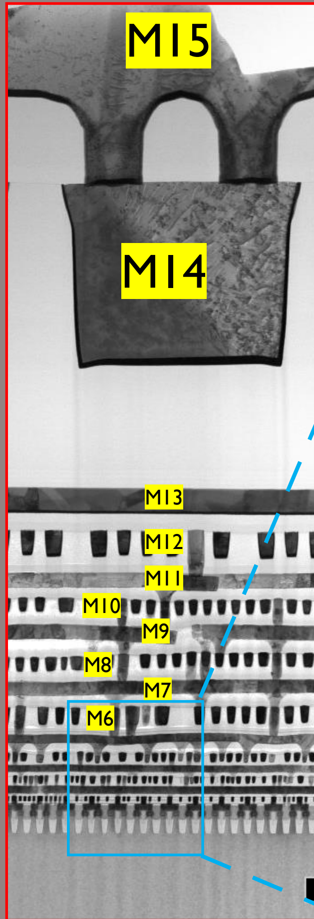
0421-1-Y-Cut-1-002



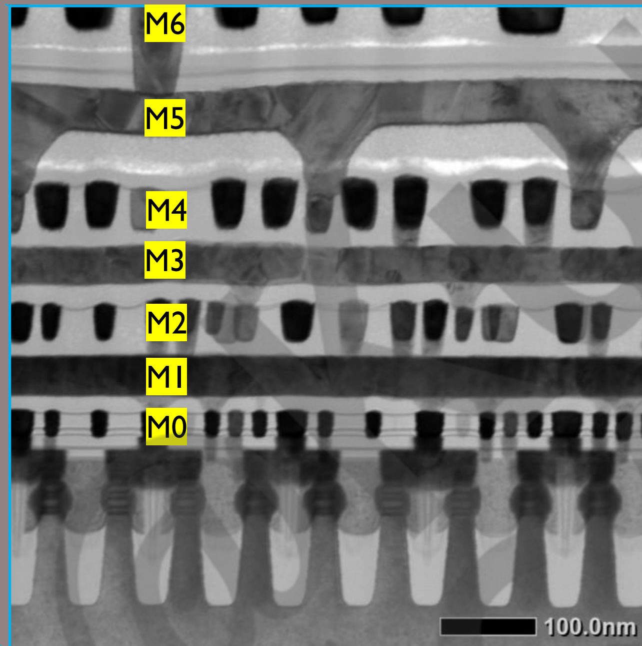
0421-1-Y-Cut-1-006

The die process uses 17 metal layers: 16 Cu + 1 Al

Exynos2600(Samsung 2nm) BEOL



0421-1-Y-Cut-1-002



0421-1-Y-Cut-1-006

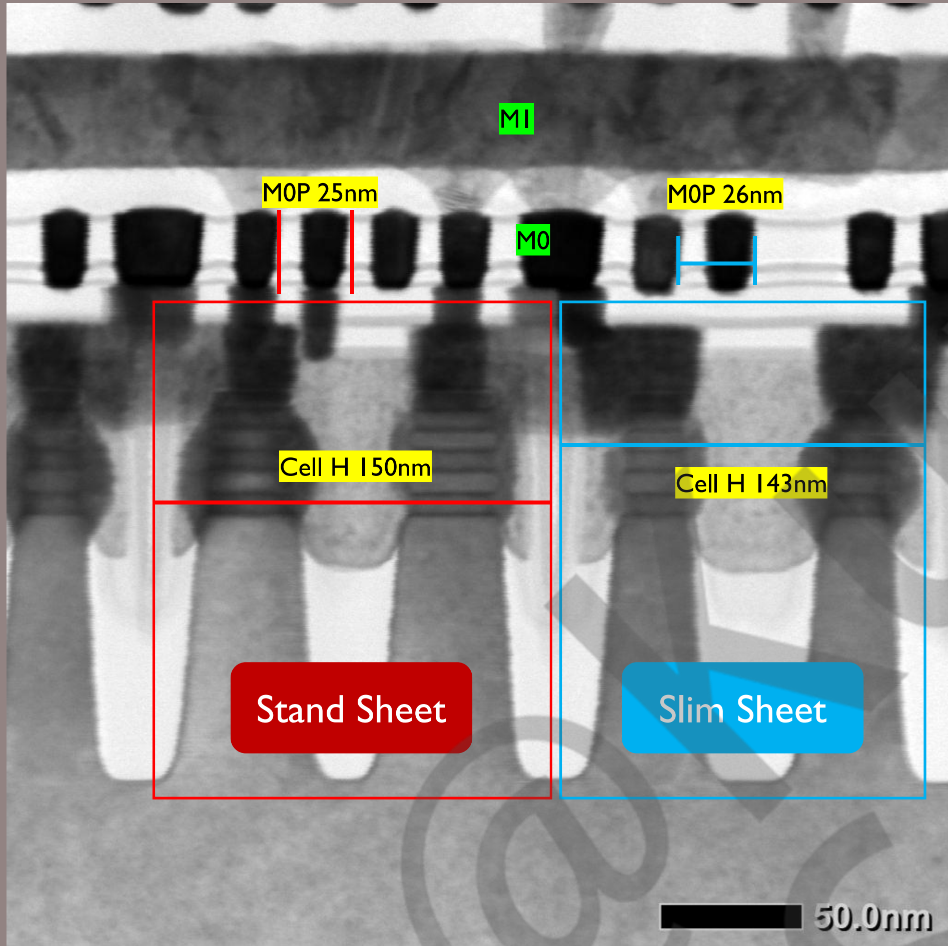
Metal Layer	Pitch	Thickness
M0	25nm/26nm	28nm
M1	33nm	44nm
M2	28nm/30nm	42nm
M3	38nm	44nm
M4	37nm/40nm	45nm
M5	84nm	48nm
M6	80nm	87nm
M7	84nm	80nm
M8	80nm	75nm
M9	87nm	80nm
M10	80nm	75nm
M11	100nm	80nm
M12	130nm	140nm
M13	130nm	140nm
M14	1620nm	1000nm
M15	4650nm	1000nm
M16(Top RDL)	?	2926nm

Min Metal Pitch =M0P(25nm)

M1 : CGP = 3 : 2

SAMPLE

Exynos2600(Samsung 2nm) BEOL-M0



0421-1 Y Cross 1-006

Metal Layer	Pitch
M0	25nm/26nm
M2	28nm/30nm

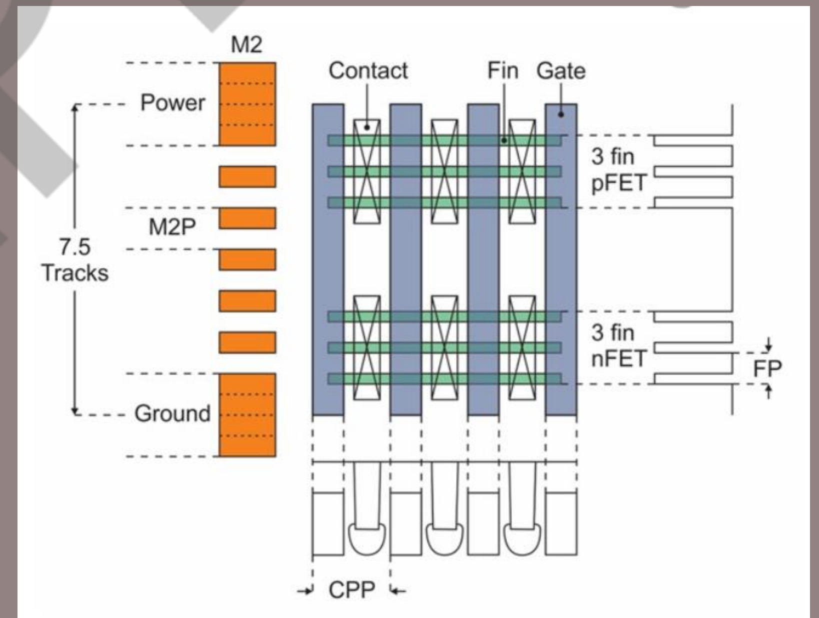
Cell H / M2P = Track

Stand Sheet 150nm

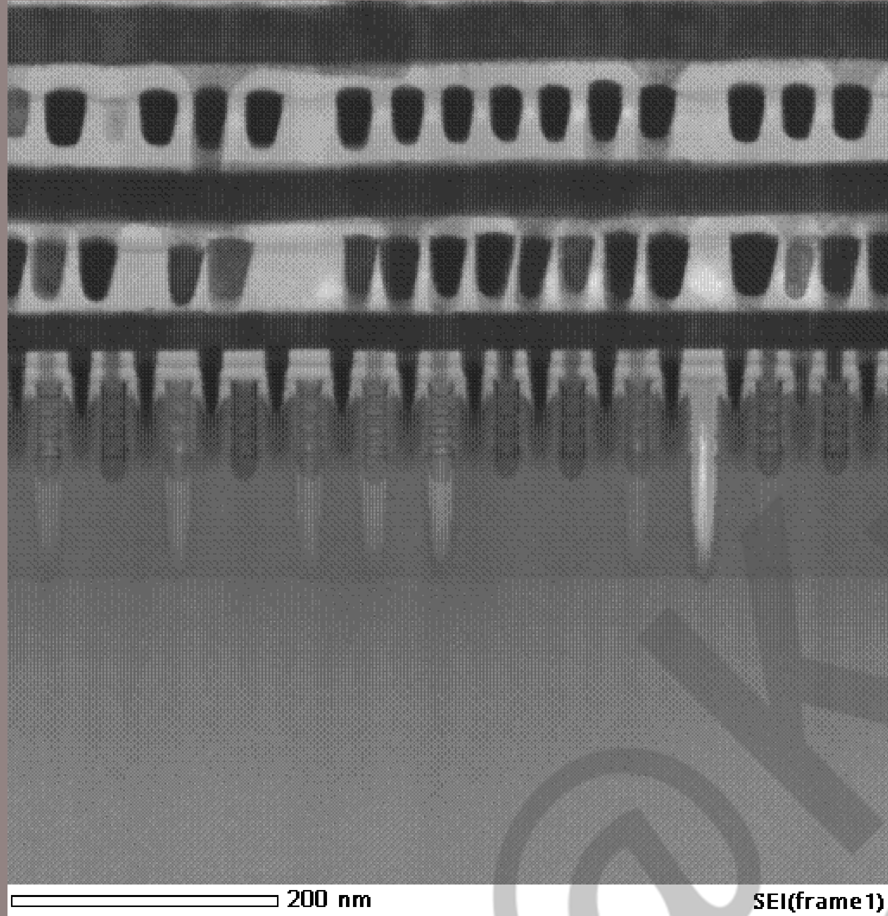
5Track uHD

Slim Sheet 143nm

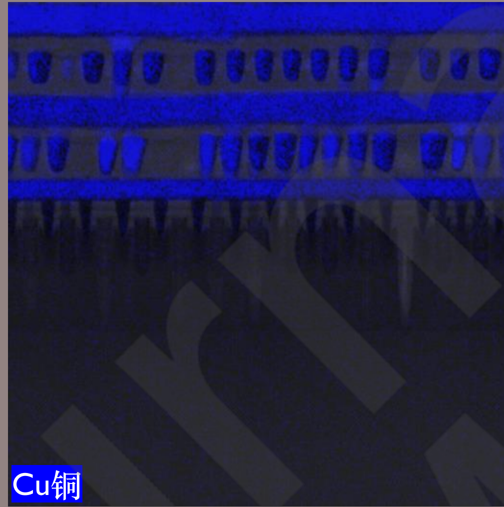
4.76Track uHD

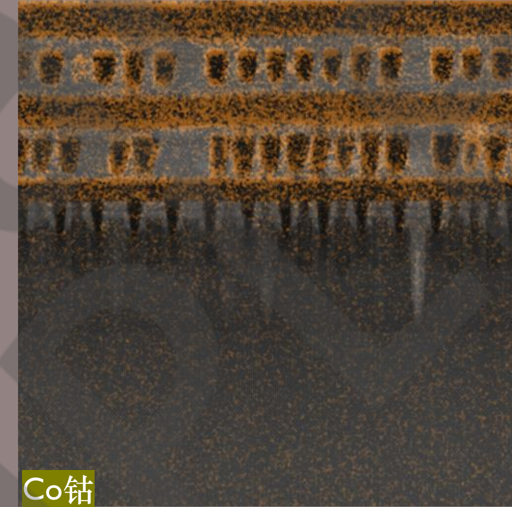


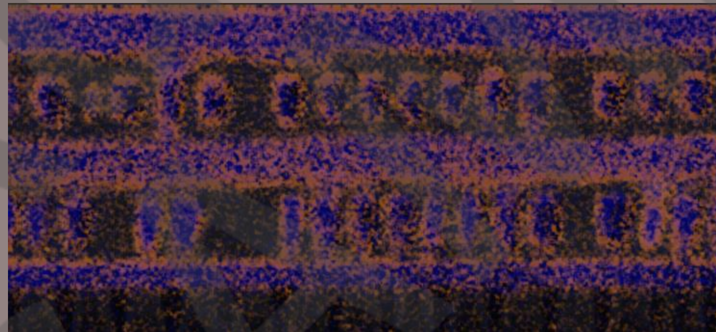
Exynos2600(Samsung 2nm) BEOL -EDS



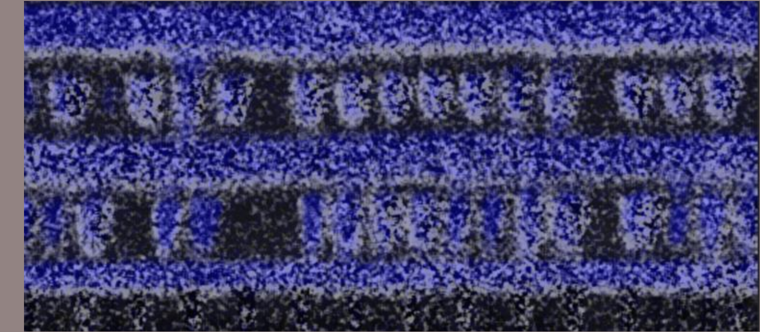
5-13min





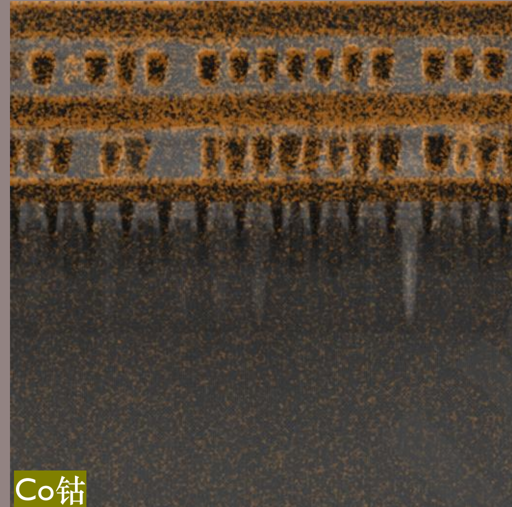


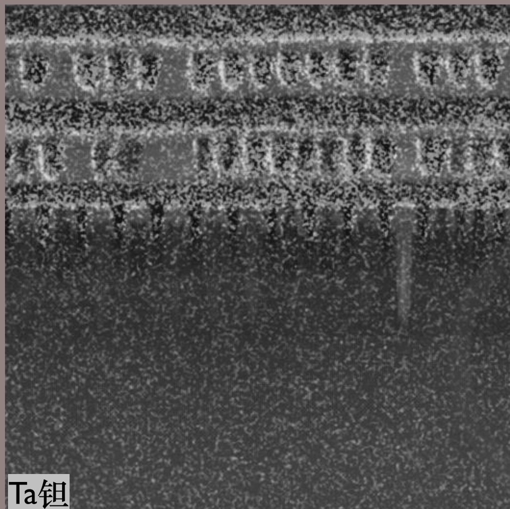
Cu+Co Overlay: Liner Conformality

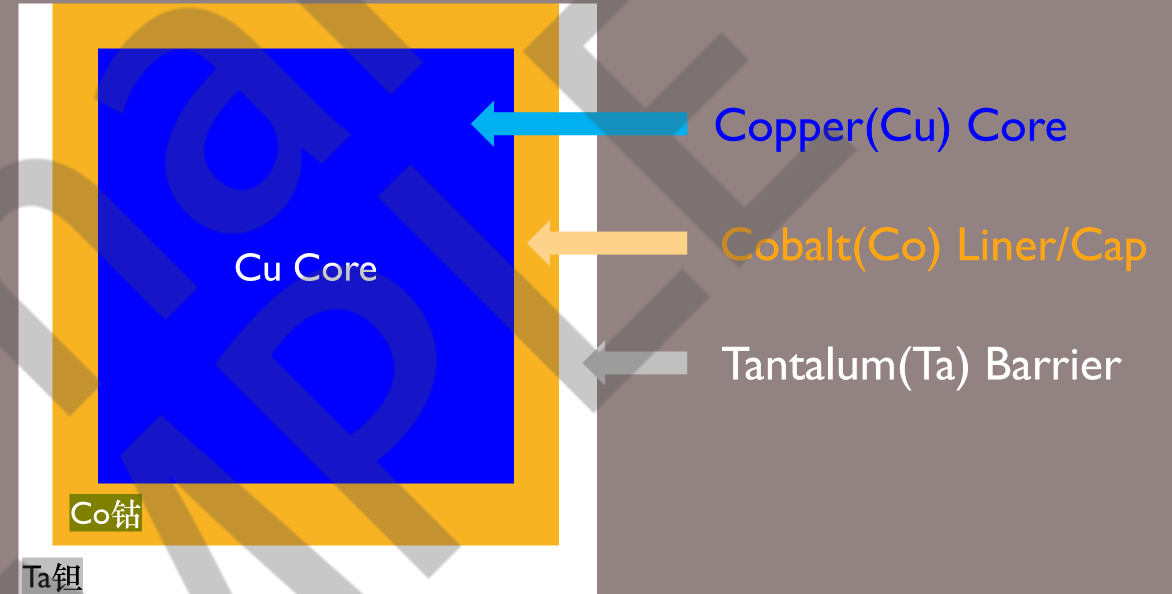


Cu+Ta Overlay: Barrier Integrity

Exynos2600(Samsung 2nm) BEOL -EDS







Cu (Copper Core): Positioned at the innermost part of the interconnect, acting as the primary conductor.

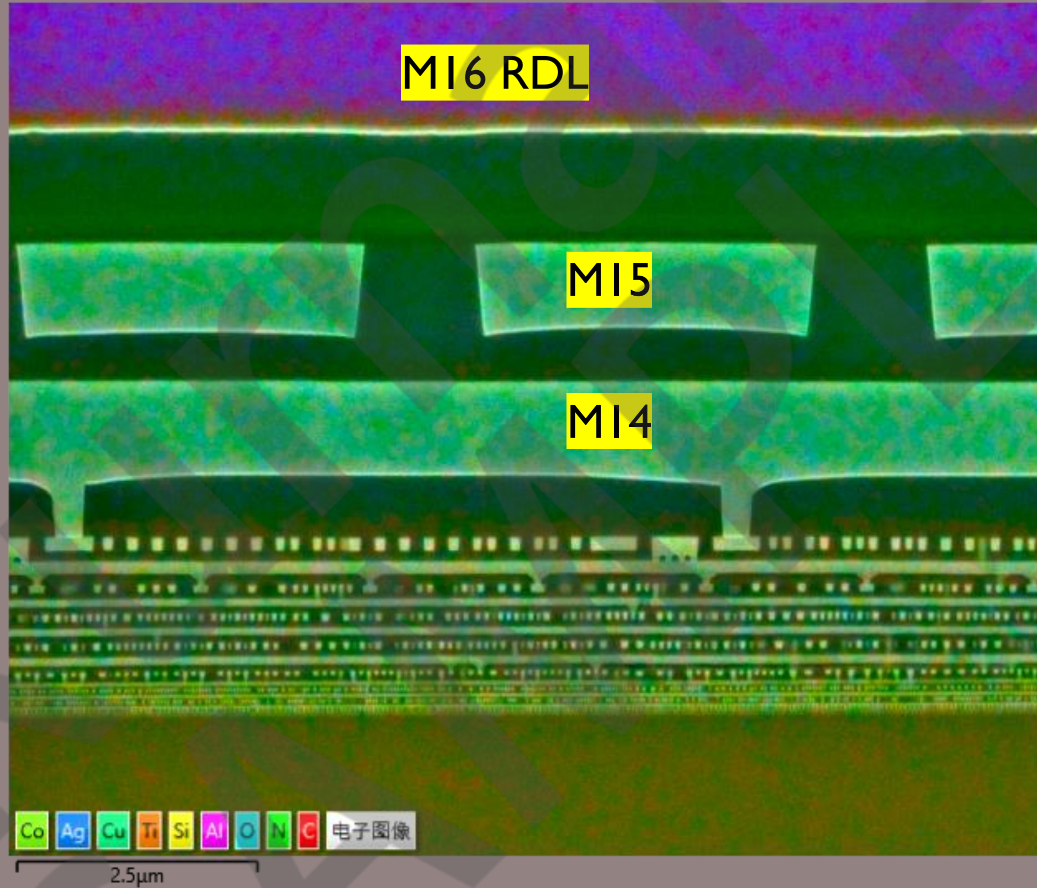
Co (Cobalt Liner & Cap):The conformal middle layer that reduces interface resistivity and mitigates Electromigration (EM) by suppressing interfacial voids.

Ta (Tantalum Barrier):The outermost diffusion barrier that prevents copper migration into the surrounding low-k dielectrics.

@Kurnal SAMPLE

Exynos2600(Samsung 2nm) BEOL -EDS

Metal Layer	element
M0	eCu (Cu+Co+Ta)
M1	eCu (Cu+Co+Ta)
M2	eCu (Cu+Co+Ta)
M3	eCu (Cu+Co+Ta)
M4	eCu (Cu+Co+Ta)
M5	eCu (Cu+Co+Ta)
M6	eCu (Cu+Co+Ta)
M7	eCu (Cu+Co+Ta)
M8	eCu (Cu+Co+Ta)
M9	eCu (Cu+Co+Ta)
M10	eCu (Cu+Co+Ta)
M11	eCu (Cu+Co+Ta)
M12	eCu (Cu+Co+Ta)
M13	eCu (Cu+Co+Ta)
M14	eCu (Cu+Co+Ta)
M15	eCu (Cu+Co+Ta)
M16(Top RDL)	Al+Ti Barrier



TiN Barrier Layer: Used as a diffusion barrier and adhesion layer for the Al RDL to prevent interdiffusion and ensure electrical stability.

Processor end

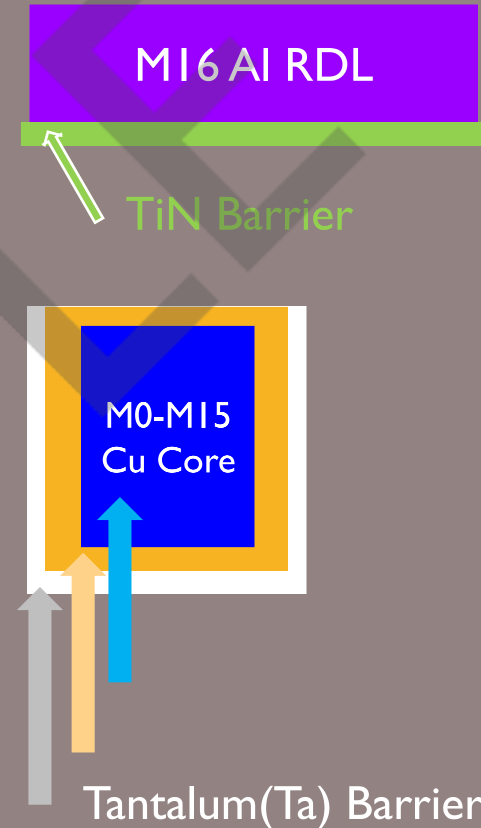
Exynos2600(Samsung 2nm)

@Kurnal SAMPLE

Processor end-BEOL

Metal Layer	Pitch	Thickness	element
M0	25nm/26nm	28nm	eCu (Cu+Co+Ta)
M1	33nm	44nm	eCu (Cu+Co+Ta)
M2	28nm/30nm	42nm	eCu (Cu+Co+Ta)
M3	38nm	44nm	eCu (Cu+Co+Ta)
M4	37nm/40nm	45nm	eCu (Cu+Co+Ta)
M5	84nm	48nm	eCu (Cu+Co+Ta)
M6	80nm	87nm	eCu (Cu+Co+Ta)
M7	84nm	80nm	eCu (Cu+Co+Ta)
M8	80nm	75nm	eCu (Cu+Co+Ta)
M9	87nm	80nm	eCu (Cu+Co+Ta)
M10	80nm	75nm	eCu (Cu+Co+Ta)
M11	100nm	80nm	eCu (Cu+Co+Ta)
M12	130nm	140nm	eCu (Cu+Co+Ta)
M13	130nm	140nm	eCu (Cu+Co+Ta)
M14	1620nm	1000nm	eCu (Cu+Co+Ta)
M15	4650nm	1000nm	eCu (Cu+Co+Ta)
M16(Top RDL)	?	2926nm	Al+Ti Barrier

Min Metal Pitch =M0P(25nm)



The die process uses 17 metal layers: 16 Cu + 1 Al

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Processor end-BEOL-VS Samsung

SF2	Pitch
M0	25nm/26nm
M1	33nm
M2	30nm
M3	38nm
M4	37nm/40nm
M5	84nm
M6	80nm

Exynos 2600(SF2)

Min Metal =M0P(25nm)

M2 Pitch =30nm

SF3	Pitch
M0	28nm/30nm
M1	33nm
M2	28.5nm
M3	37nm
M4	45nm
M5	53.5nm
M6	100nm

Exynos W1000(SF3)

Min Metal =M0P(28nm)

M2 Pitch =28.5nm

SF4	Pitch
M0	28nm
M1	36nm
M2	33nm
M3	44nm
M4	76nm
M5	76nm
M6	76nm

Exynos 2200(SF4)

Min Metal =M0P(28nm)

M2 Pitch =33nm

SF5	Pitch
M0	40nm
M1	36nm
M2	36nm
M3	
M4	
M5	
M6	

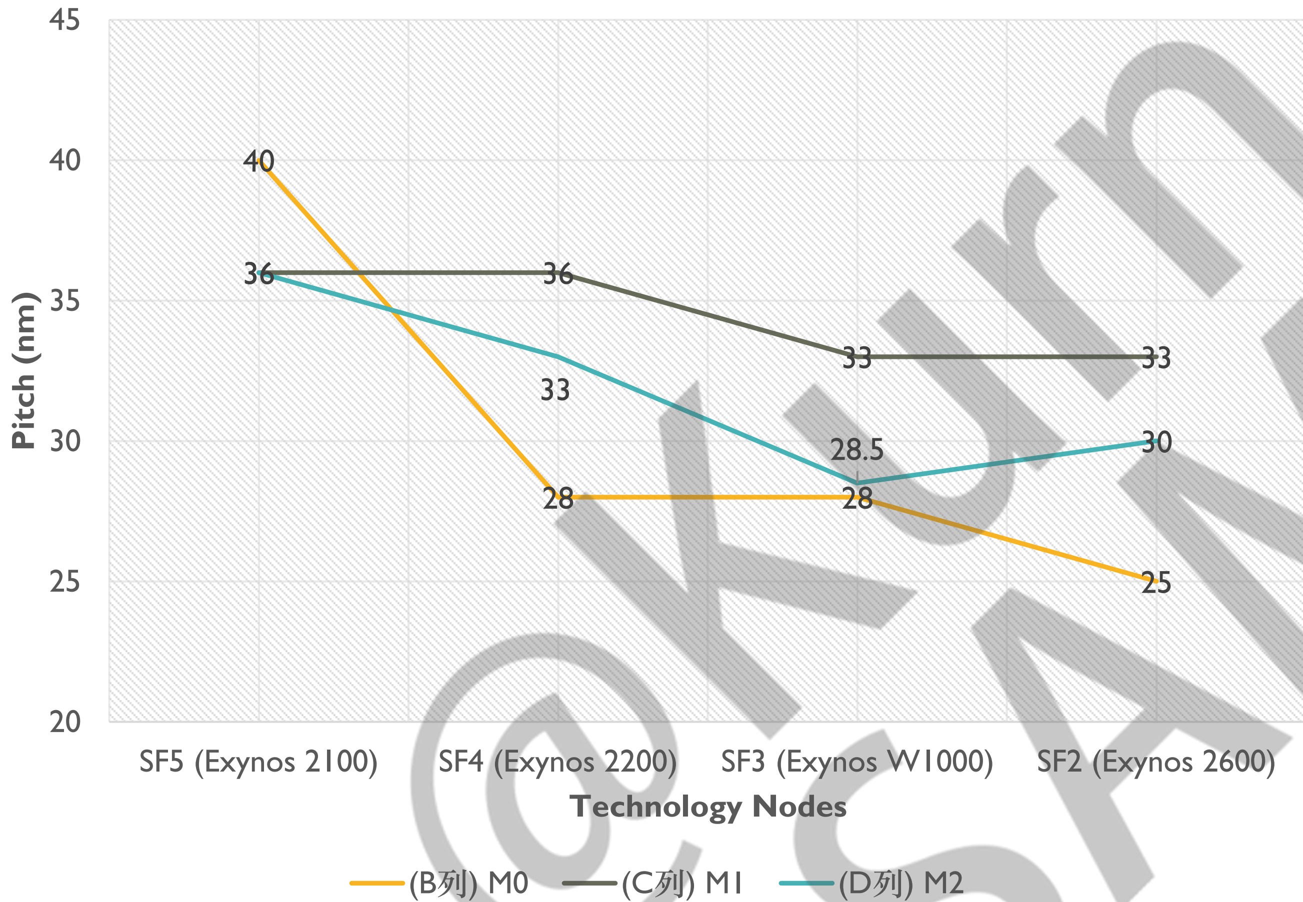
Exynos 2100(SF5)

Min Metal =M2P(36nm)

M2 Pitch =36nm

@Kurnal SAMPLE

Processor end-BEOL-VS Samsung



SF2	Pitch
M0	25nm/26nm
M1	33nm
M2	30nm

SF3	Pitch
M0	28nm/30nm
M1	33nm
M2	28.5nm

SF3 → SF2: M0 0.9x; M1 Same; M2 1.05x

SF3	Pitch
M0	28nm/30nm
M1	33nm
M2	28.5nm

SF4	Pitch
M0	28nm
M1	36nm
M2	33nm

SF4 → SF3: M0 Same; M1 0.92x; M2 0.86x

SF4	Pitch
M0	28nm
M1	36nm
M2	33nm

SF5	Pitch
M0	40nm
M1	36nm
M2	36nm

SF5 → SF4: M0 0.7x; M1 Same; M2 0.92x

@Kurnal SAMPLE

Processor end-BEOL-VS High End

Exynos 2600(SF2)

SEC SF2	Pitch
M0	25nm/26nm
M1	33nm
M2	30nm
M3	38nm
M4	37nm/40nm

Min Metal =M0P(25nm)

M2 Pitch =30nm

M1 : CGP = 3:2

GAA

Exynos W1000(SF3)

SEC SF3	Pitch
M0	28nm/30nm
M1	33nm
M2	28.5nm
M3	37nm
M4	45nm

Min Metal =M0P(28nm)

M2 Pitch =28.5nm

M1 : CGP = 3:2

GAA

Panter Lake(18A)

Intel 18A	Pitch
FM0	36nm
FM1	50nm
FM2	36nm
FM3	40nm
FM4	40nm

Min Metal =M0P(36nm)

M2 Pitch =36nm

M1 : CGP = 1:1

GAA + BSPDN

D9500(N3P)

TSMC N3P	Pitch
M0	23nm
M1	48nm/54nm
M2	27nm
M3	38nm
M4	35nm

Min Metal =M0P(23nm)

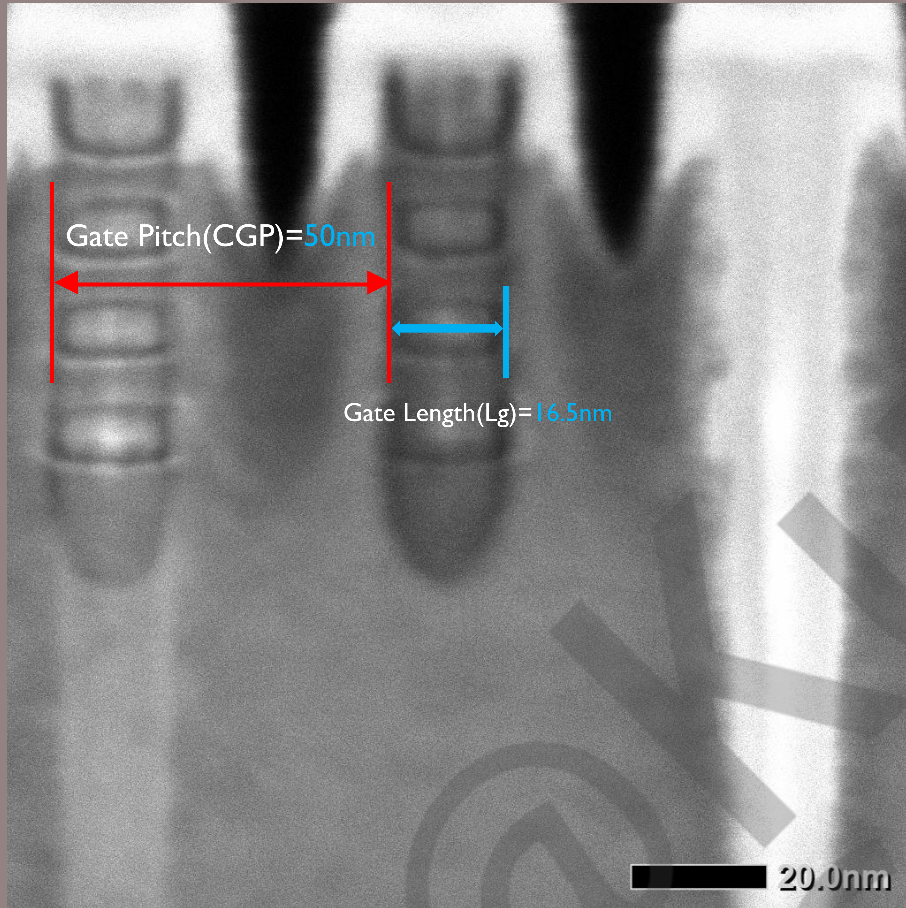
M2 Pitch =27nm

M1 : CGP = 1:1

FinFET

@Kurnal SAMPLE

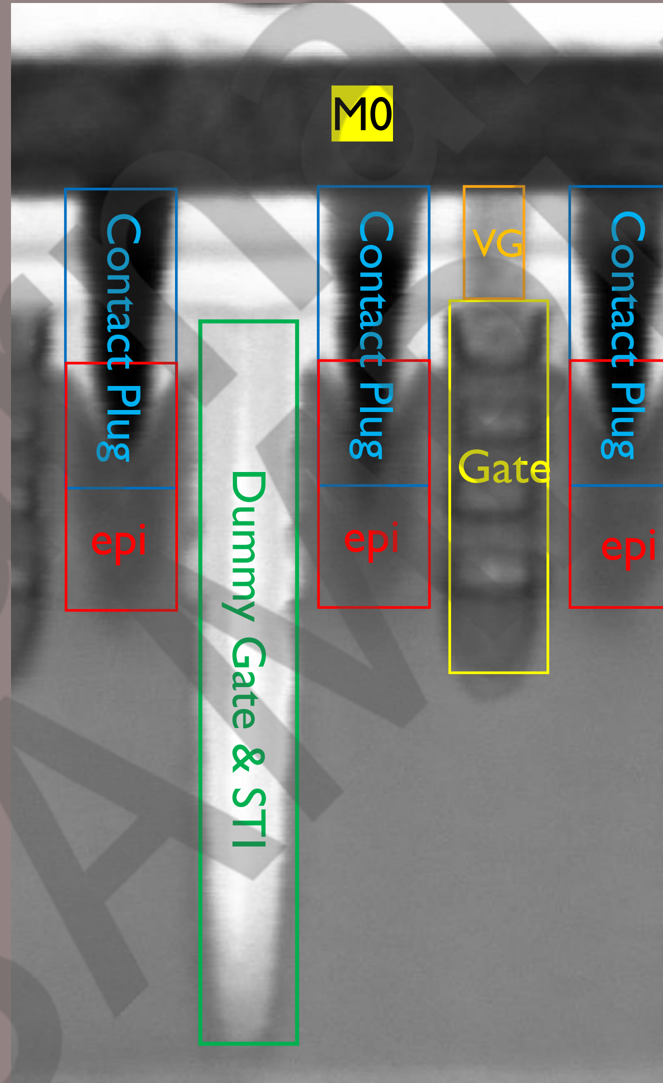
Processor end-Gate cut

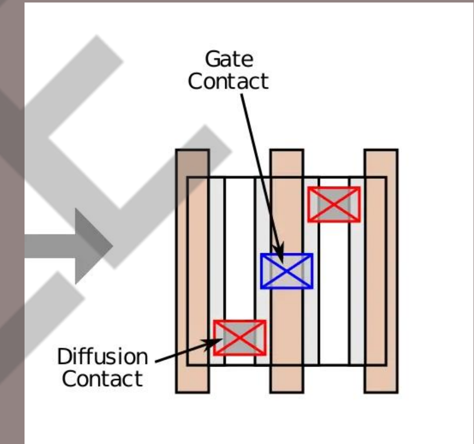


0421-1 X Cross 2-003

Gate Pitch=50nm

Gate Length=16.5nm





Use COAG

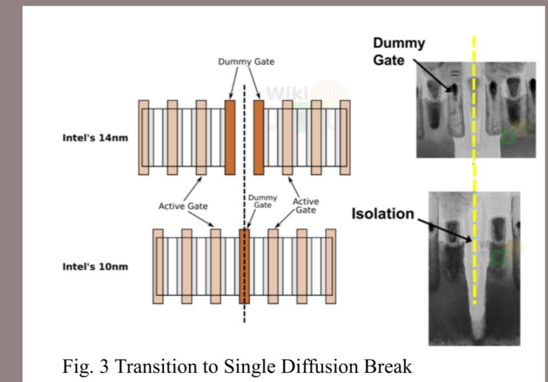
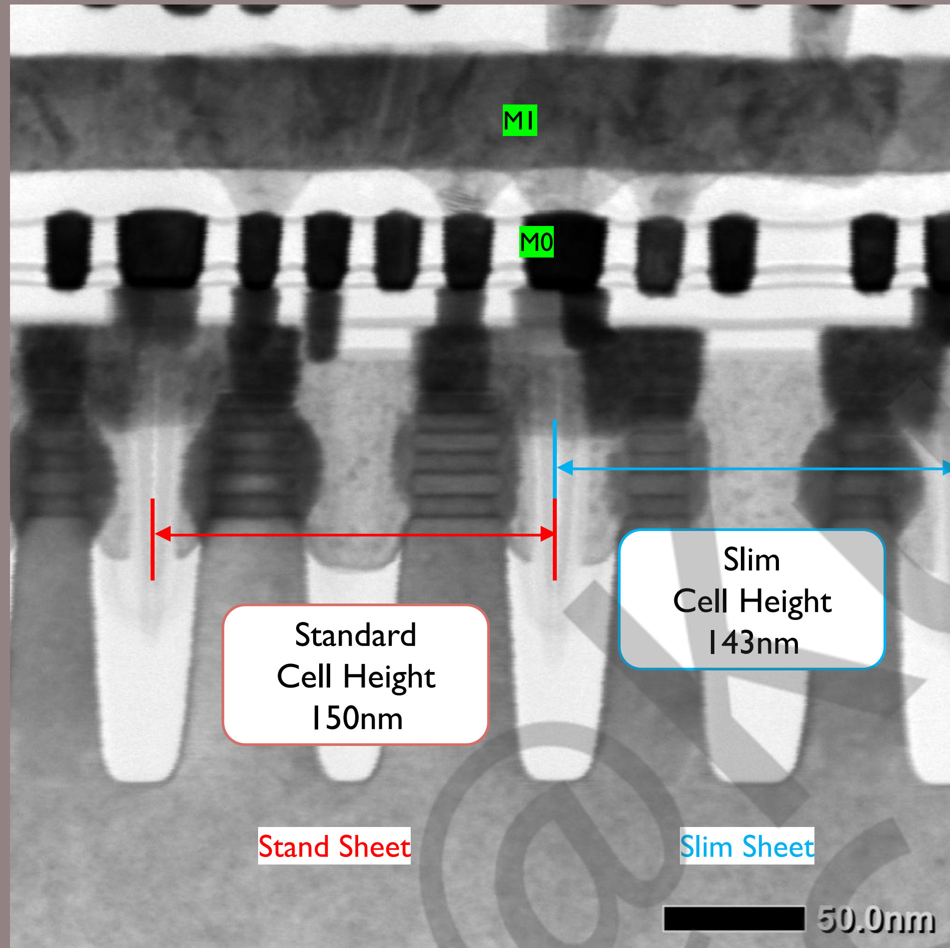


Fig. 3 Transition to Single Diffusion Break

Use Single Diffusion Break

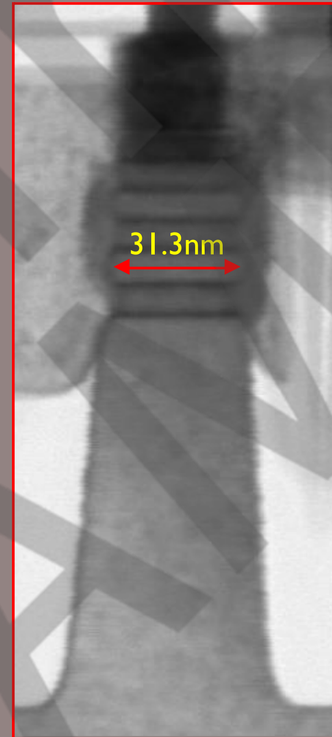
Processor end-FET Cut



0421-1 Y Cross 1-006

Stand Sheet
150nm

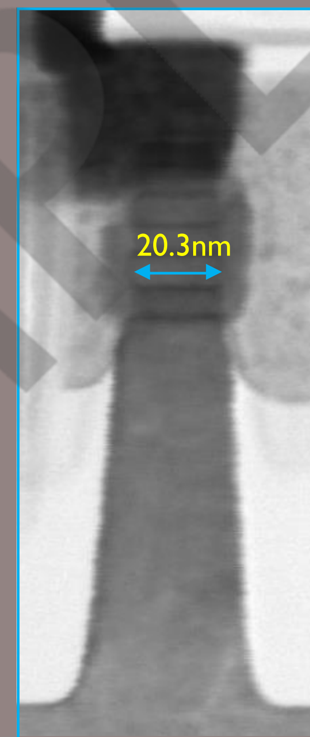
5Track
uHD



Stand Sheet

Slim Sheet
143nm

4.76Track
uHD



Slim Sheet

Logic Density

Exynos2600(Samsung 2nm)

@Kurnal SAMPLE

Processor end-Transistor

半导体工艺指标

Logic Transistor Density

// NAND2 + SFF Weighted Metric · Intel Standard

// 输入参数

Cell Height (单元高度)
150 nm

Gate Pitch (栅极间距)
50 nm

Standard Formula
Density = 0.6 × (4 / (H × P × 3)) + 0.4 × (32 / (H × P × 19))

// 扩散中断方案 (Diffusion Break)

SDB	DDB	MDB
单扩散中断 (SDB)	双扩散中断 (DDB)	混合扩散中断 (MDB)
NAND2: ÷ (H × P × 3) SFF: ÷ (H × P × 19) Tr(SFF) = 32	NAND2: ÷ (H × P × 4) SFF: ÷ (H × P × 20) Tr(SFF) = 32	(SDB + DDB) / 2 Avg Of Both Results

// 数据详情

NAND2 密度	SFF 密度	Total Density
106.67 MT/mm²	89.82 MT/mm²	196.49 MT / mm²

半导体工艺指标

Logic Transistor Density

// NAND2 + SFF Weighted Metric · Intel Standard

// 输入参数

Cell Height (单元高度)
143 nm

Gate Pitch (栅极间距)
50 nm

Standard Formula
Density = 0.6 × (4 / (H × P × 3)) + 0.4 × (32 / (H × P × 19))

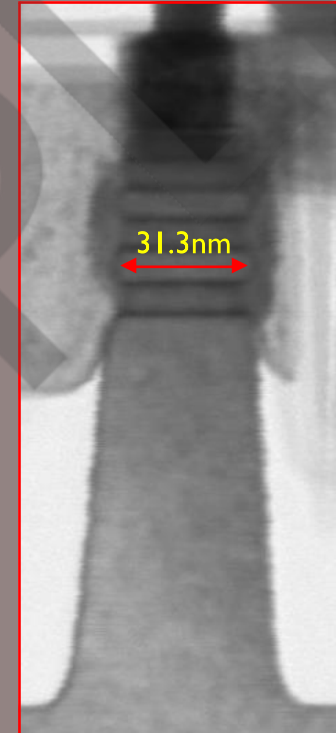
// 扩散中断方案 (Diffusion Break)

SDB	DDB	MDB
单扩散中断 (SDB)	双扩散中断 (DDB)	混合扩散中断 (MDB)
NAND2: ÷ (H × P × 3) SFF: ÷ (H × P × 19) Tr(SFF) = 32	NAND2: ÷ (H × P × 4) SFF: ÷ (H × P × 20) Tr(SFF) = 32	(SDB + DDB) / 2 Avg Of Both Results

// 数据详情

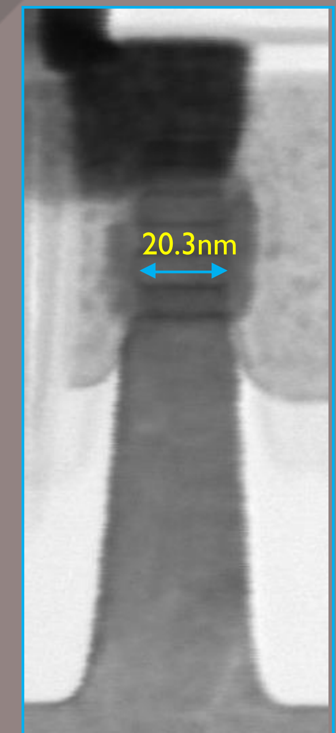
NAND2 密度	SFF 密度	Total Density
111.89 MT/mm²	94.22 MT/mm²	206.11 MT / mm²

Stand Sheet
196.49Mtr/mm2



Stand Sheet

Slim Sheet
206.11Mtr/mm2



Slim Sheet

	18A HP	18A HD	SF3E HD	SF2 UHD	N3E HD	N3P HD	N2 HD	2HP HD	2HP HP
Fin/GAA	GAA+BSPDN	GAA+BSPDN	GAA	GAA	FinFET	FinFET	GAA	GAA	GAA
Track	5T	5T	6T	6T	6.5	6.5	5T/6T	?	?
Gate Channel (nm)	14	14	?	16.5	?	?	?	8	8
Gate Pitch (nm)	50	50	48	50	48	47	48	45	45
Fin Pitch (nm)	"80" GAAfet	“70" GAAfet	“?“ GAAfet	“?“ GAAfet	26	26	?	?	?
M2P (nm)	36	32	28	28	26	26	26	?	?
Cell Height (nm)	180	160	168	143	M143	M140	130	138	184
Logic Density (MTr/mm^2)	163.74	184.21	182.75	206.11	214.7	223.96	236.17	237.31	177.98

@Kurnal SAMPLE

Processor end-Transistor

Exynos 2600(SF2)

SEC SF2	UHD
Cell H	143nm
Track	5T
Gate Pitch	50nm
Logic Trs(Min)	206.11Mtr

Exynos W1000(SF3)

SEC SF3	HD
Cell H	168nm
Track	6T
Gate Pitch	48nm
Logic Trs(Min)	182.75Mtr

Panter Lake(18A)

Intel 18A	HD
Cell H	160nm
Track	5T
Gate Pitch	50nm
Logic Trs(Min)	184.21Mtr

D9500(N3P)

TSMC N3P	UHD
Cell H	140nm
Track	5.3T
Gate Pitch	47nm
Logic Trs(Min)	223.96Mtr

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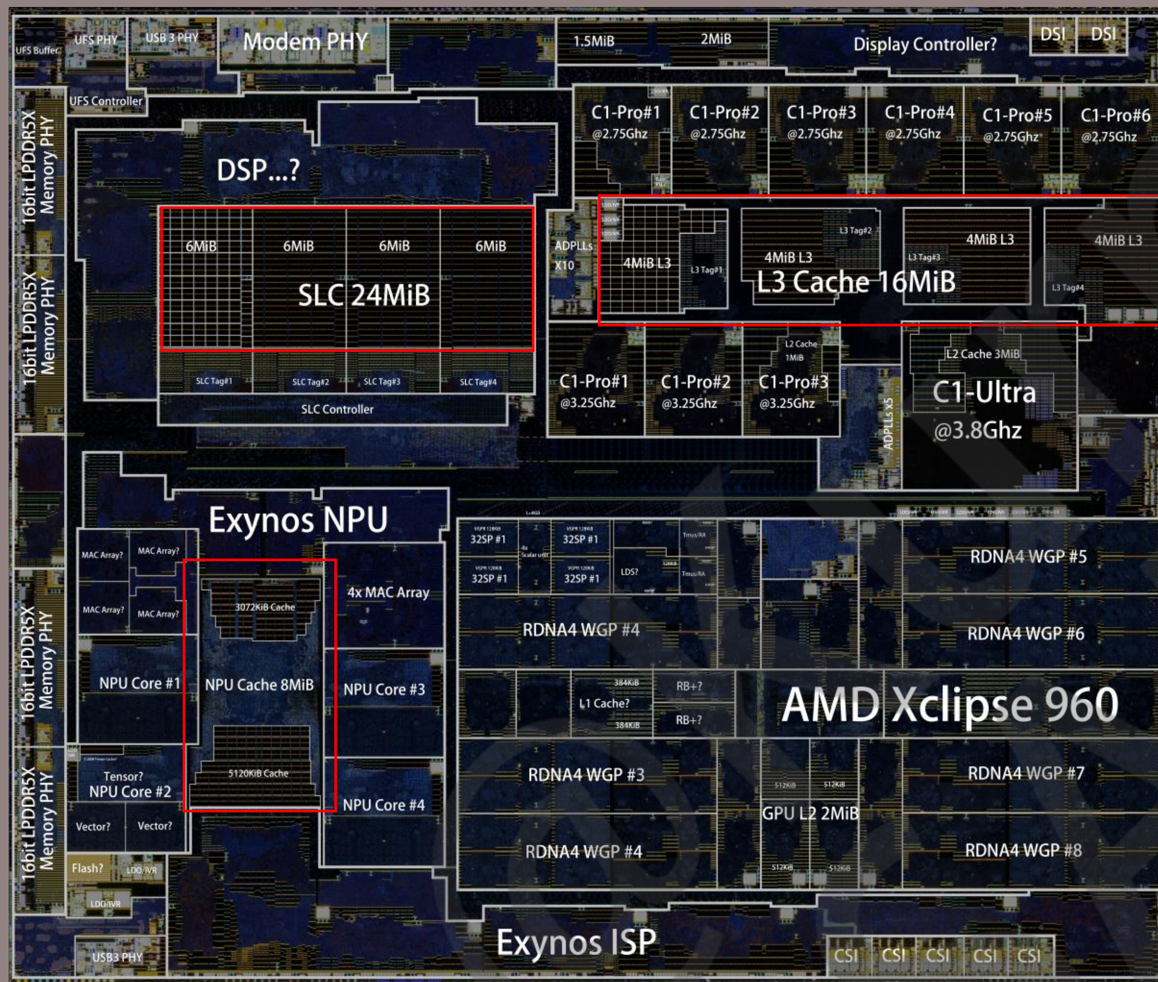
SRAM Density

Exynos2600(Samsung 2nm)

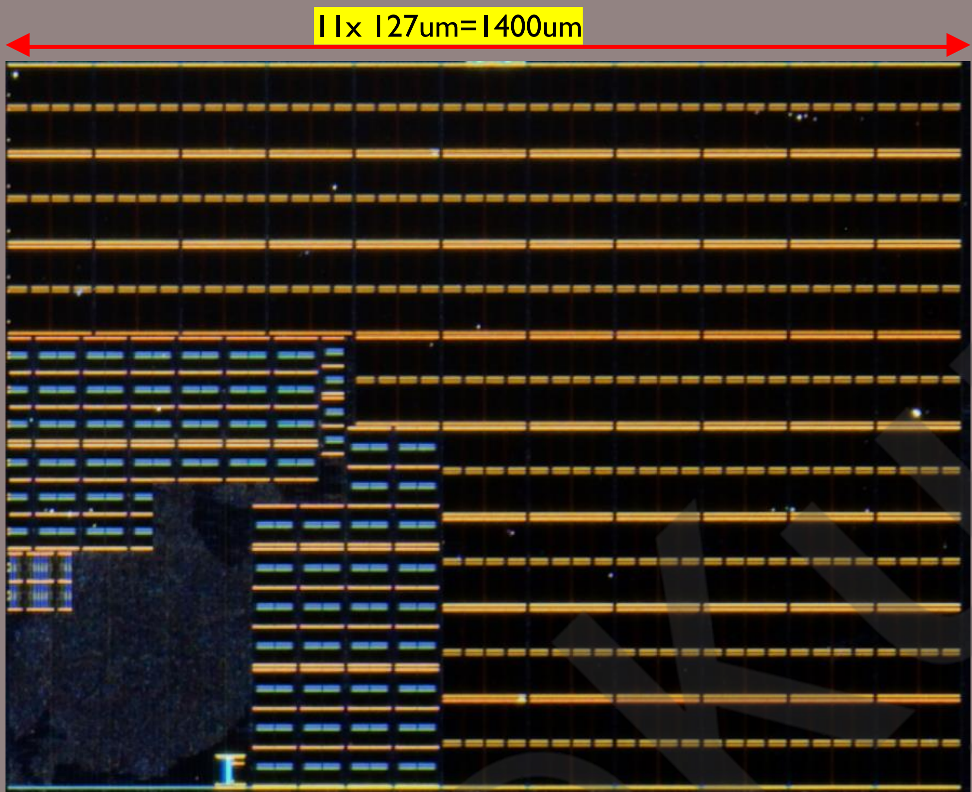
@Kurnal SAMPLE

SRAM Density-SF2-CPU L3



4MiB L3 (64 Block SF2 SRAM IP #1)

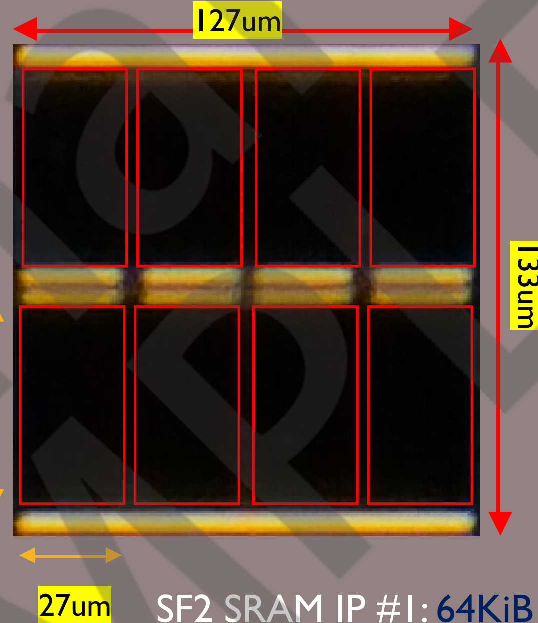
SRAM Density-SF2-CPU L3



4MiB L3 (64 Block SF2 SRAM IP #1)

29.538Mb/mm2

54um



SF2 SRAM IP #1: 64KiB

SRAM ARRAY

Field	Value	Unit
NUMBER OF ARRAYS	8	#
ARRAY LENGTH	27	µm
ARRAY WIDTH	54	µm

SRAM BLOCK

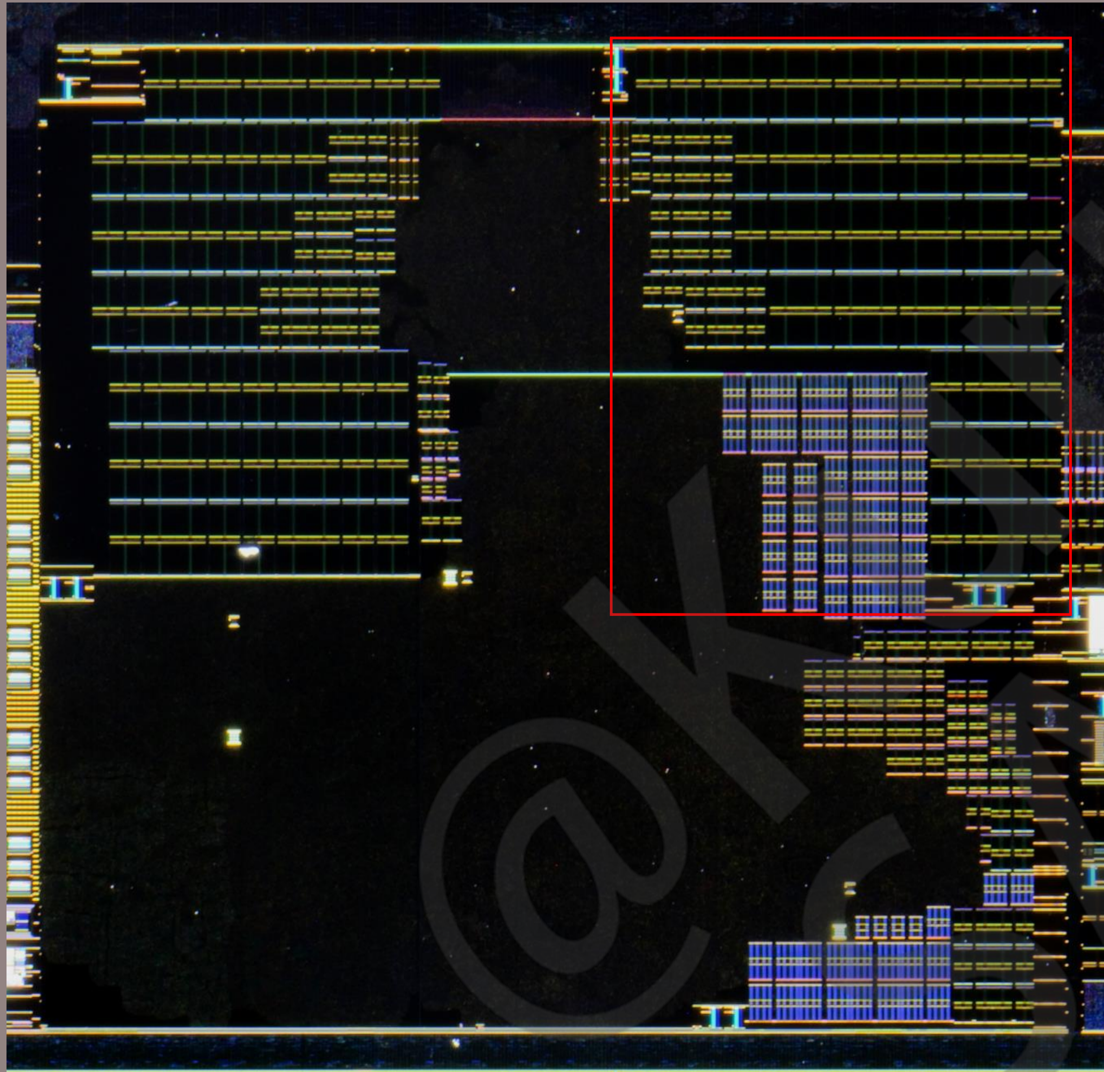
Field	Value	Unit
BLOCK LENGTH	127	µm
BLOCK WIDTH	133	µm
TOTAL CAPACITY	64	KiB

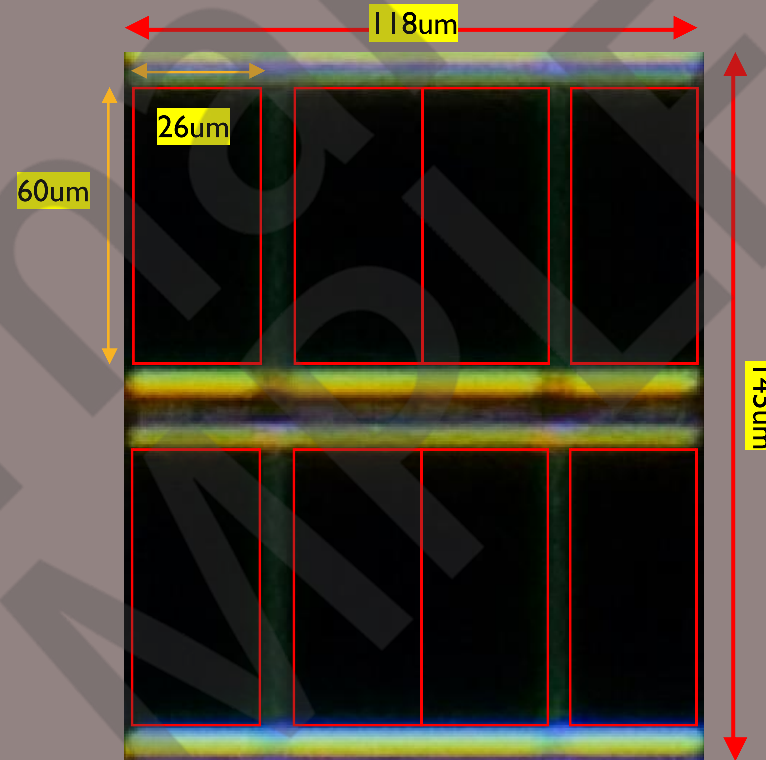
RESULTS OVERVIEW

MACRO DENSITY	ARRAY PROPORTION	BIT CELL SIZE
31.04 Mbit / mm²	69.1 %	0.0222 µm² / bit

BLOCK AREA	TOTAL ARRAY AREA	CAPACITY	BITS / MM²
16,891.0 µm²	11,664.0 µm²	524,288 bit	31.039 bits / µm²

SRAM Density-SF2-CPU L2(C1 Ultra)





SRAM ARRAY

NUMBER OF ARRAYS: 8 #

ARRAY LENGTH: 26 µm

ARRAY WIDTH: 60 µm

SRAM BLOCK

BLOCK LENGTH: 118 µm

BLOCK WIDTH: 145 µm

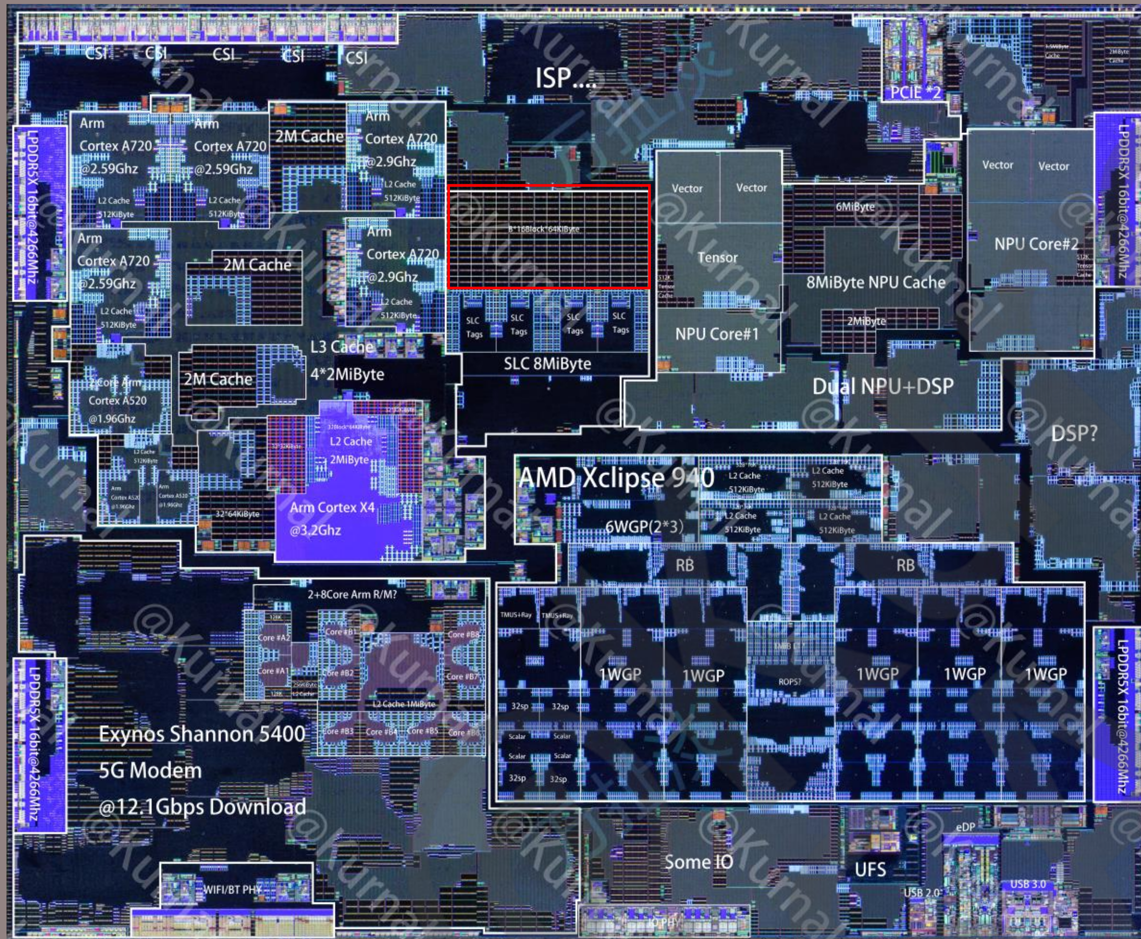
TOTAL CAPACITY: 64 KiB

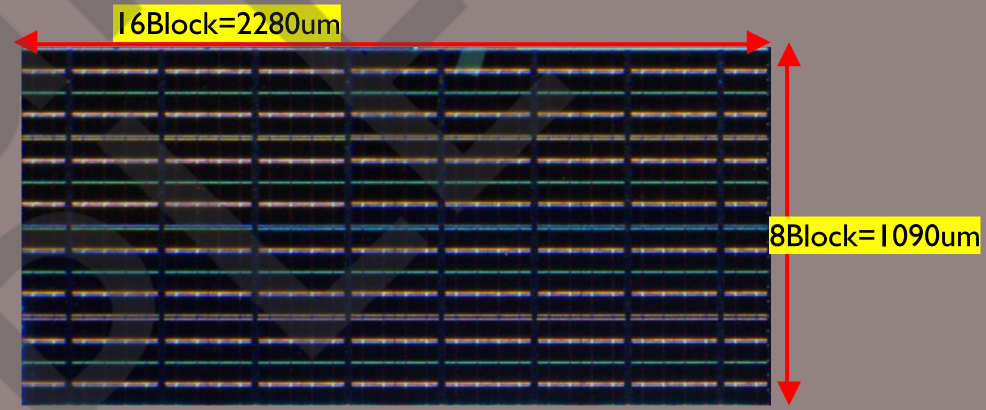
SF2 SRAM IP #2 64KiB

MACRO DENSITY	ARRAY PROPORTION	BIT CELL SIZE
30.64 Mbit / mm²	72.9 %	0.0238 µm² / bit

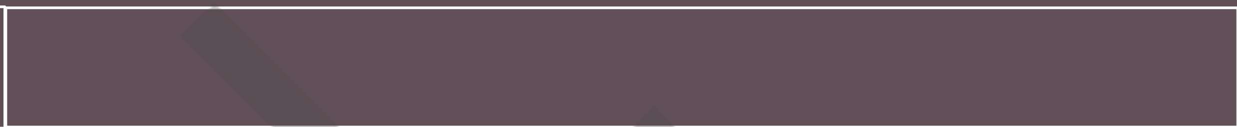
BLOCK AREA	TOTAL ARRAY AREA	CAPACITY	BITS / MM²
17,110.0 µm²	12,480.0 µm²	524,288 bit	30.642 bits / µm²

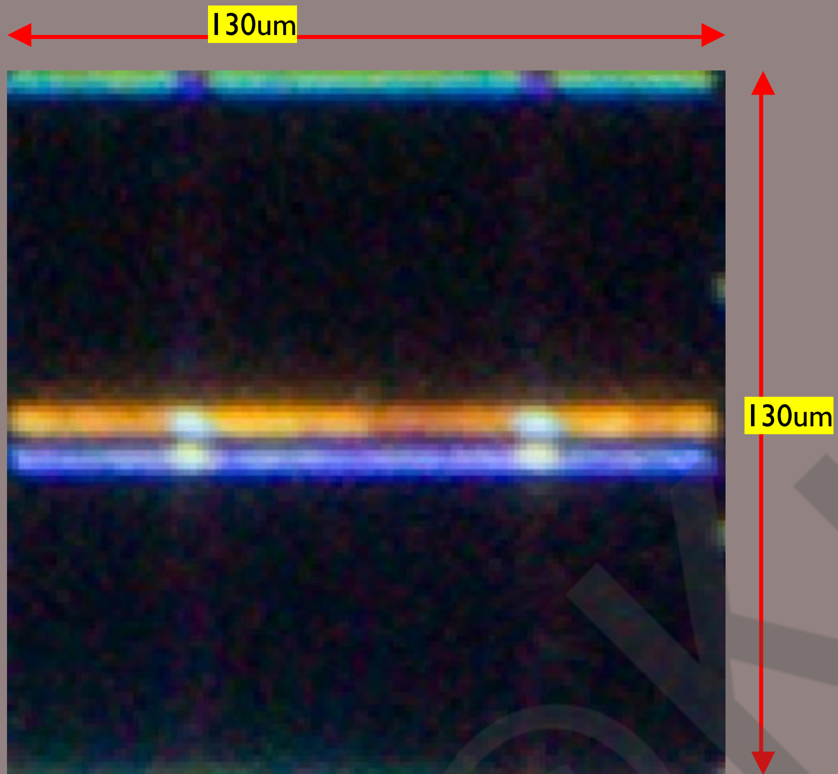
SRAM Density-SF4





SF4 SRAM IP #1: 64KiB





SRAM 密度 计算器

宏密度 · 阵列占比 · bit Cell 尺寸

SRAM 模块

块长度: 130 μm

块宽度: 130 μm

总容量: 64 KiB

SRAM 阵列

阵列数量: 8 #

阵列长度: 57 μm

阵列宽度: 29 μm

结果总览

宏密度	阵列占比	BIT CELL 尺寸
31.02 Mbit / mm²	78.2 %	0.0252 μm² / bit

块面积	总阵列面积	容量	BITS / MM²
16,900.0 μm²	13,224.0 μm²	524,288 bit	31.023 bits / μm²

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