

# Xiaomi Watch Xring chip

Chip analyze

V1



@Kurnal



Version	Date	Updates	Author
V0	2025/05/10 21:26	Working	Kurnal
V1	2025/05/14 01:51	Finish	Kurnal
B站工坊			

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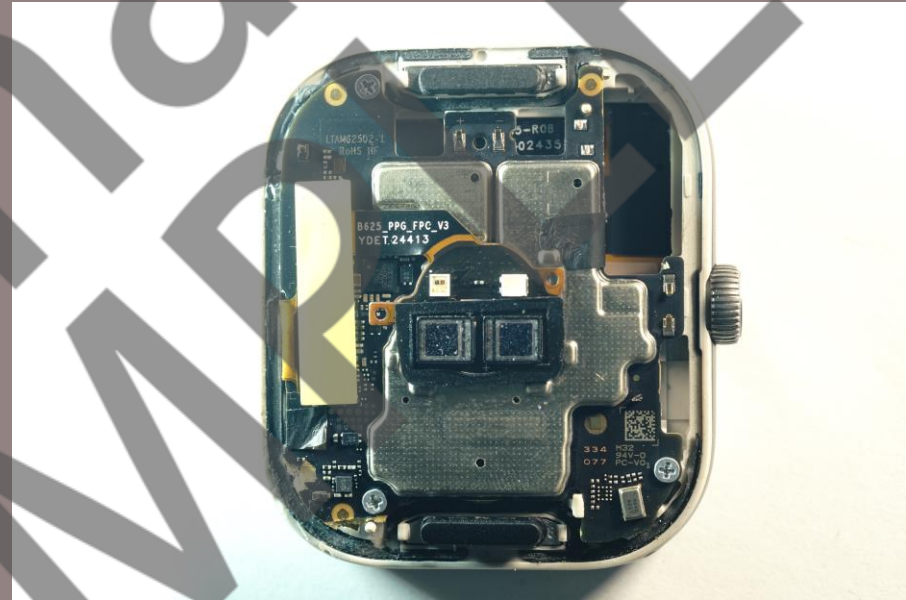
This report is not for commercial use

# Mother board

Component analyze

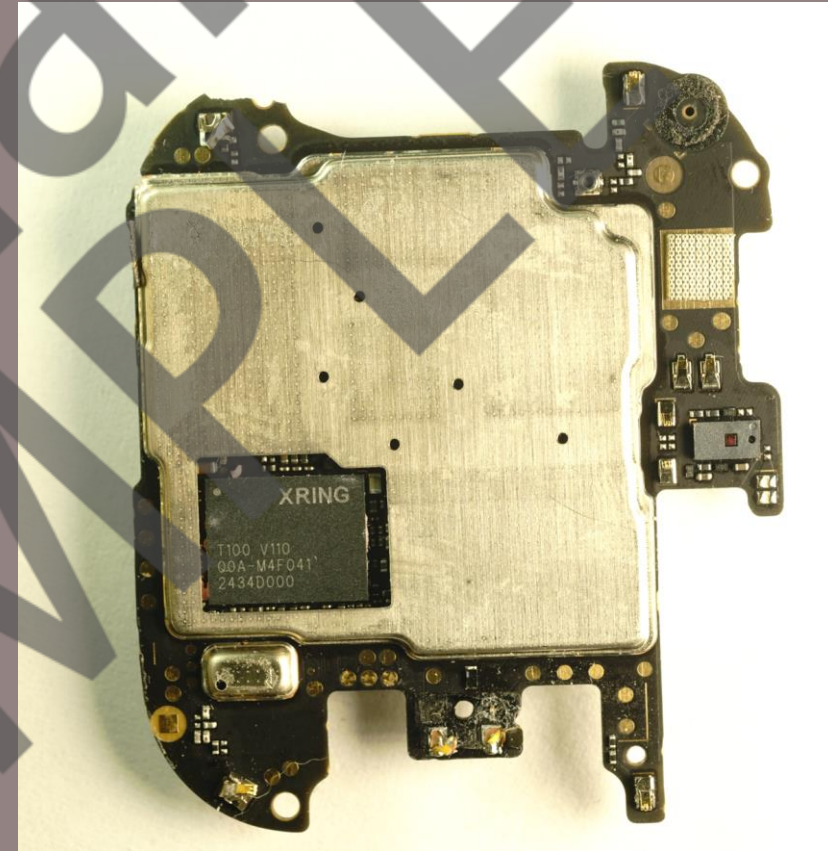


Red Mi Watch 5 Esim





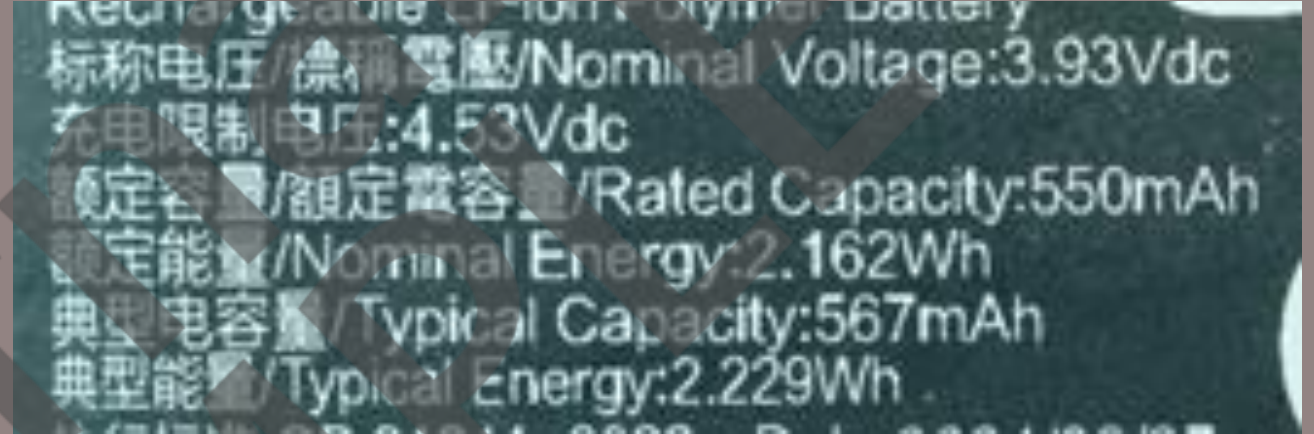
Battery



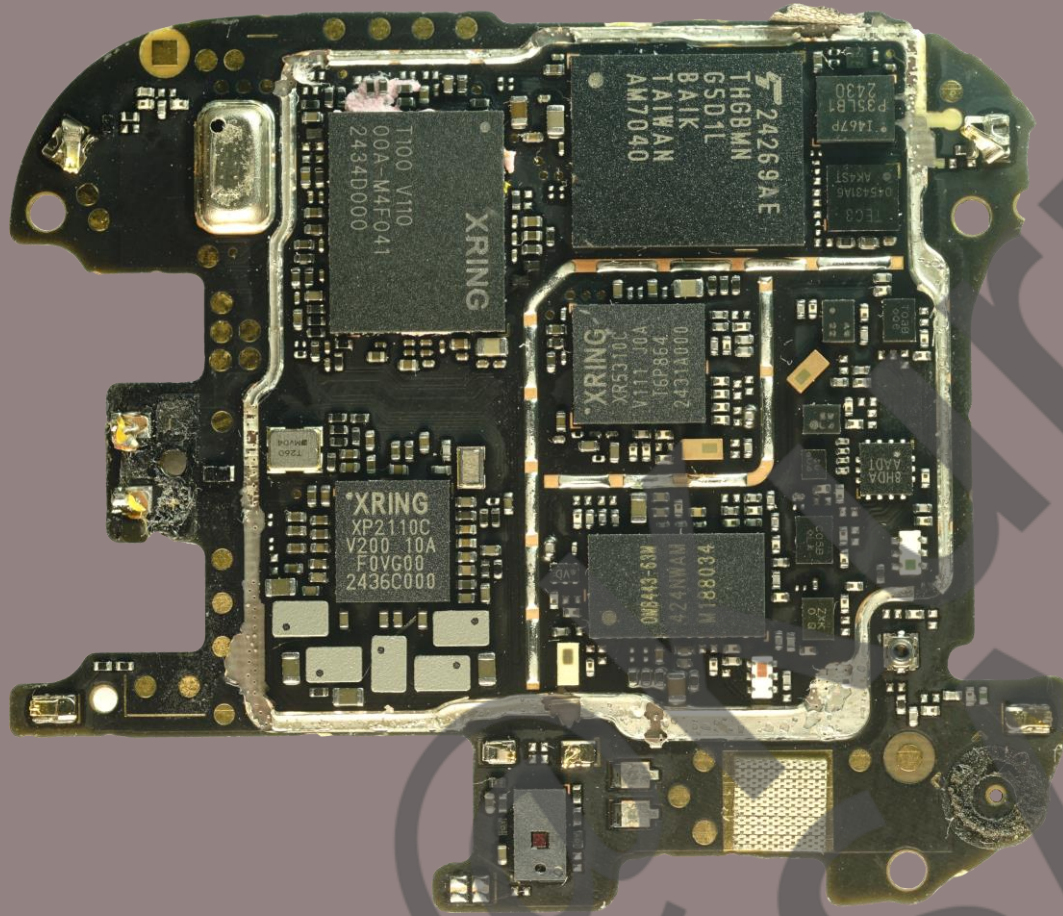
MotherBoard



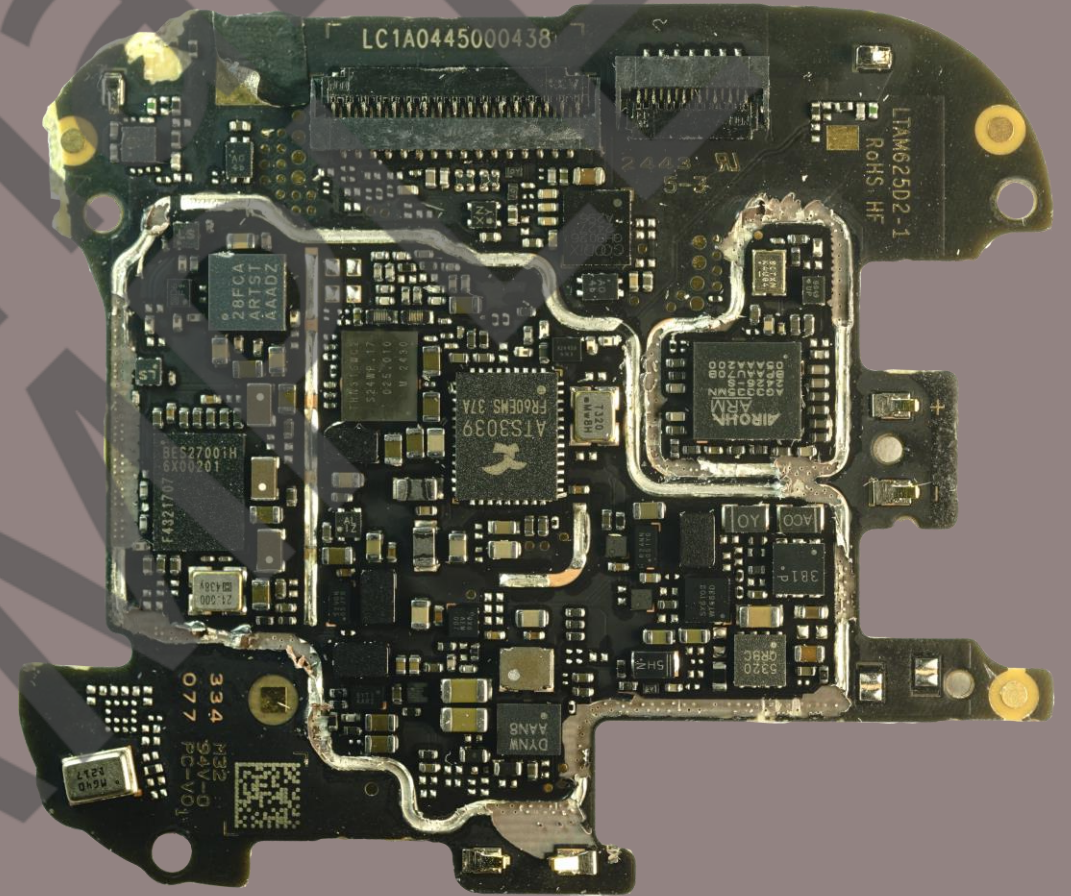
Battery



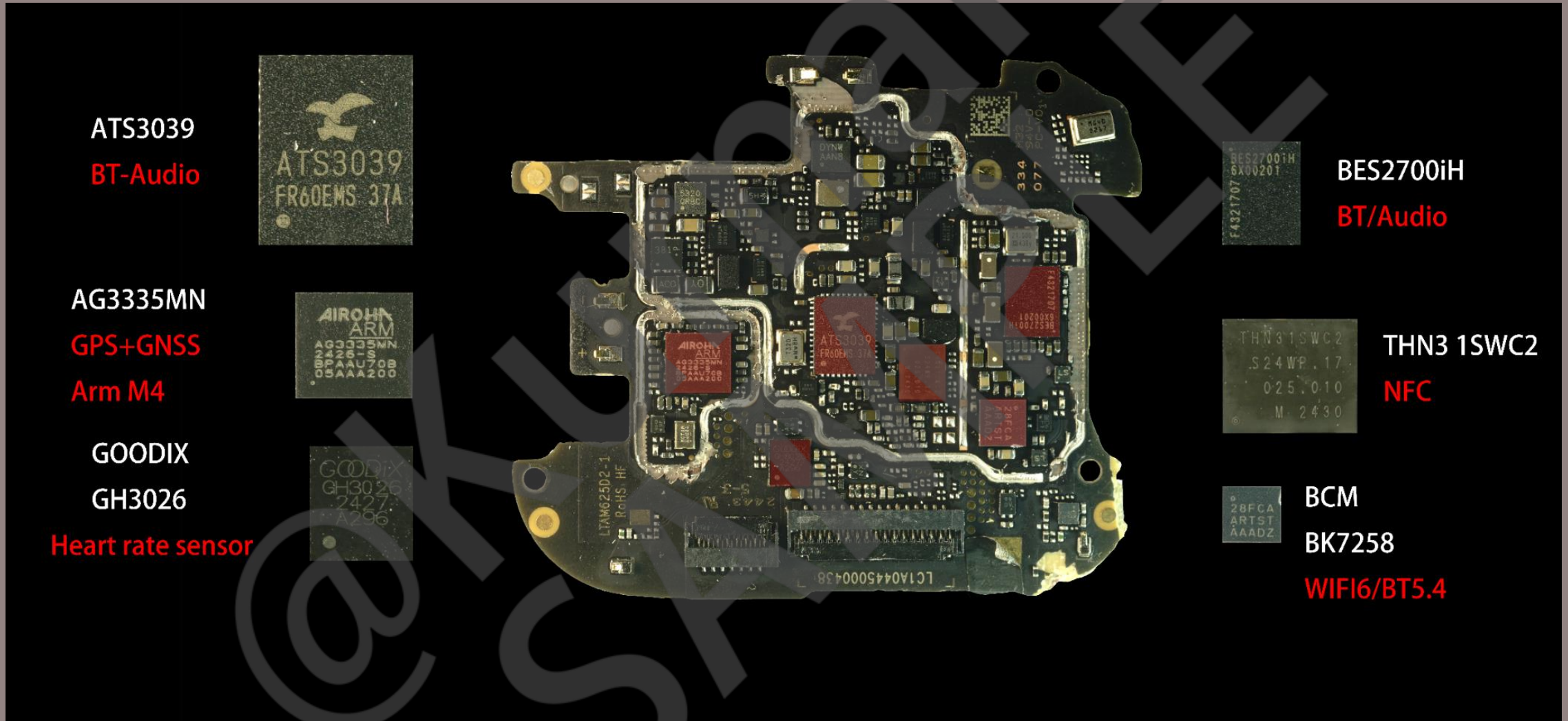
550mAh/2.162Wh  
567mAh/2.229Wh



PCB Top view



PCB Bottom view



ATS3039  
BT-Audio



AG3335MN  
GPS+GNSS  
Arm M4



GOODIX  
GH3026  
Heart rate sensor



BES2700iH  
BT/Audio

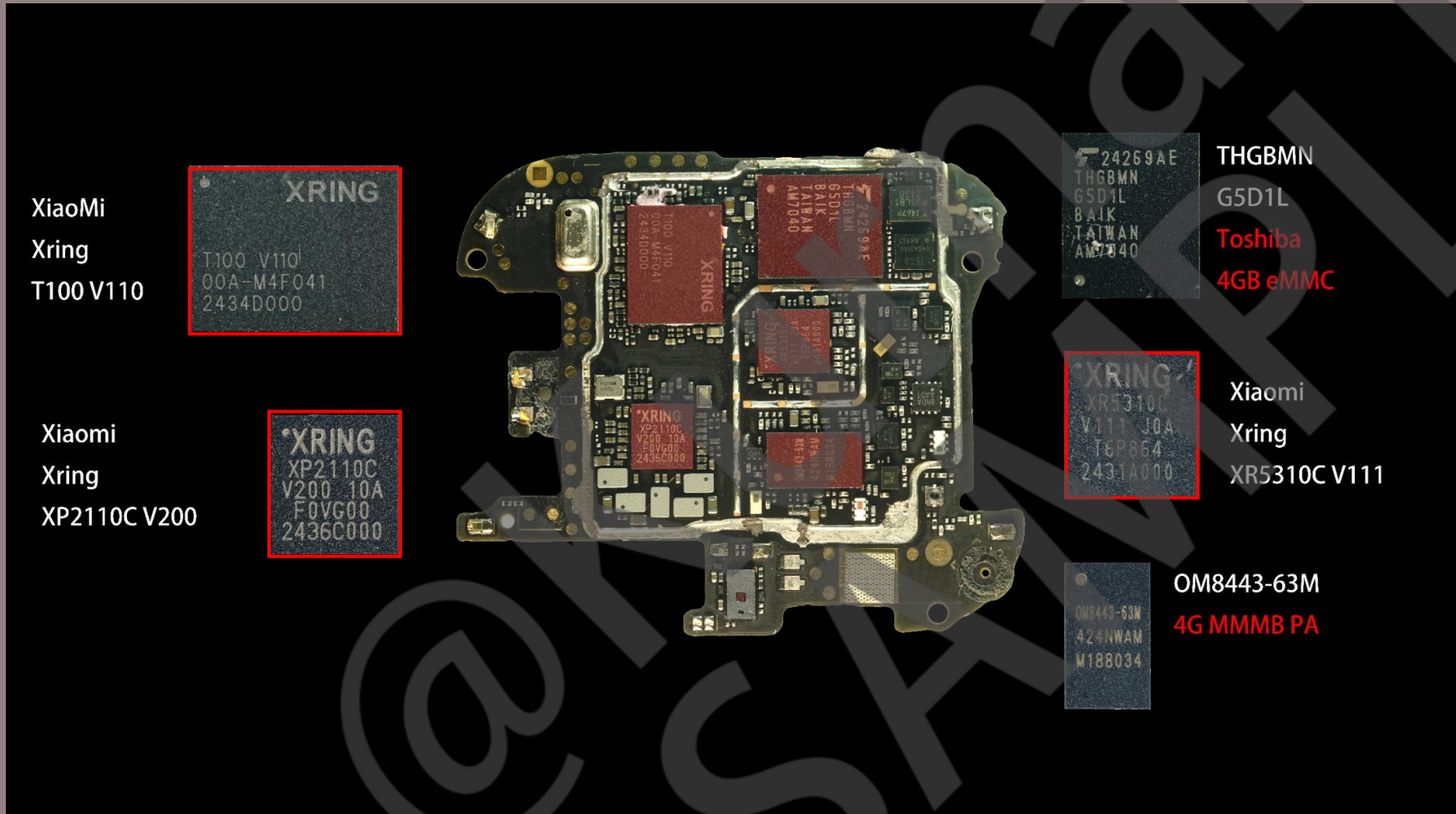


THN3 1SWC2  
NFC



BCM  
BK7258  
WIFI6/BT5.4





There have **3** Xring Chip on the Mother Board

# Xring analyze

T100 V110



Xring-T100 V100

1



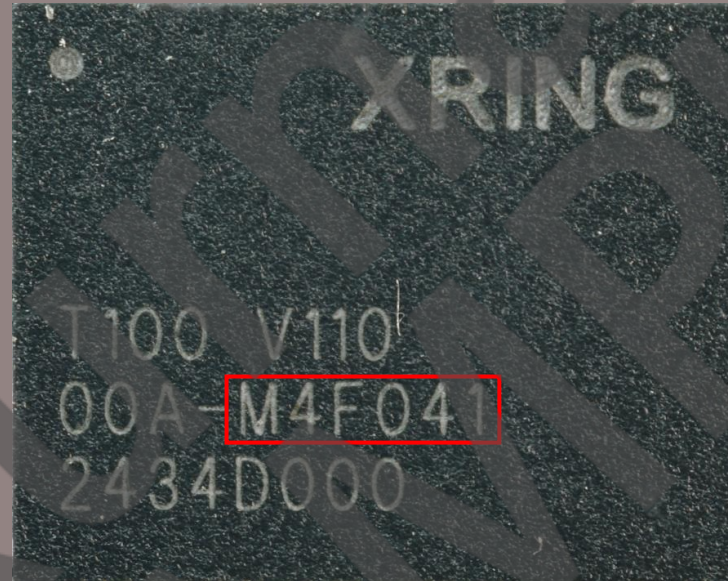
Xring-XR5310C VIII

2



XP2110CV200

3

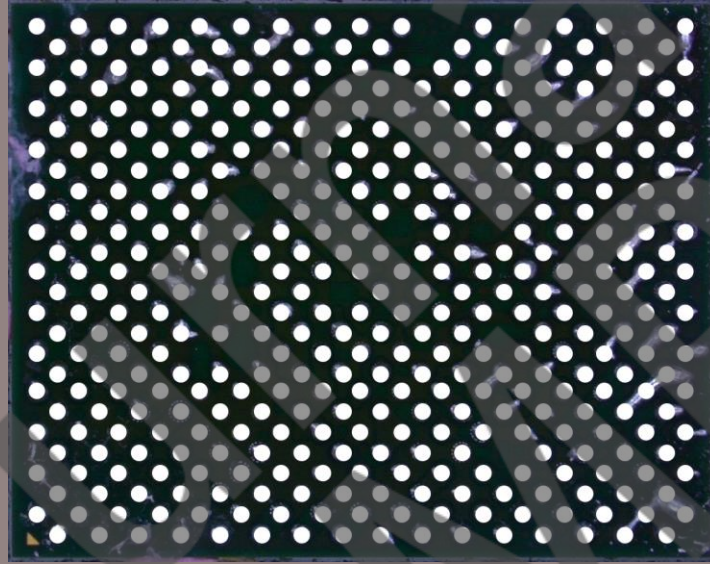


Xiaomi Xring LOGO

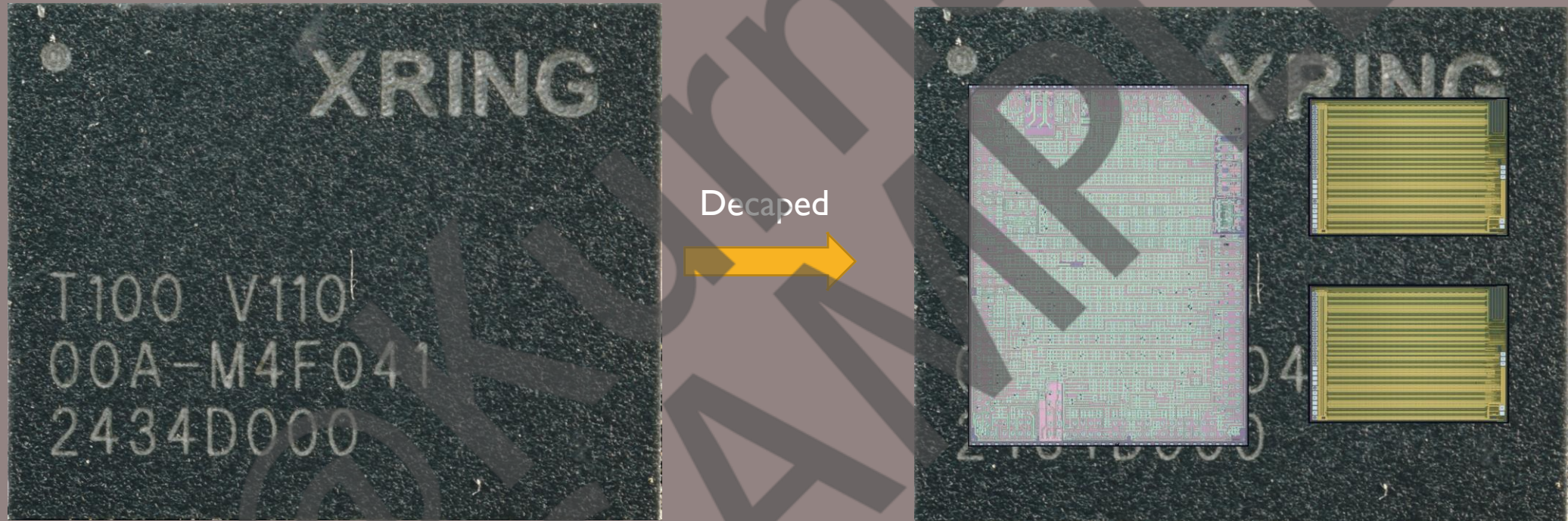
Product name: **T100**  
Version : **V110**

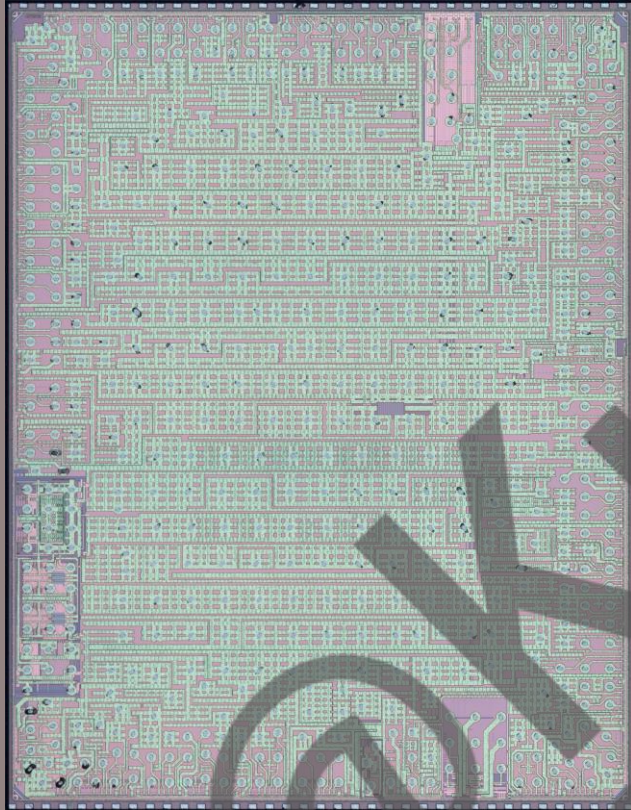
Packaged/Production Date  
**2024-34Week**

# Xring Chip-T100



Package Size: **6.72x8.48**  
Pad number: **429**





Xring T100 SoC view

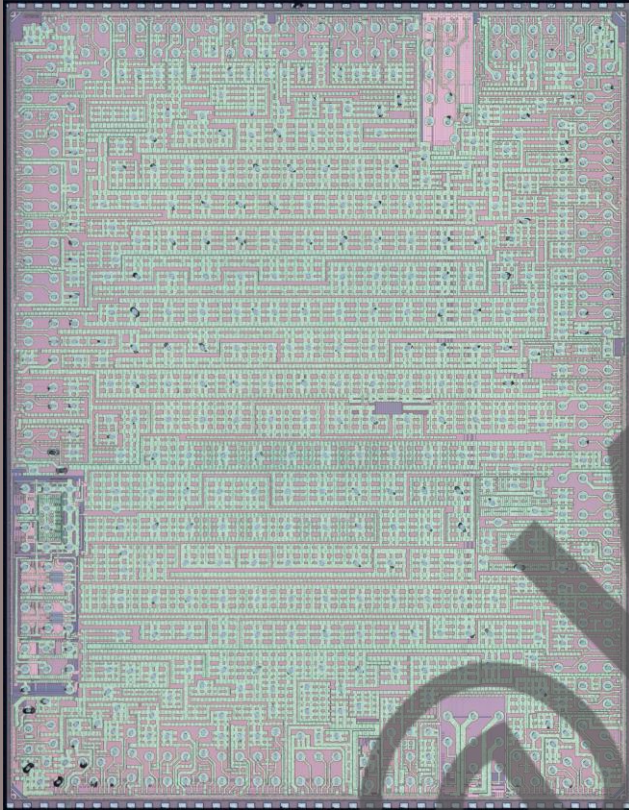


Xring T100 Memory Die view

There have 3 Dies In Xring T100 Package

- 1 T100 SoC Die
- 2 Memory Dies

# Xring Chip-T100-DPW

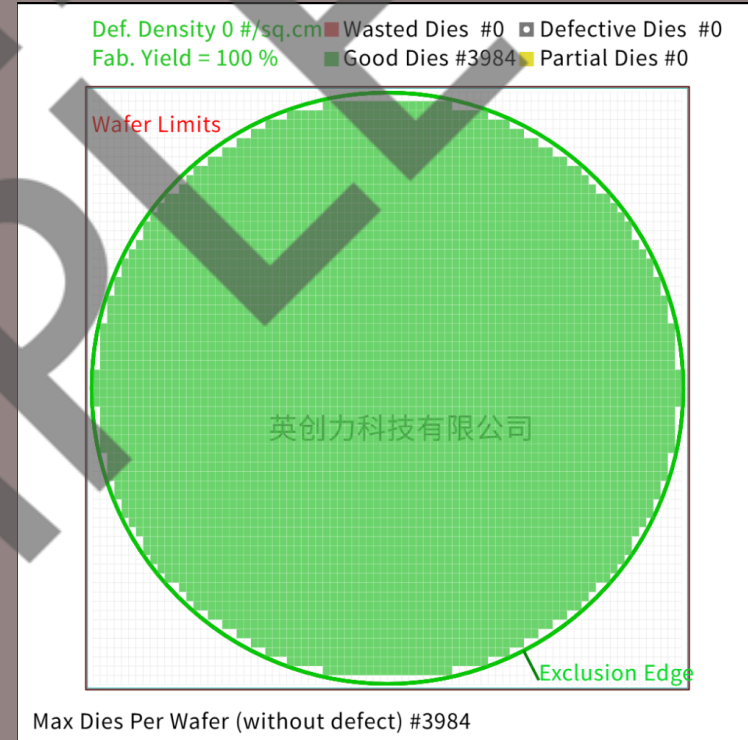


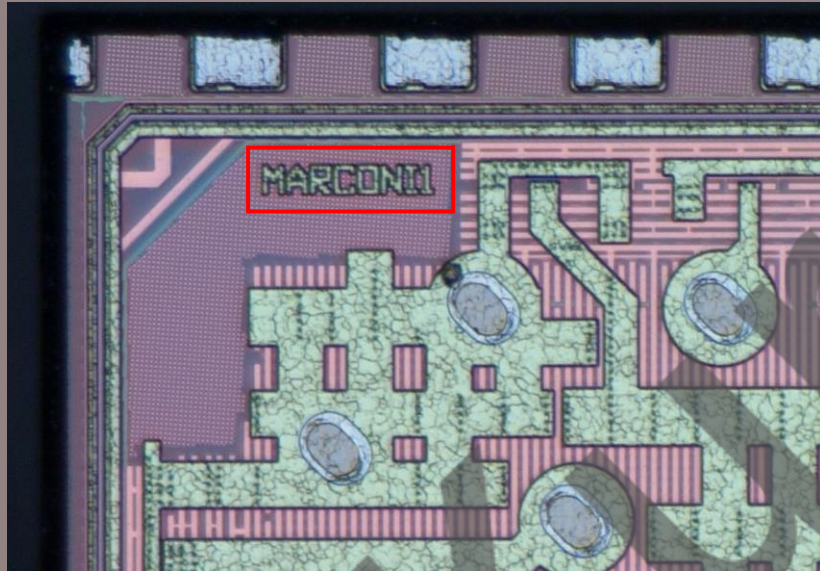
Xring T100 SoC view

Total Diesize: **17.1315mm<sup>2</sup>**  
(3.645mm x 4.7mm)

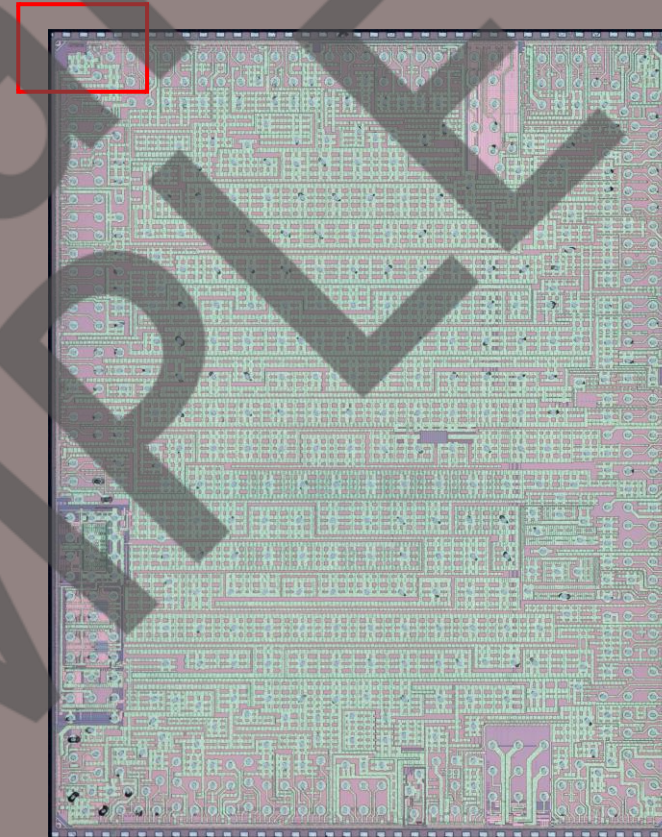
Used diesize: **14.868mm<sup>2</sup>**  
(3.41mm x 4.36mm)

Die Per Wafer: **3984**

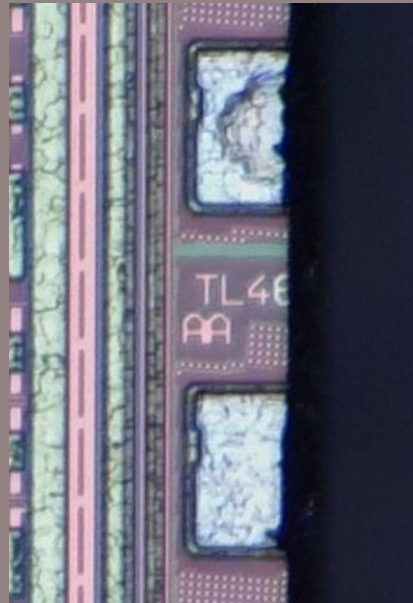




The Die Mark: **Marcon** |



Xring T100 SoC view



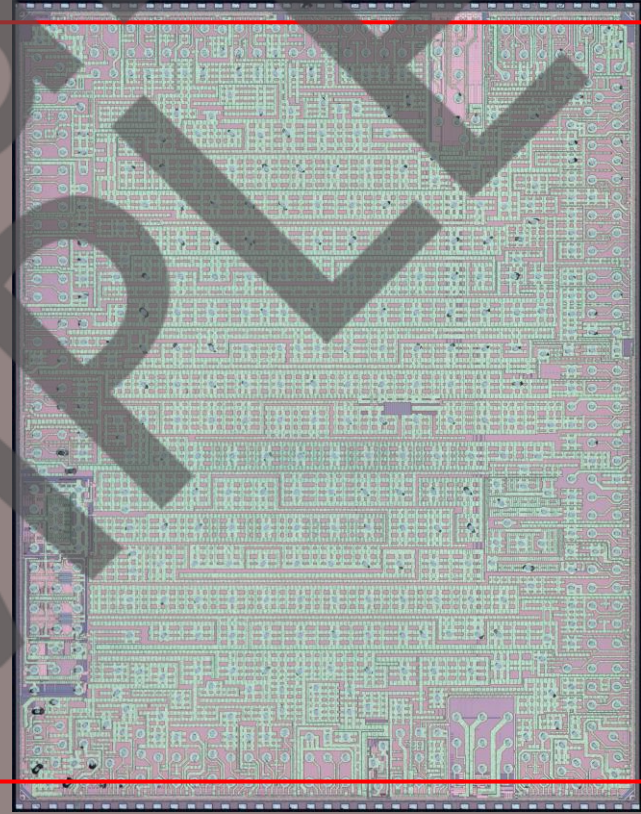
TL48XX AA



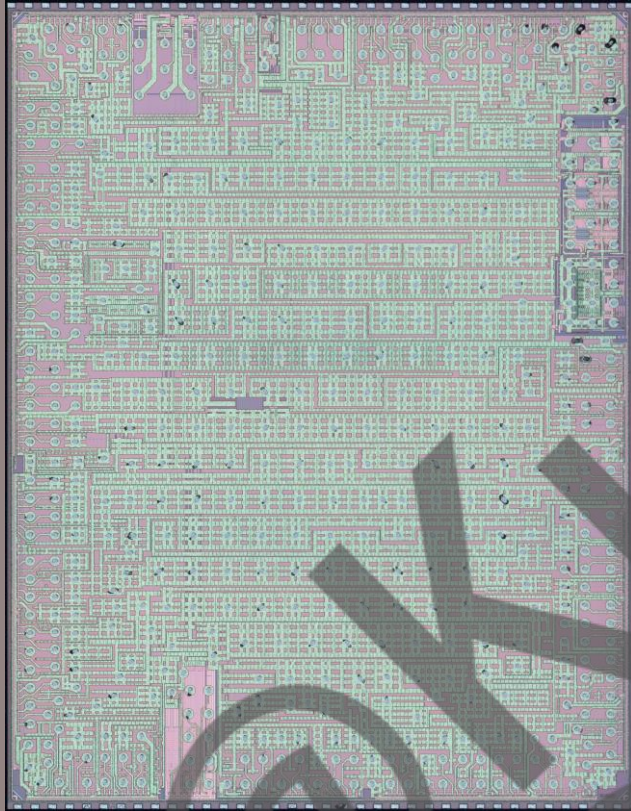
TL4979 AA



TL4979 AA



Xring T100 SoC view



Delayer





Chip Process: **TSMC 12nm**

TSMC	<b>N12</b>	<b>N12</b>	<b>N12</b>
Lib	UHD	HD	UHP
Gate Length	16/20/24	16/20/24	16/20/24
Gate Pitch	96	90	96
M2P	64	64	64
Track	6	9	12
Cell H	384	576	768
DDB/SDB	DDB	DDB	DDB
逻辑密度 (MTr)	33.64	22.42	16.82

Chip Process: **TSMC 12nm**

Used diesize: **14.868mm<sup>2</sup>**  
(3.41mm x 4.36mm)

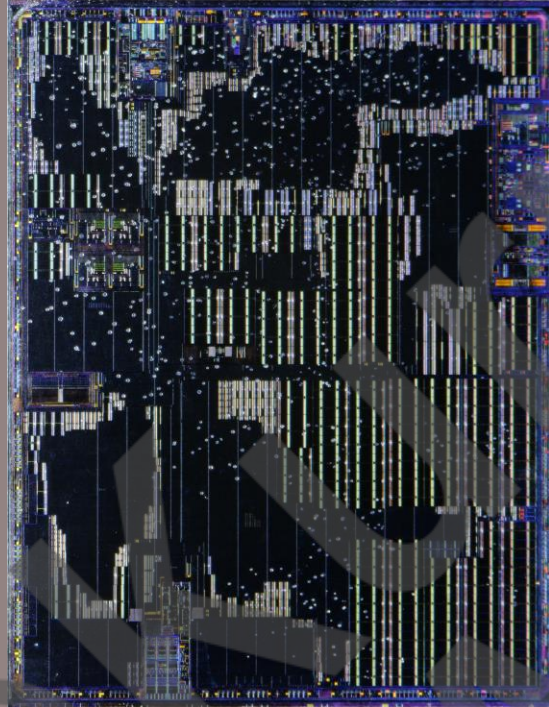
Estimate the number of transistors:  
**500.159Million (5.00159亿)**

TSMC	<b>N12</b>	<b>N12</b>	<b>N12</b>
Lib	UHD	HD	UHP
Gate Length	16/20/24	16/20/24	16/20/24
Gate Pitch	96	90	96
M2P	64	64	64
Track	6	9	12
Cell H	384	576	768
DDB/SDB	DDB	DDB	DDB
逻辑密度 (MTr)	33.64	22.42	16.82

XiaoMi Xring T100  
TSMC 12nm

Diesize: 14.868mm<sup>2</sup>

Transister number  
500.159Million



Middle-End



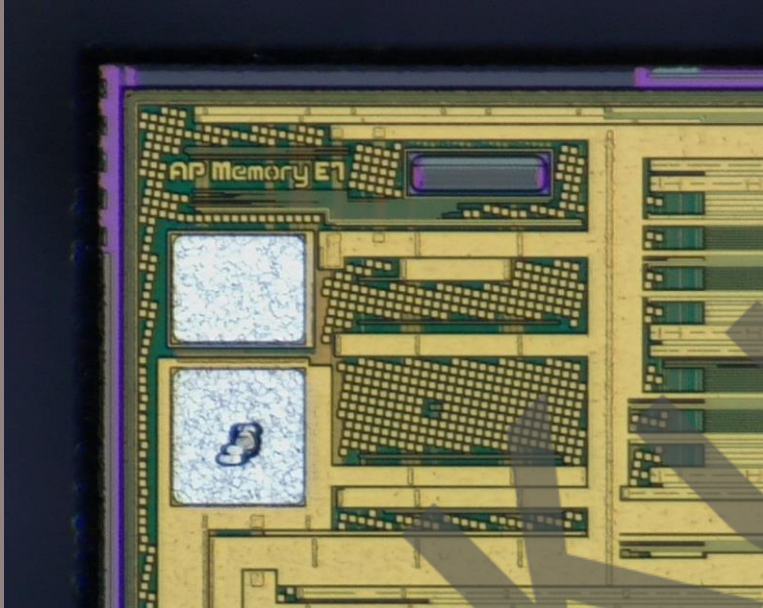
High-End

Qualcomm W5Gen I  
Samsung 4nm

Diesize: 16.78mm<sup>2</sup>

Transister number  
2120Million

# Xring Chip-T100-memory die



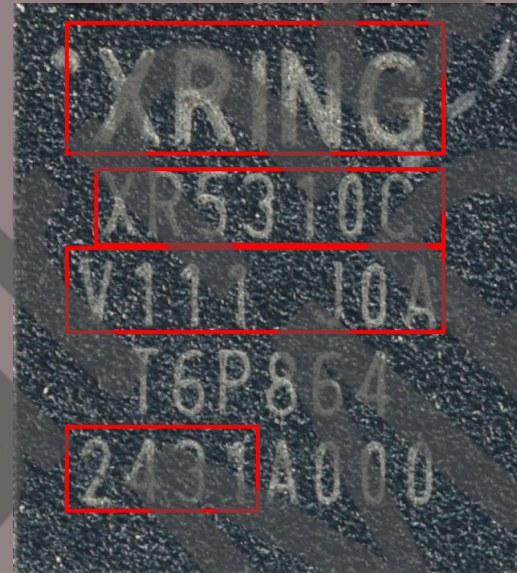
Memory die mark: **AP Memory E7**

# Xring analyze

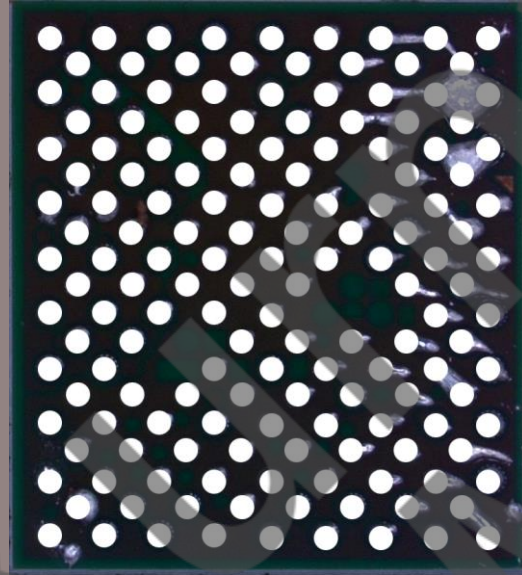
XR5310C

Product name: XR 5310C  
Version : VIII

Packaged/Production Date  
2024-31 Week



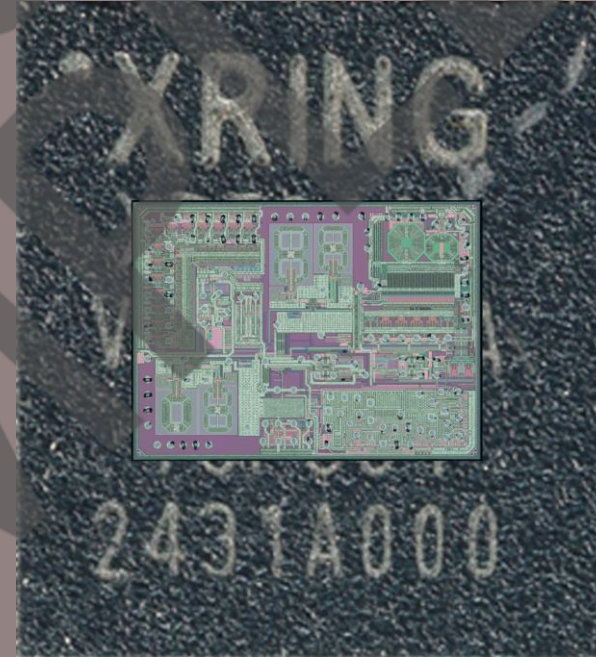
Xiaomi Xring LOGO

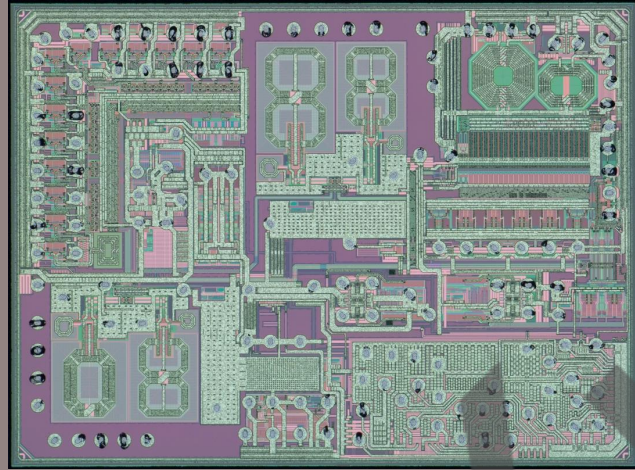


Package Size:  $4.53 \times 5.02 = 22.74 \text{mm}^2$   
Pad number: 156



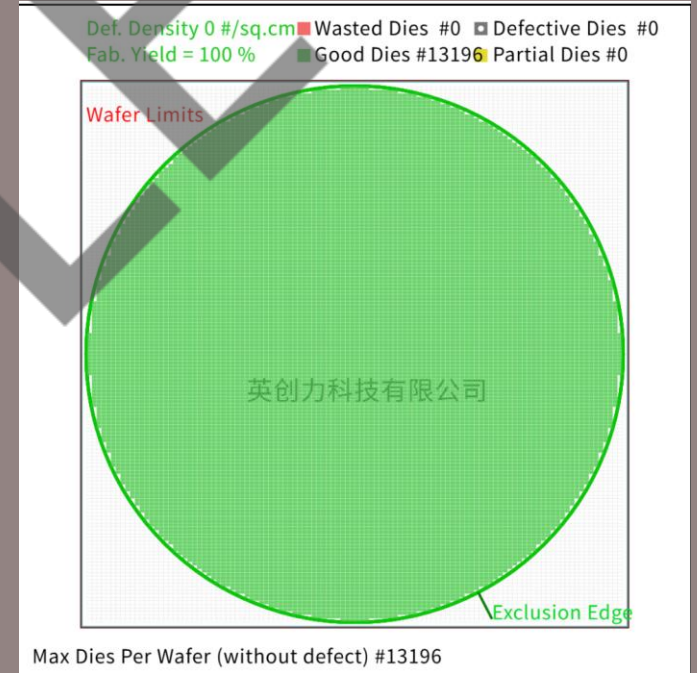
Decaped

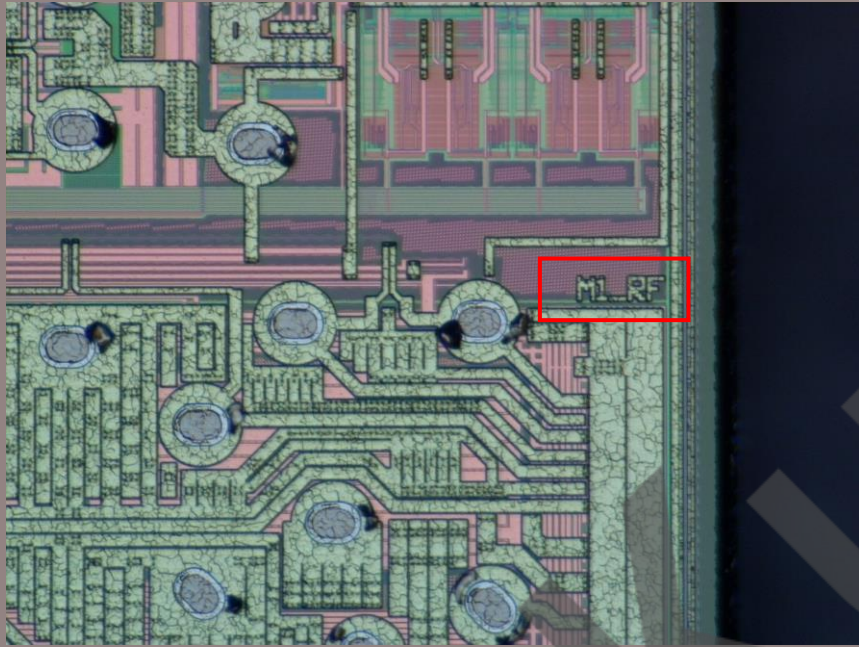




Xring XR5310C view

Total Diesize: **5.26mm<sup>2</sup>**  
(2.67mm × 1.97mm)  
Used diesize: **5.04mm<sup>2</sup>**  
(2.61mm × 1.93mm)  
Die Per Wafer(300mm): **13196**

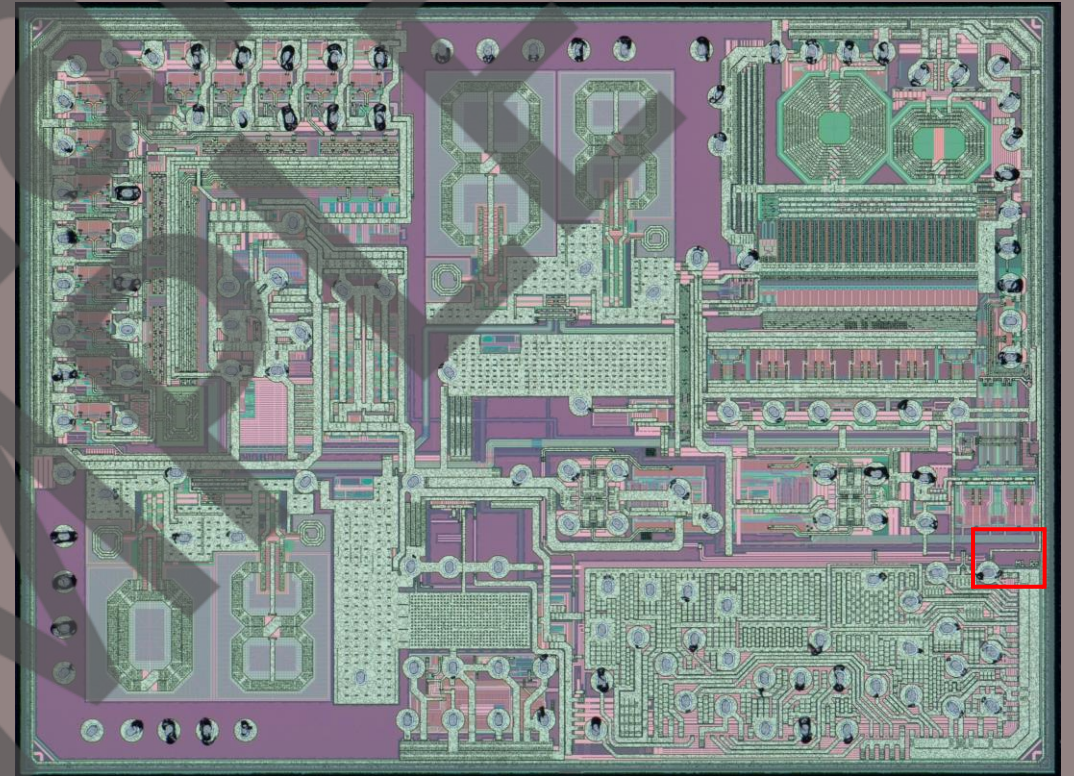




The Die Mark: **MI\_RF**

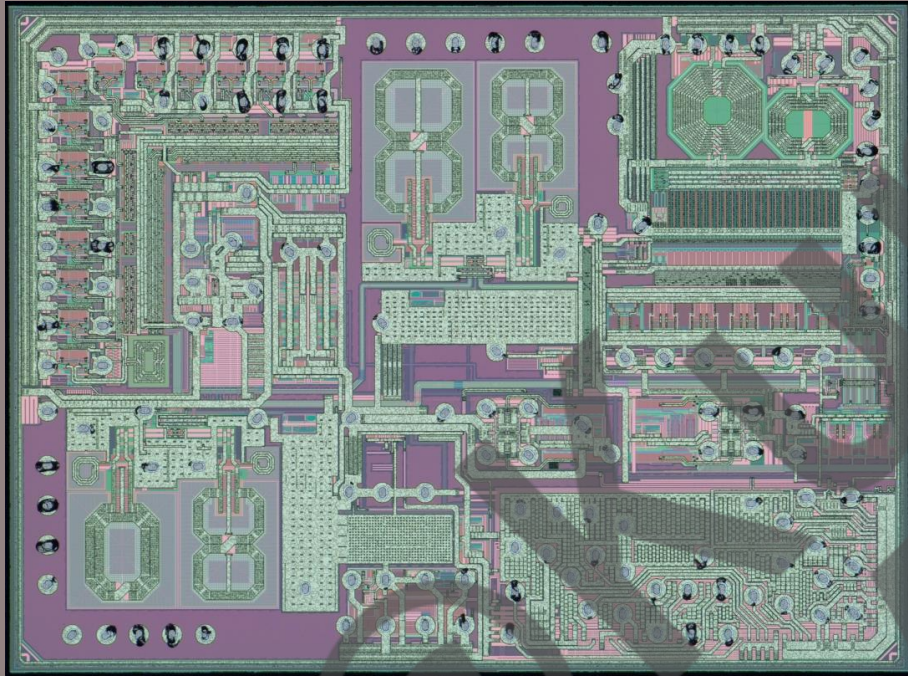


**MI=Macron I**



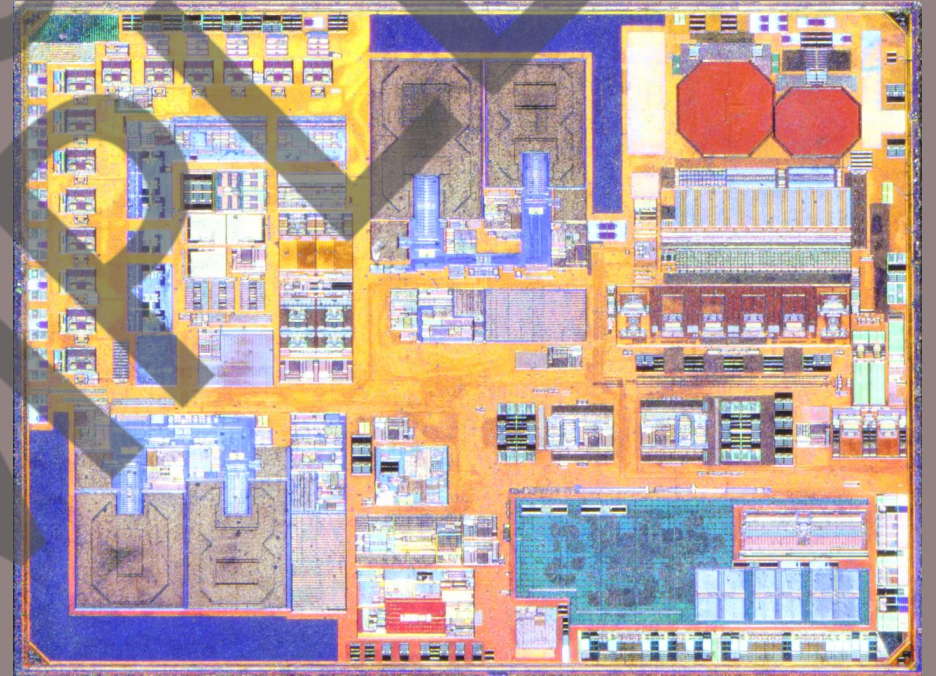
Xring XR5310C view

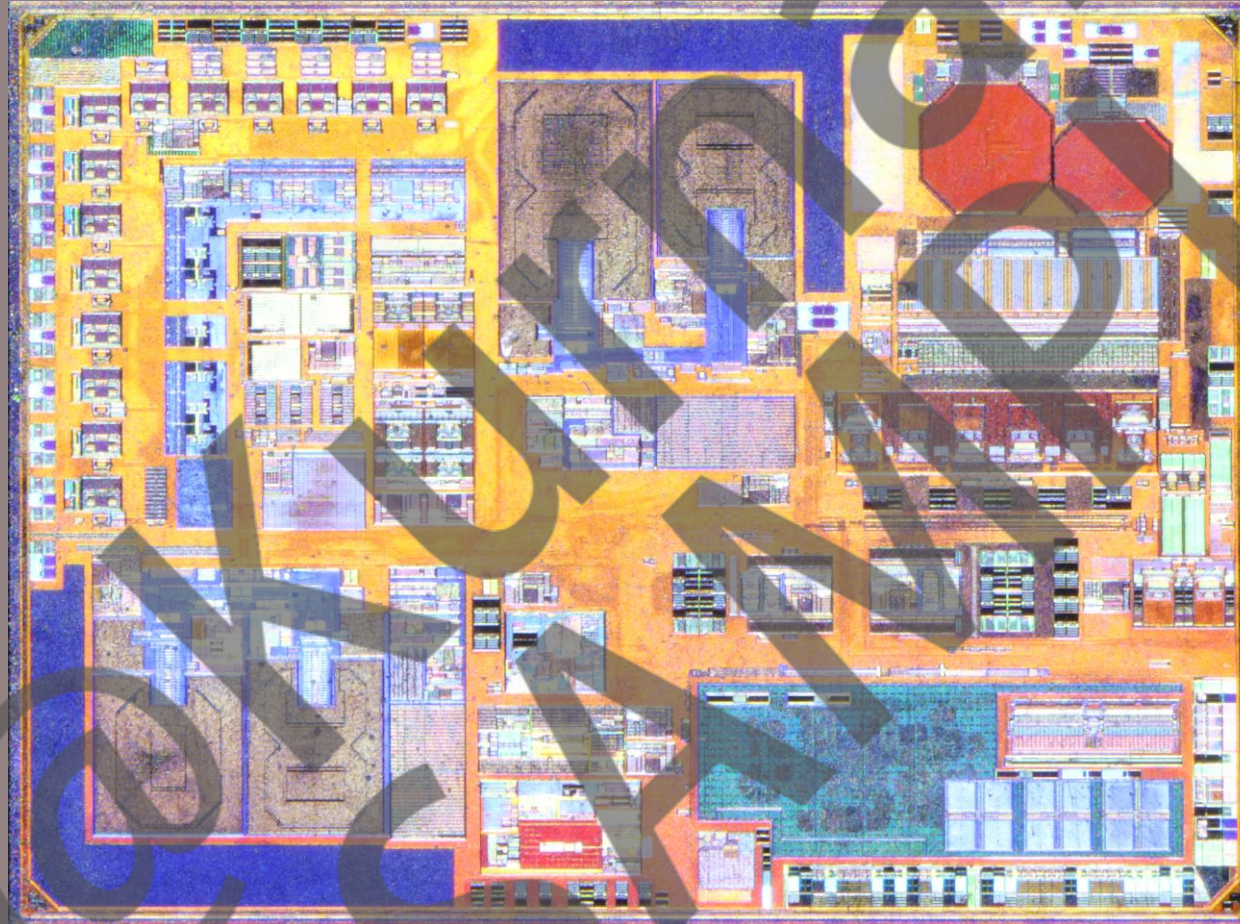
So this chip is **Macron I RF** chip



Xring XR5310C view

Delayer



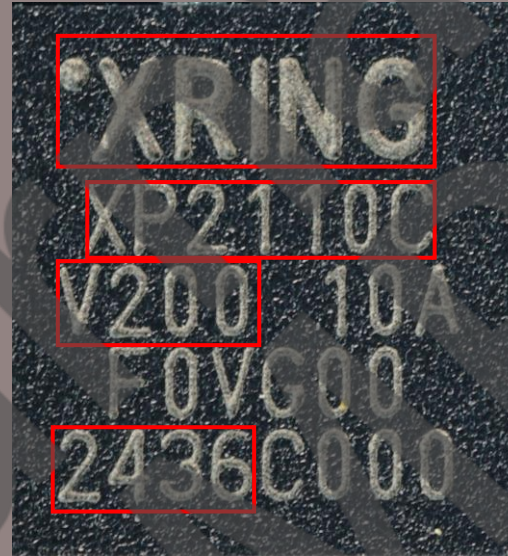


# Xring analyze

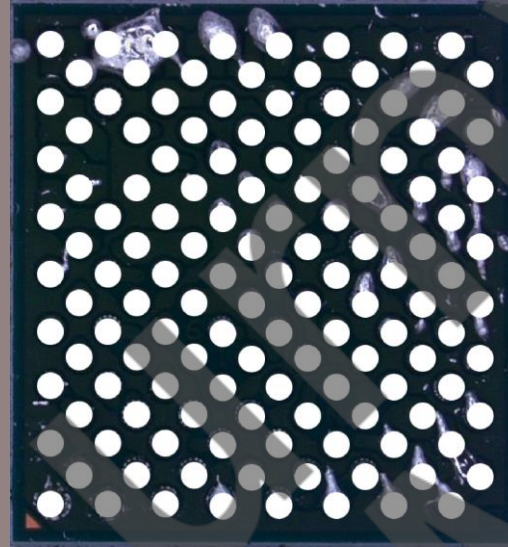
XP2110C

Product name: **XP2110C**  
Version : **V200**

Packaged/Production Date  
**2024-36Week**



Xiaomi Xring LOGO

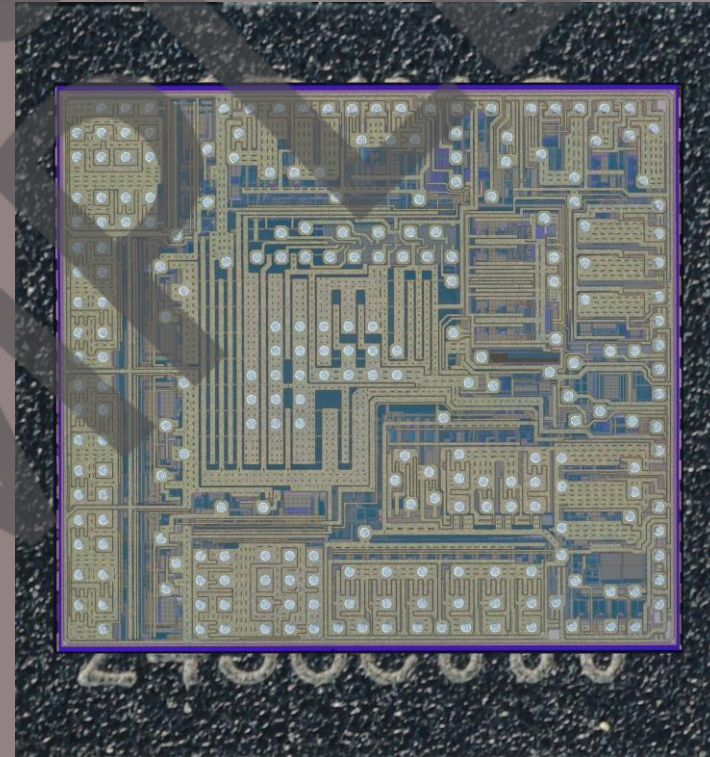


Package Size:  $4.64 \times 4.33 = 20.09 \text{mm}^2$

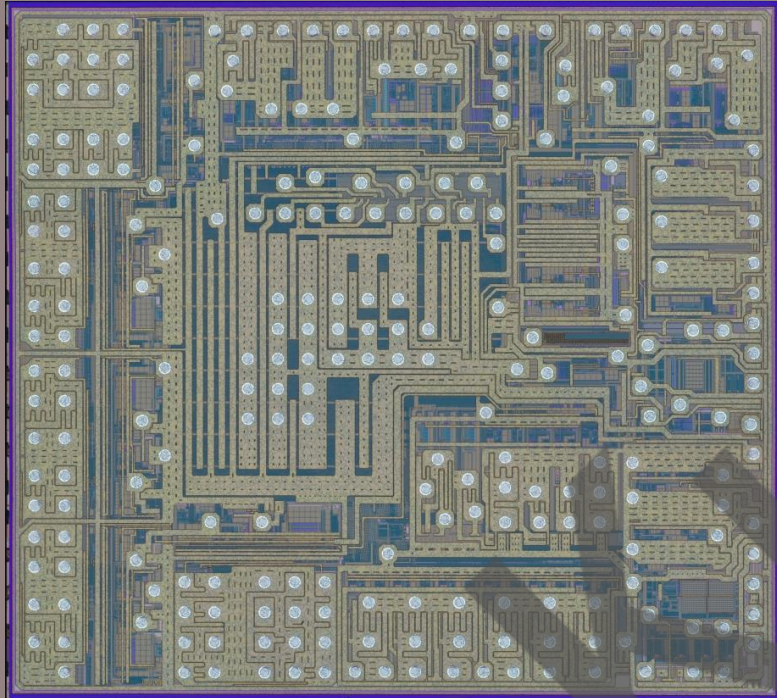
Pad number: 135



Decaped



# Xring Chip-XP2110C

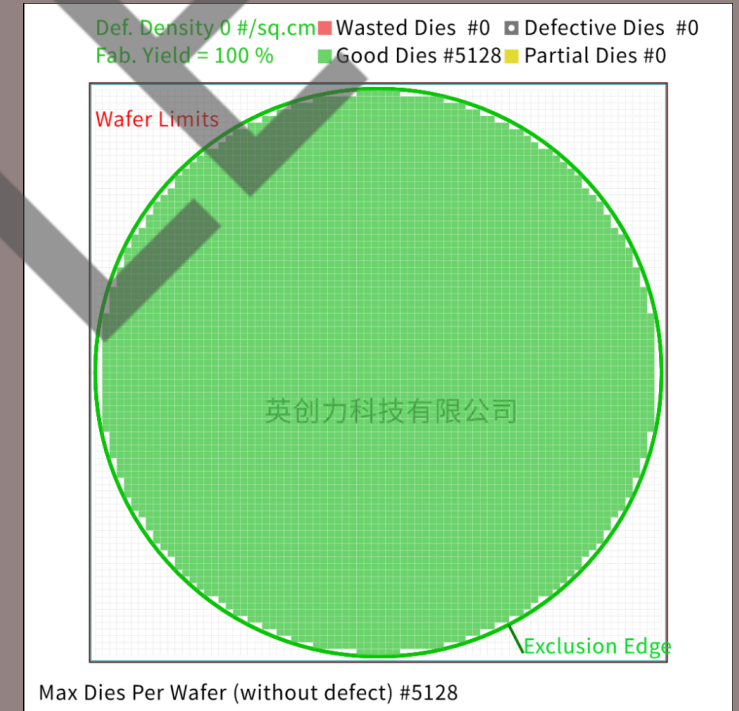


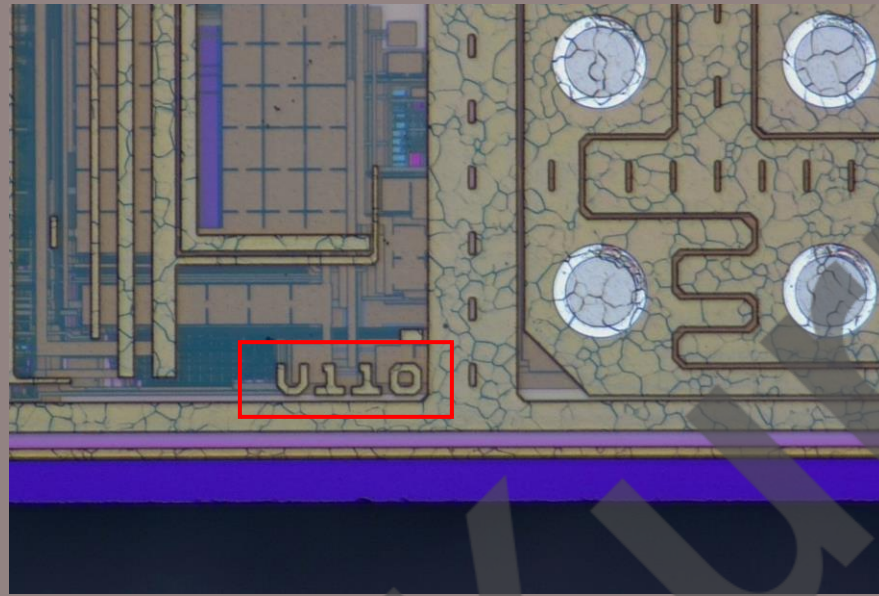
Xring XP2110C view

Total Diesize: **14.42mm<sup>2</sup>**  
(3.85mm x 3.475mm)

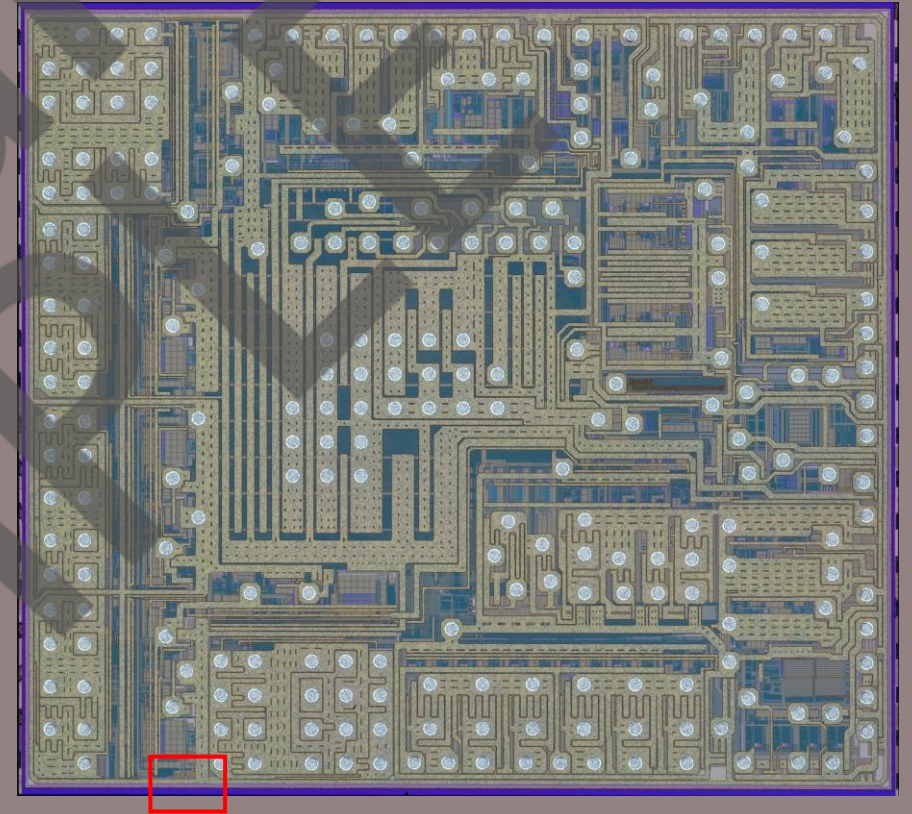
Used diesize: **12.566mm<sup>2</sup>**  
(3.74mm x 3.36mm)

Die Per Wafer=(300mm): **5128**

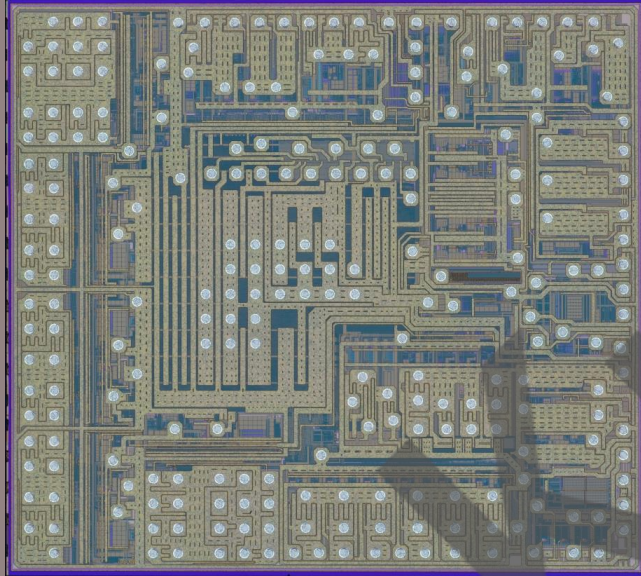




The Die Mark: **U110**

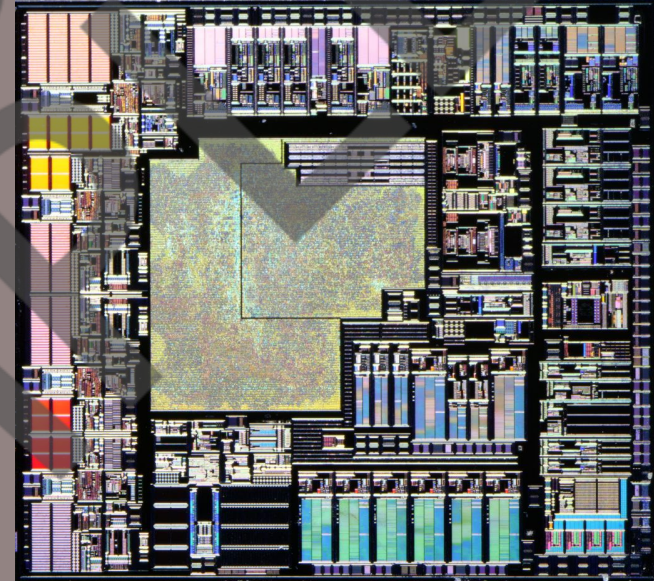


Xring XP2110C view

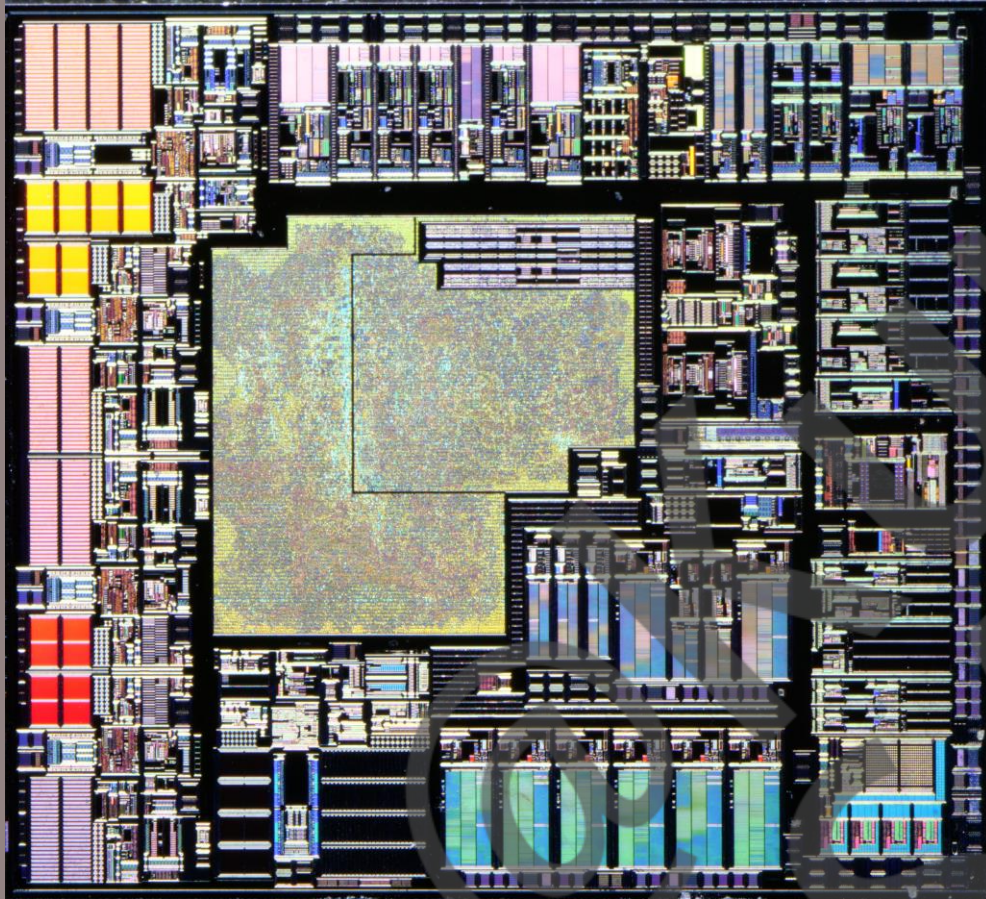


Xring XP2110C view

Delayer



Xring XP2110C Dieshot view



Xring XP2110C Dieshot view

This Chip is **PMIC**  
(Power Management Integrated Circuit)